GigaDevice Semiconductor Inc.

GD32L235xx
Arm® Cortex®-M23 32-bit MCU

Datasheet

Revision 2.2

(Jan. 2026)

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1. General description

The GD32L235xx device belongs to the value line of GD32 MCU family. It is a new 32-bit general-purpose microcontroller based on the ARM® Cortex®-M23 core. The Cortex-M23 processor is an energy-efficient processor with a very low gate count. It is intended to be used for microcontroller and deeply embedded applications that require an area-optimized processor. The processor delivers high energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier and a 17-cycle divider.

The GD32L235xx device incorporates the ARM® Cortex®-M23 32-bit processor core operating at up to 64 MHz frequency with Flash accesses 0~2 wait states to obtain maximum efficiency. It provides up to 128 KB embedded Flash memory and up to 24 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer one 12-bit ADC, one DAC, two comparators, up to six general 16-bit timers, two basic timers, one advanced timer and two 16-bit low power timers, as well as standard and advanced communication interfaces: up to two SPIs, three I2Cs, two USARTs, two UARTs, an I2S, a CAN, an USBD and two LPUARTs. Additional peripherals as segment LCD controller (SLCD), cryptographic acceleration unit (CAU) are included.

The device operates from a 1.71 to 3.63 V power supply and available in -40 to +85 °C temperature range for grade 6 devices, and -40°C to +105°C temperature range for grade 7 devices. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make the GD32L235xx devices suitable for a wide range of applications, especially in areas such as industrial control, motor drives, user interface, power monitor and alarm systems, consumer and handheld equipment, gaming and GPS, E-bike and so on.

2. Device overview

2.1. Device information

Table 2-1. GD32L235xx devices features and peripheral list

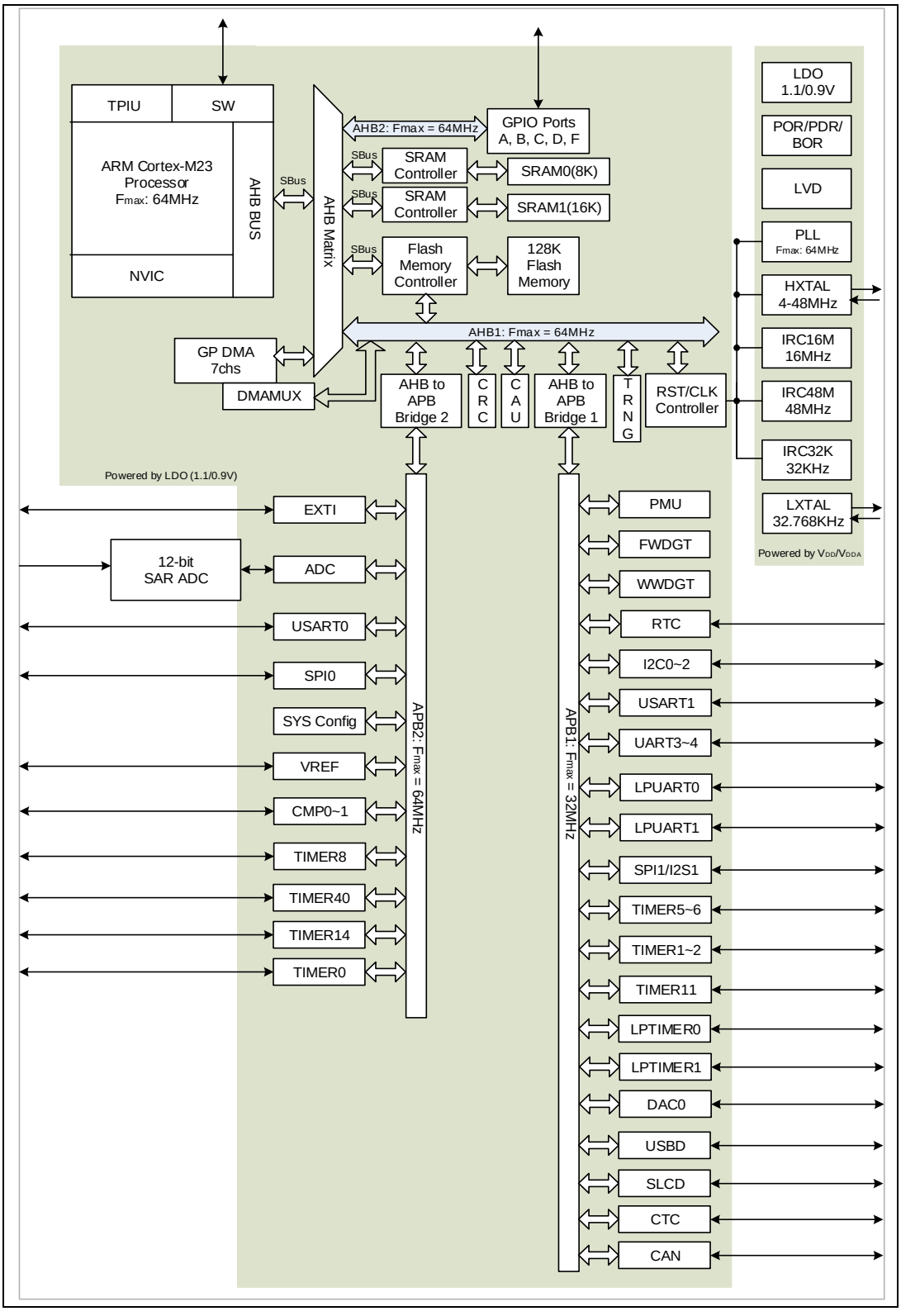
Part Number		GD32L235xx											
		E8Y6	EBY6	K8Q6	K8Q7	KBQ6	KBQ7	K8Q6P	KBQ6P	K8T6	KBT6	C8O6	CBO6
FLASH (KB)		64	128	64	64	128	128	64	128	64	128	64	128
SRAM (KB)		12	24	12	12	24	24	12	24	12	24	12	24
Timers	Advanced timer(16-bit)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)
	General timer(16-bit)	5 (1, 2, 8,11,14)	6 (1, 2, 8,11,14,40)	5 (1, 2, 8,11,14)	5 (1, 2, 8,11,14)	6 (1, 2, 8,11,14,40)	6 (1, 2, 8,11,14,40)	5 (1, 2, 8,11,14)	6 (1, 2, 8,11,14,40)	5 (1, 2, 8,11,14)	6 (1, 2, 8,11,14,40)	5 (1, 2, 8,11,14)	6 (1, 2, 8,11,14,40)
	Low power timer(16-bit)	2	2	2	2	2	2	2	2	2	2	2	2
	SysTick	1	1	1	1	1	1	1	1	1	1	1	1
	Basic timer(16-bit)	2 (5, 6)	2 (5, 6)	2 (5, 6)	2 (5, 6)	2 (5, 6)	2 (5, 6)	2 (5, 6)	2 (5, 6)	2 (5, 6)	2 (5, 6)	2 (5, 6)	2 (5, 6)
	Watchdog	2	2	2	2	2	2	2	2	2	2	2	2
	RTC	1	1	1	1	1	1	1	1	1	1	1	1
Connectivity	UART	1 (3)	2 (3, 4)	1 (3)	1 (3)	2 (3, 4)	2 (3, 4)	1 (3)	2 (3, 4)	1 (3)	2 (3, 4)	1 (3)	2 (3, 4)
	USART	2 (0, 1)	2 (0, 1)	2 (0, 1)	2 (0, 1)	2 (0, 1)	2 (0, 1)	2 (0, 1)	2 (0, 1)	2 (0, 1)	2 (0, 1)	2 (0, 1)	2 (0, 1)
	LPUART	2	2	2	2	2	2	2	2	2	2	2	2
	I2C	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)
	SPI/I2S	2/1 (0-1)/(1)	2/1 (0-1)/(1)	2/1 (0-1)/(1)	2/1 (0-1)/(1)	2/1 (0-1)/(1)	2/1 (0-1)/(1)	2/1 (0-1)/(1)	2/1 (0-1)/(1)	2/1 (0-1)/(1)	2/1 (0-1)/(1)	2/1 (0-1)/(1)	2/1 (0-1)/(1)
	CAN	1	1	1	1	1	1	1	1	1	1	1	1
	USBD	0	0	1	1	1	1	1	1	1	1	1	1
GPIO		22	22	29	29	29	29	28	28	27	27	43	43
ADC	Units	1	1	1	1	1	1	1	1	1	1	1	1
	Channels (External)	10	10	10	10	10	10	10	10	10	10	10	10
	Channels (Internal)	4	4	4	4	4	4	4	4	4	4	4	4
DAC		1	1	1	1	1	1	1	1	1	1	1	1
CMP		2	2	2	2	2	2	2	2	2	2	2	2
SLCD		0	0	0	0	0	0	0	0	0	0	0	0
Package		WLCSP25		QFN32				QFN32		LQFP32		QFN48	

Table 2-2. GD32L235xx devices features and peripheral list (Continue.)

Part Number		GD32L235xx							
		C8T6	CBT6	CBT7	R8O6	RBO6	R8T6	RBT6	RBT7
FLASH (KB)		64	128	128	64	128	64	128	128
SRAM (KB)		12	24	24	12	24	12	24	24
Timers	Advanced timer(16-bit)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)
	General timer(16-bit)	5 (1, 2, 8,11,14)	6 (1, 2, 8,11,14,40)	6 (1, 2, 8,11,14,40)	5 (1, 2, 8,11,14)	6 (1, 2, 8,11,14,40)	5 (1, 2, 8,11,14)	6 (1, 2, 8,11,14,40)	6 (1, 2, 8,11,14,40)
	Low power timer(16-bit)	2	2	2	2	2	2	2	2
	SysTick	1	1	1	1	1	1	1	1
	Basic timer(16-bit)	2 (5, 6)	2 (5, 6)	2 (5, 6)	2 (5, 6)	2 (5, 6)	2 (5, 6)	2 (5, 6)	2 (5, 6)
	Watchdog	2	2	2	2	2	2	2	2
	RTC	1	1	1	1	1	1	1	1
Connectivity	UART	1 (3)	2 (3, 4)	2 (3, 4)	1 (3)	2 (3, 4)	1 (3)	2 (3, 4)	2 (3, 4)
	USART	2 (0, 1)	2 (0, 1)	2 (0, 1)	2 (0, 1)	2 (0, 1)	2 (0, 1)	2 (0, 1)	2 (0, 1)
	LPUART	2	2	2	2	2	2	2	2
	I2C	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)
	SPI/I2S	2/1 (0-1)/(1)	2/1 (0-1)/(1)	2/1 (0-1)/(1)	2/1 (0-1)/(1)	2/1 (0-1)/(1)	2/1 (0-1)/(1)	2/1 (0-1)/(1)	2/1 (0-1)/(1)
	CAN	1	1	1	1	1	1	1	1
	USBD	1	1	1	1	1	1	1	1
GPIO		43	43	43	59	59	59	59	59
ADC	Units	1	1	1	1	1	1	1	1
	Channels (External)	10	10	10	16	16	16	16	16
	Channels (Internal)	4	4	4	4	4	4	4	4
DAC		1	1	1	1	1	1	1	1
CMP		2	2	2	2	2	2	2	2
SLCD		0	0	0	1	1	1	1	1
Package		LQFP48			QFN64		LQFP64		

2.2. Block diagram

Figure 2-1. GD32L235xx block diagram



2.3. Pinouts and pin assignment

Figure 2-2. GD32L235Rx LQFP64 pinouts

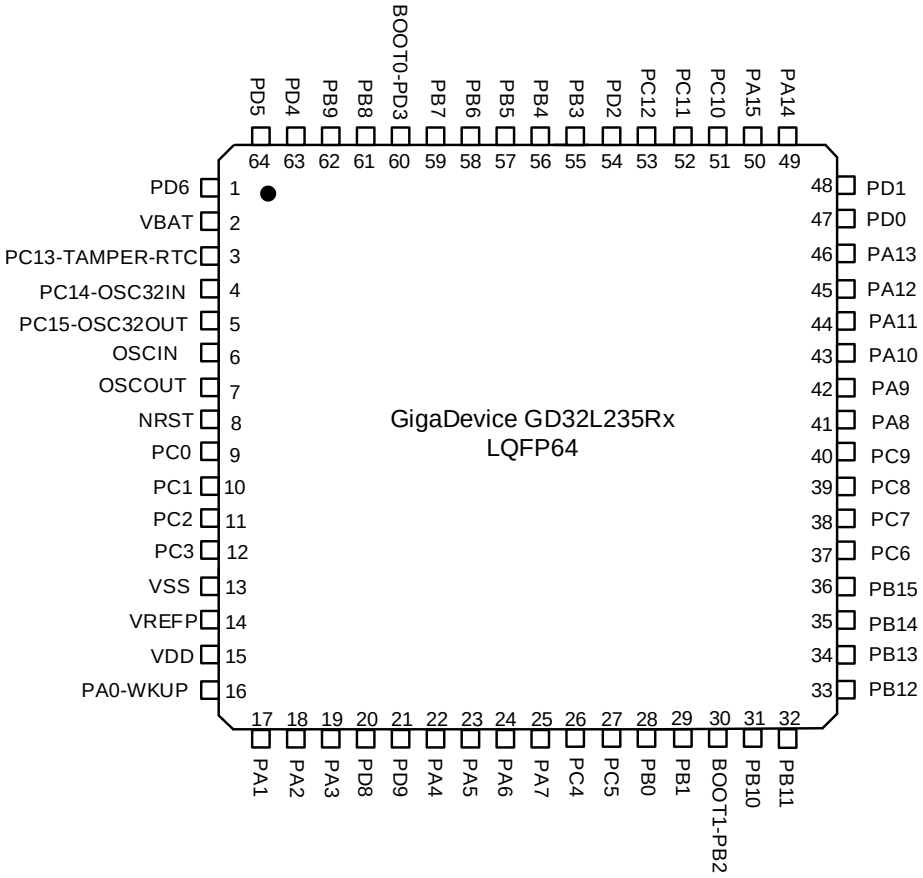


Figure 2-3. GD32L235Rx QFN64 pinouts

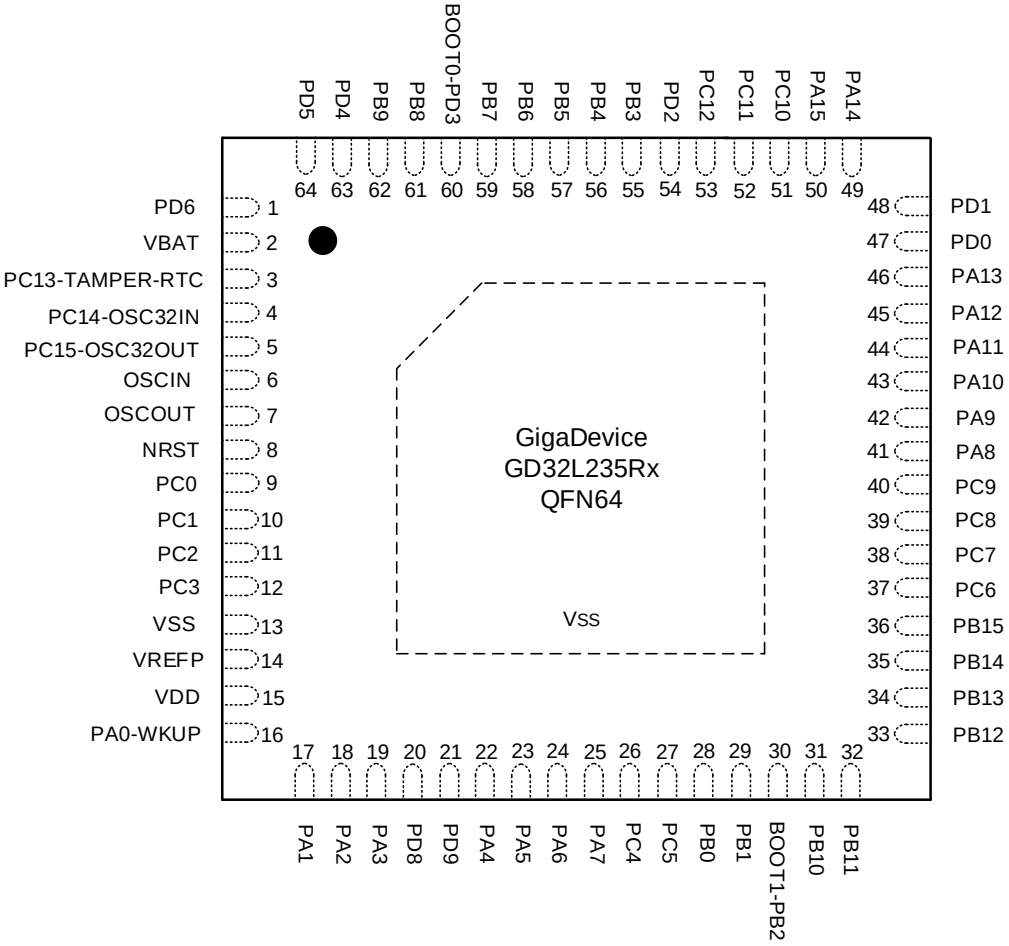


Figure 2-4. GD32L235Cx LQFP48 pinouts

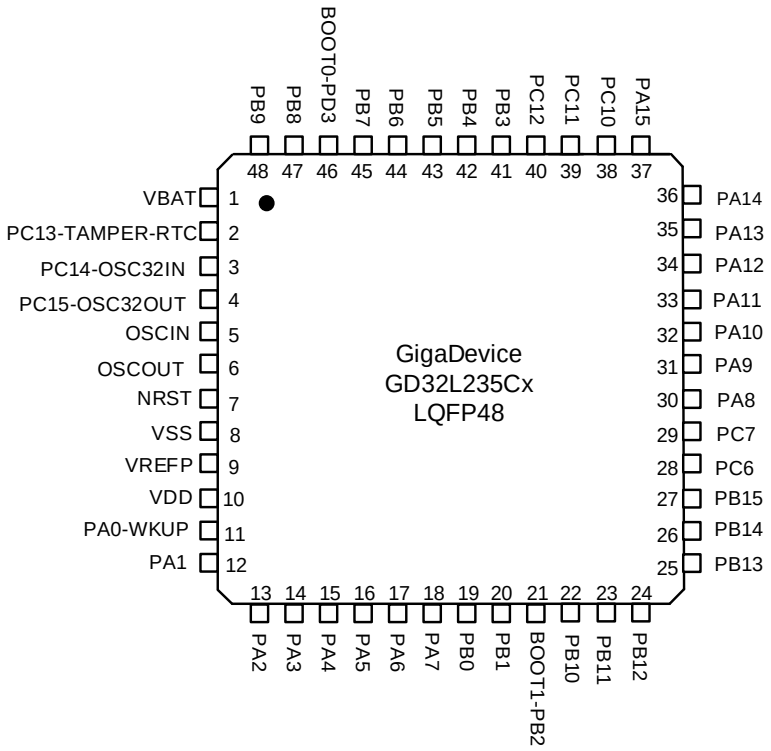


Figure 2-5. GD32L235Cx QFN48 pinouts

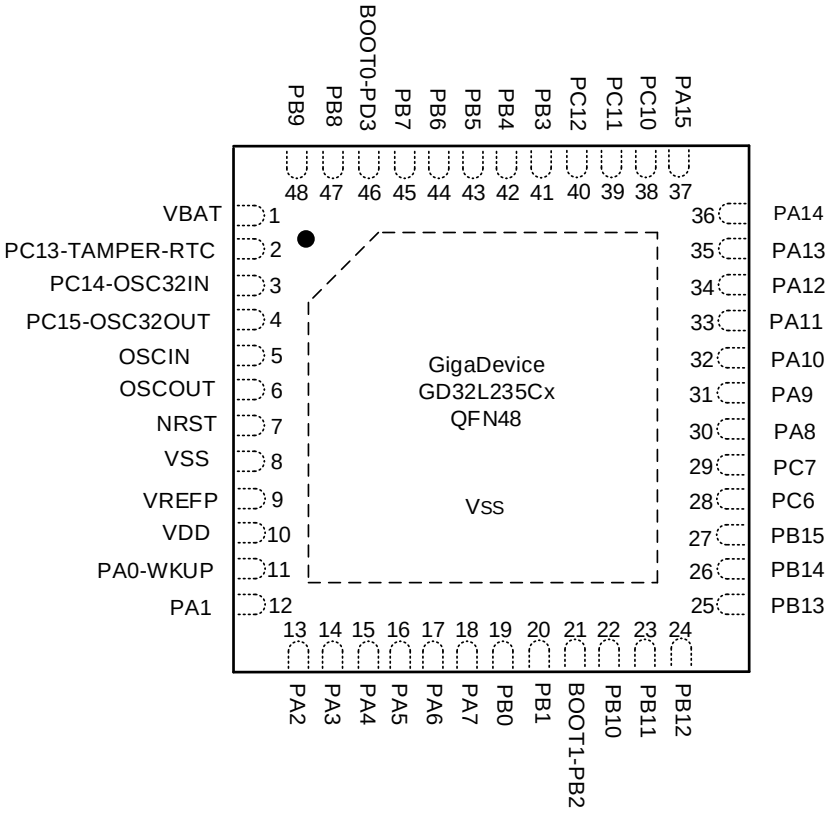


Figure 2-6. GD32L235Kx LQFP32 pinouts

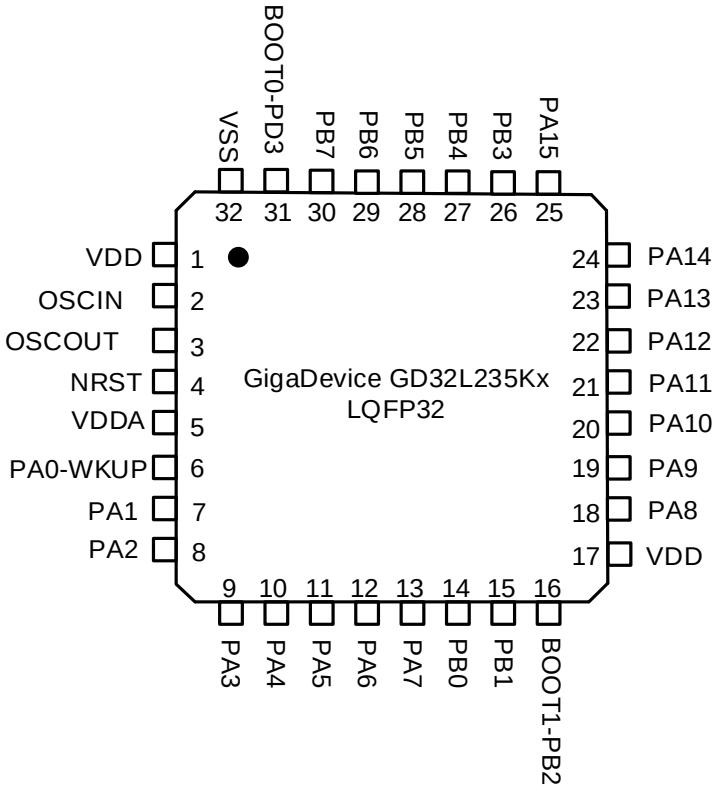


Figure 2-7. GD32L235Kx QFN32 pinouts

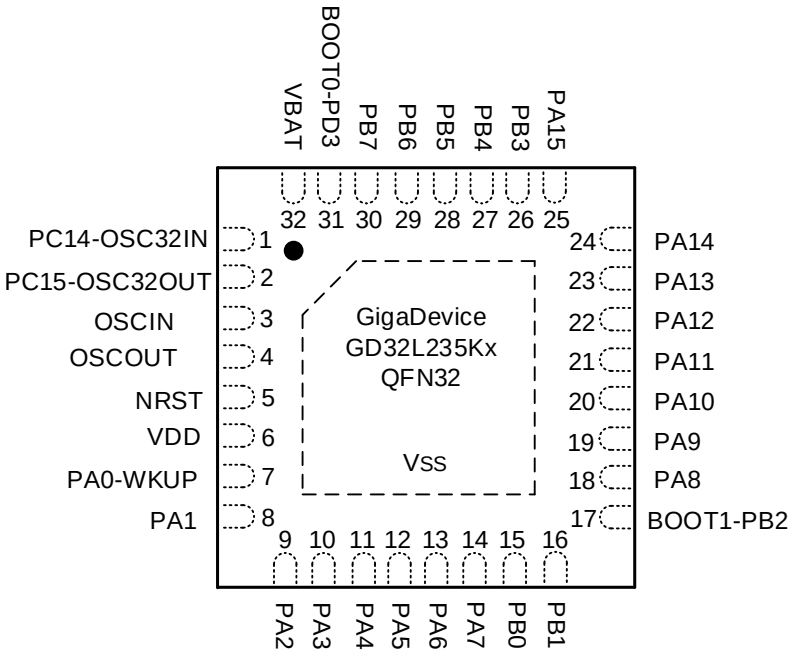


Figure 2-8. GD32L235KxxxP QFN32 VREFP pinouts

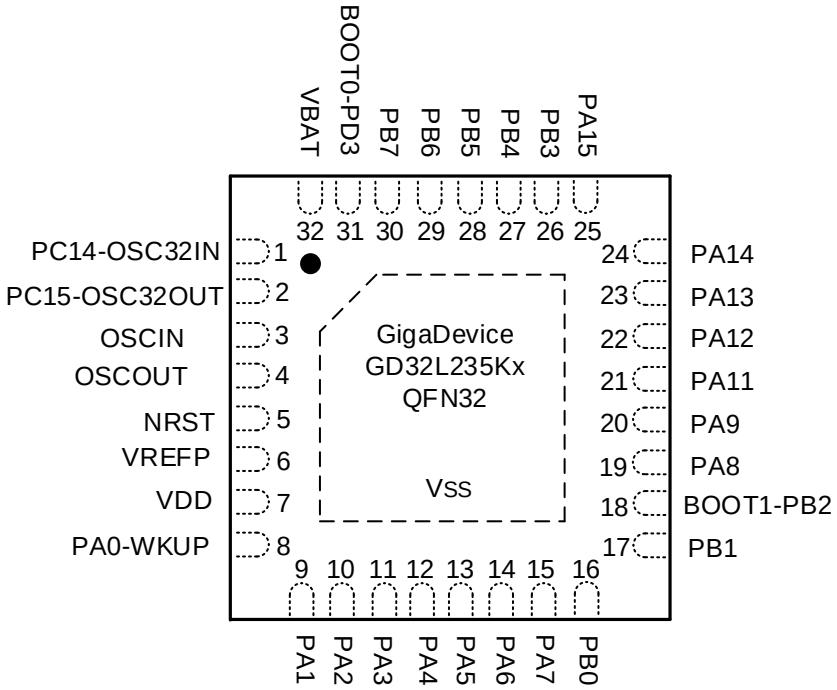
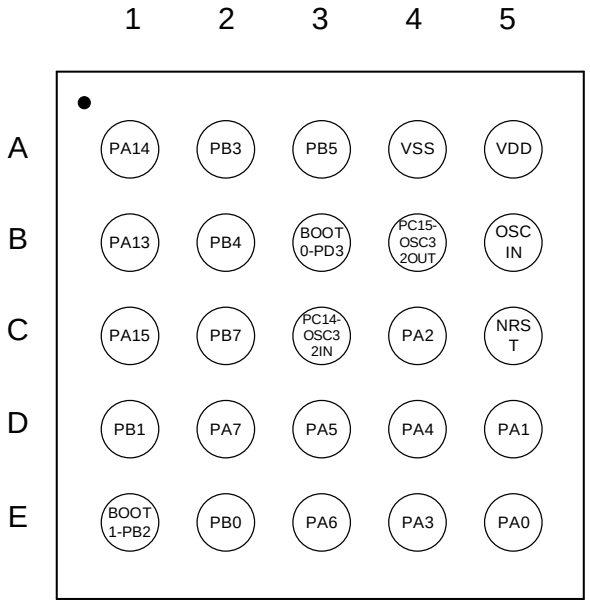


Figure 2-9. GD32L235Ex WLCSP25 pinouts



2.4. Memory map

Table 2-3. GD32L235xx memory map

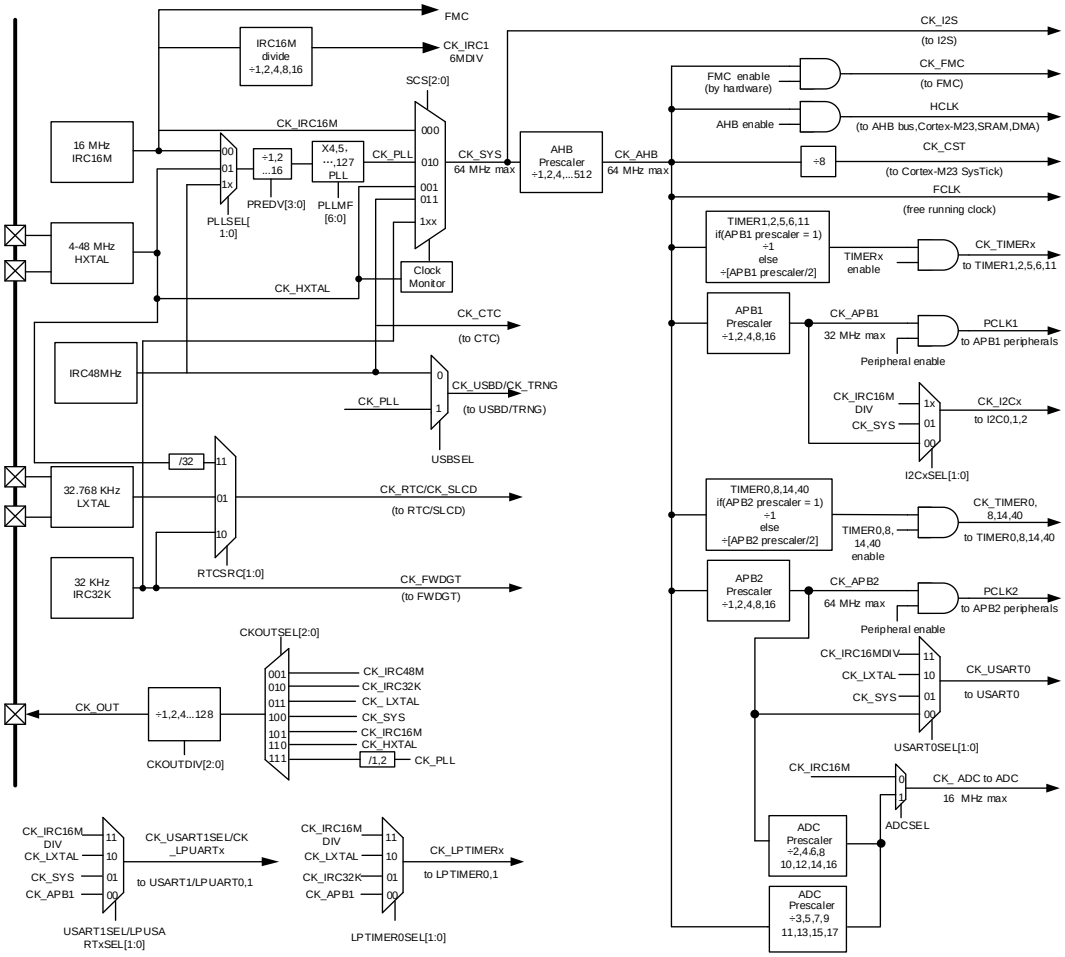
Pre-defined Regions	Bus	ADDRESS	Peripherals
		0xE000 0000 – 0xE00F FFFF	Cortex®-M23 internal peripherals
External Device		0xA000 0000 – 0xDFFF FFFF	Reserved
External RAM		0x60000000 – 0x9FFFFFFF	Reserved
Peripherals	AHB1	0x5006 1000 – 0x5FFF FFFF	Reserved
		0x5006 0C00 – 0x5006 0FFF	Reserved
		0x5006 0800 – 0x5006 0BFF	TRNG
		0x5006 0400 – 0x5006 07FF	Reserved
		0x5006 0000 – 0x5006 03FF	CAU
		0x5005 0400 – 0x5005 FFFF	Reserved
		0x5005 0000 – 0x5005 03FF	Reserved
		0x5004 0000 – 0x5004 FFFF	Reserved
		0x5000 0000 – 0x5003 FFFF	Reserved
	AHB2	0x4800 1800 – 0x4FFF FFFF	Reserved
		0x4800 1400 – 0x4800 17FF	GPIOF
		0x4800 1000 – 0x4800 13FF	Reserved
		0x4800 0C00 – 0x4800 0FFF	GPIOD
		0x4800 0800 – 0x4800 0BFF	GPIOC
		0x4800 0400 – 0x4800 07FF	GPIOB
		0x4800 0000 – 0x4800 03FF	GPIOA
	AHB1	0x4002 4400 – 0x47FF FFFF	Reserved
		0x4002 4000 – 0x4002 43FF	Reserved
		0x4002 3400 – 0x4002 3FFF	Reserved
		0x4002 3000 – 0x4002 33FF	CRC
		0x4002 2400 – 0x4002 2FFF	Reserved
		0x4002 2000 – 0x4002 23FF	FMC
		0x4002 1400 – 0x4002 1FFF	Reserved
		0x4002 1000 – 0x4002 13FF	RCU
		0x4002 0C00 – 0x4002 0FFF	Reserved
		0x4002 0800 – 0x4002 0BFF	DMAMUX
		0x4002 0400 – 0x4002 07FF	Reserved
		0x4002 0000 – 0x4002 03FF	DMA
	APB2	0x4001 8000 – 0x4001 FFFF	Reserved
		0x4001 D000 – 0x4001 D3FF	TIMER40
		0x4001 8000 – 0x4001 CFFF	Reserved
		0x4001 7C00 – 0x4001 7FFF	CMP
		0x4001 5C00 – 0x4001 7BFF	Reserved
		0x4001 5800 – 0x4001 5BFF	DBG
		0x4001 5000 – 0x4001 57FF	Reserved

Pre-defined Regions	Bus	ADDRESS	Peripherals
		0x4001 4C00 – 0x4001 4FFF	TIMER8
		0x4001 4400 – 0x4001 4BFF	Reserved
		0x4001 4000 – 0x4001 43FF	TIMER14
		0x4001 3C00 – 0x4001 3FFF	Reserved
		0x4001 3800 – 0x4001 3BFF	USART0
		0x4001 3400 – 0x4001 37FF	Reserved
		0x4001 3000 – 0x4001 33FF	SPI0
		0x4001 2C00 – 0x4001 2FFF	TIMER0
		0x4001 2800 – 0x4001 2BFF	Reserved
		0x4001 2400 – 0x4001 27FF	ADC
		0x4001 0800 – 0x4001 23FF	Reserved
		0x4001 0400 – 0x4001 07FF	EXTI
		0x4001 0000 – 0x4001 03FF	SYSCFG + VREF
	APB1	0x4000 CC00 – 0x4000 FFFF	Reserved
		0x4000 C800 – 0x4000 CBFF	CTC
		0x4000 C400 – 0x4000 C7FF	Reserved
		0x4000 C000 – 0x4000 C3FF	I2C2
		0x4000 9800 – 0x4000 BFFF	Reserved
		0x4000 9400 – 0x4000 97FF	LPTIMER0
		0x4000 8400 – 0x4000 93FF	Reserved
		0x4000 8000 – 0x4000 83FF	LPUART0
		0x4000 7C00 – 0x4000 7FFF	LPTIMER1
		0x4000 7800 – 0x4000 7BFF	Reserved
		0x4000 7400 – 0x4000 77FF	DAC0
		0x4000 7000 – 0x4000 73FF	PMU
		0x4000 6800 – 0x4000 6FFF	Reserved
		0x4000 6400 – 0x4000 67FF	CAN
		0x4000 6000 – 0x4000 63FF	Shared USBD/CAN RAM (512 bytes)
		0x4000 5C00 – 0x4000 5FFF	USBD
		0x4000 5800 – 0x4000 5BFF	I2C1
		0x4000 5400 – 0x4000 57FF	I2C0
		0x4000 5000 – 0x4000 53FF	UART4
		0x4000 4C00 – 0x4000 4FFF	UART3
		0x4000 4800 – 0x4000 4BFF	LPUART1
		0x4000 4400 – 0x4000 47FF	USART1
		0x4000 4000 – 0x4000 43FF	Reserved
		0x4000 3C00 – 0x4000 3FFF	Reserved
		0x4000 3800 – 0x4000 3BFF	SPI1/I2S1
		0x4000 3400 – 0x4000 37FF	Reserved
		0x4000 3000 – 0x4000 33FF	FWDGT
		0x4000 2C00 – 0x4000 2FFF	WWDGT

Pre-defined Regions	Bus	ADDRESS	Peripherals
		0x4000 2800 – 0x4000 2BFF	RTC
		0x4000 2400 – 0x4000 27FF	SLCD
		0x4000 2000 – 0x4000 23FF	Reserved
		0x4000 1C00 – 0x4000 1FFF	Reserved
		0x4000 1800 – 0x4000 1BFF	TIMER11
		0x4000 1400 – 0x4000 17FF	TIMER6
		0x4000 1000 – 0x4000 13FF	TIMER5
		0x4000 0800 – 0x4000 0FFF	Reserved
		0x4000 0400 – 0x4000 07FF	TIMER2
		0x4000 0000 – 0x4000 03FF	TIMER1
		0x4000 0000 – 0x4000 03FF	Reserved
SRAM		0x2000 8000 – 0x3FFF FFFF	Reserved
		0x2000 6000 – 0x2000 7FFF	Reserved
		0x2000 4000 – 0x2000 5FFF	SRAM1(16KB)
		0x2000 2000 – 0x2000 3FFF	
		0x2000 1000 – 0x2000 1FFF	SRAM0(8KB)
		0x2000 0000 – 0x2000 0FFF	
Code		0x1FFF F810 – 0x1FFF FFFF	Reserved
		0x1FFF F800 – 0x1FFF F80F	Option bytes(16B)
		0x1FFF D000- 0x1FFF F7FF	System memory(10KB)
		0x1FFF 7200 – 0x1FFF CFFF	Reserved
		0x1FFF 7000 – 0x1FFF 71FF	OTP(512B)
		0x1000 0000 – 0x1FFF 6FFF	Reserved
		0x0804 0000 – 0x0FFF FFFF	Reserved
		0x0802 0000 – 0x0803 FFFF	Reserved
		0x0801 0000 – 0x0801 FFFF	Main Flash memory(128KB)
		0x0800 0000 – 0x0800 FFFF	
		0x0004 0000 – 0x07FF FFFF	Reserved
		0x0001 0000 – 0x0003 FFFF	Aliased to Flash or system memory
		0x0000 0000 – 0x0000 FFFF	

2.5. Clock tree

Figure 2-10. GD32L235xx clock tree



Note:

The TIMERs are clocked by the clock divided from CK_APB2 and CK_APB1. The frequency of TIMERs clock is equal to CK_APBx (APB prescaler is 1), twice the CK_APBx (APB prescaler is not 1).

Legend:

HXTAL: High speed crystal oscillator

LXTAL: Low speed crystal oscillator

IRC16M: Internal 16M RC oscillator

IRC48M: Internal 48M RC oscillator

IRC32K: Internal 32K RC oscillator

2.6. Pin definitions

2.6.1. GD32L235Rx LQFP64 pin definitions

Table 2-4. GD32L235Rx LQFP64 pin definitions

GD32L235Rx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PD6	1	I/O	-	Default: PD6 Alternate: LPTIMER0_IN1, LPTIMER1_OUT, USART1_RX, EVENTOUT, SPI0_MOSI Additional: VSLCD
VBAT	2	P	-	Default: VBAT
PC13-TAMPER-RTC	3	I/O	-	Default: PC13 Alternate: TIMER0_BRKIN, EVENTOUT Additional: RTC_TAMP0, RTC_OUT, RTC_TS, WKUP1
PC14-OSC32IN	4	I/O	-	Default: PC14 Alternate: TIMER0_BRKIN, EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	5	I/O	-	Default: PC15 Alternate: TIMER14_BRKIN, EVENTOUT Additional: OSC32OUT
OSCIN	6	I/O	-	Default: OSCIN Alternate: EVENTOUT, SPI1_NSS, I2S1_WS, CK_OUT, LPTIMER1_OUT, TIMER8_CH0, TIMER0_CH0 Additional: PF0
OSCOUT	7	I/O	-	Default: OSCOUT Alternate: EVENTOUT, SPI1_SCK, I2S1_CK, TIMER14_CH0_ON Additional: PF1
NRST	8	I/O	-	Default: NRST
PC0	9	I/O	5VT	Default: PC0 Alternate: SEG18, I2C2_SCL, LPUART0_RX, LPTIMER0_IN0, LPTIMER1_IN0, LPUART1_TX, EVENTOUT Additional: ADC_IN10
PC1	10	I/O	5VT	Default: PC1 Alternate: SEG19, I2C2_SDA, LPUART0_TX, EVENTOUT, LPTIMER0_OUT, LPUART1_RX, TIMER14_CH0, LPTIMER1_IN1 Additional: ADC_IN11
PC2	11	I/O	5VT	Default: PC2 Alternate: SPI1_MISO, I2S1_MCK, SEG20, EVENTOUT, LPTIMER0_IN1, TIMER14_CH1 Additional: ADC_IN12
PC3	12	I/O	5VT	Default: PC3

GD32L235Rx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: SPI1_MOSI, I2S1_SD, SEG21, LPTIMER0_ETI0, EVENTOUT, LPTIMER1_ETI0 Additional: ADC_IN13
VSS	13	P	-	Default: VSS
VREFP	14	P	-	Default: VREFP
VDD	15	P	-	Default: VDD
PA0	16	I/O	5VT	Default: PA0 Alternate: USART1_CTS, TIMER1_CH0, TIMER1_ETI, CMP0_OUT, EVENTOUT, UART3_TX, SPI1_SCK, I2S1_CK, LPTIMER0_OUT, CAN_RX Additional: WKUP0, ADC_IN0, RTC_TAMP1, CMP0_IM4
PA1	17	I/O	5VT	Default: PA1 Alternate: USART1_RTS, USART1_DE, TIMER1_CH1, I2C0_SMBA, SPI0_SCK, SEG0, EVENTOUT, UART3_RX, TIMER14_CH0_ON, CAN_TX Additional: ADC_IN1, CMP0_IP
PA2	18	I/O	5VT	Default: PA2 Alternate: USART1_TX, TIMER8_CH0, TIMER1_CH2, SPI0_IO2, CMP1_OUT, LPUART0_TX, SEG1, EVENTOUT, SPI0_MOSI, TIMER14_CH0 Additional: ADC_IN2, CMP1_IM4, RTC_TAMP2, WKUP2
PA3	19	I/O	5VT	Default: PA3 Alternate: USART1_RX, TIMER1_CH3, TIMER8_CH1, SPI0_IO3, LPUART0_RX, SEG2, EVENTOUT, SPI1_MISO, I2S1_MCK, TIMER14_CH1 Additional: ADC_IN3, CMP1_IP0
PD8	20	I/O	5VT	Default: PD8 Alternate: LPTIMER0_ETI0, LPUART0_TX, EVENTOUT, SEG30, LPTIMER0_OUT, SPI0_SCK
PD9	21	I/O	5VT	Default: PD9 Alternate: LPTIMER0_IN0, LPUART0_RX, EVENTOUT, SEG31, TIMER0_BRKIN, SPI0_NSS
PA4	22	I/O		Default: PA4 Alternate: SPI0_NSS, USART1_CK, SPI1_NSS, I2S1_WS, LPTIMER0_OUT, EVENTOUT, SPI1_MOSI, I2S1_SD, LPTIMER1_OUT, TIMER8_CH0, TIMER40_CH1(3), CAN_RX Additional: ADC_IN4, DAC0_OUT0
PA5	23	I/O	5VT	Default: PA5 Alternate: SPI0_SCK, TIMER1_CH0, TIMER1_ETI, LPTIMER0_ETI0, EVENTOUT, TIMER40_CH0(3), LPTIMER1_ETI0, CAN_TX Additional: ADC_IN5
PA6	24	I/O	5VT	Default: PA6

GD32L235Rx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: SPI0_MISO, TIMER2_CH0, LPTIMER0_IN0, CMP0_OUT, LPUART0_CTS, SEG3, EVENTOUT, TIMER0_BRKIN, I2C2_SDA, TIMER11_CH0, TIMER40_CH0(3), I2C1_SDA Additional: ADC_IN6
PA7	25	I/O	5VT	Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, LPTIMER0_ETI0, I2C2_SCL, CMP1_OUT, SEG4, EVENTOUT, TIMER0_CH0_ON, TIMER11_CH1, TIMER11_CH0, TIMER8_CH0, I2C1_SCL Additional: ADC_IN7
PC4	26	I/O	5VT	Default: PC4 Alternate: LPUART0_TX, USART0_TX, TIMER1_CH0, TIMER1_ETI, SEG22, EVENTOUT, CAN_RX Additional: ADC_IN14
PC5	27	I/O	5VT	Default: PC5 Alternate: LPUART0_RX, USART0_RX, TIMER1_CH1, SEG23, EVENTOUT, CAN_TX Additional: ADC_IN15
PB0	28	I/O	5VT	Default: PB0 Alternate: TIMER2_CH2, LPTIMER0_OUT, SPI0_NSS, CMP0_OUT, SEG5, EVENTOUT, UART4_TX(3), LPUART1_CTS, TIMER0_CH1_ON, LPTIMER1_IN1 Additional: ADC_IN8, VREF_OUT
PB1	29	I/O	5VT	Default: PB1 Alternate: TIMER2_CH3, LPUART0_RTS, LPUART0_DE, LPTIMER0_IN0, SEG6, EVENTOUT, UART4_RX(3), LPUART1_RTS, LPUART1_DE, LPTIMER1_IN0, TIMER0_CH2_ON, TIMER8_CH0 Additional: ADC_IN9, VREF_OUT
BOOT1-PB2	30	I/O	5VT	Default: BOOT1, PB2 Alternate: LPTIMER0_OUT, EVENTOUT, RTC_OUT, I2C2_SMBA Additional: PB2, WKUP3
PB10	31	I/O	5VT	Default: PB10 Alternate: SPI1_SCK, I2S1_CK, LPUART0_TX, I2C1_SCL, LPUART0_RX, TIMER1_CH2, CMP0_OUT, SEG10, EVENTOUT
PB11	32	I/O	5VT	Default: PB11 Alternate: LPUART0_RX, I2C1_SDA, LPUART0_TX, TIMER1_CH3, CMP1_OUT, SEG11, EVENTOUT, SPI1_MOSI, I2S1_SD
PB12	33	I/O	5VT	Default: PB12 Alternate: SPI1_NSS, I2S1_WS, I2C1_SMBA, LPUART0_RTS, LPUART0_DE, SEG12, EVENTOUT, TIMER0_BRKIN, TIMER14_BRKIN

GD32L235Rx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PB13	34	I/O	5VT	Default: PB13 Alternate: CK_OUT, SPI1_SCK, I2S1_CK, LPUART0_CTS, I2C1_SCL, SEG13, EVENTOUT, TIMER8_CH0, TIMER0_CH0_ON, TIMER14_CH0_ON
PB14	35	I/O	5VT	Default: PB14 Alternate: SPI1_MISO, LPUART0_RTS, LPUART0_DE, I2C1_SDA, TIMER11_CH0, SEG14, EVENTOUT, RTC_OUT, TIMER8_CH1, TIMER0_CH1_ON, TIMER14_CH0
PB15	36	I/O	5VT	Default: PB15 Alternate: SPI1_MOSI, I2S1_SD, TIMER11_CH1, SEG15, EVENTOUT, TIMER0_CH2_ON, TIMER14_CH0_ON, TIMER14_CH1 Additional: RTC_REFIN
PC6	37	I/O	5VT	Default: PC6 Alternate: I2S1_MCK, TIMER2_CH0, SEG24, EVENTOUT, TIMER11_CH0, LPUART1_TX, TIMER1_CH2 Additional: WKUP4
PC7	38	I/O	5VT	Default: PC7 Alternate: TIMER2_CH1, SEG25, EVENTOUT, TIMER11_CH1, LPUART1_RX, TIMER1_CH3
PC8	39	I/O	5VT	Default: PC8 Alternate: TIMER2_CH2, I2C2_SDA, SEG26, EVENTOUT, TIMER0_CH0, LPUART1_CTS
PC9	40	I/O	5VT	Default: PC9 Alternate: TIMER2_CH3, I2C2_SCL, SEG27, EVENTOUT, TIMER0_CH1, I2C2_SDA, LPUART1_RTS, LPUART1_DE
PA8	41	I/O	5VT	Default: PA8 Alternate: USART0_CK, CK_OUT, LPTIMER0_OUT, I2C2_SMBA, COM0, EVENTOUT, CTC_SYNC, TIMER0_CH0, SPI1_NSS, I2S1_WS, LPTIMER1_OUT, I2C1_SMBA, I2C2_SCL
PA9	42	I/O	5VT	Default: PA9 Alternate: CK_OUT, USART0_TX, I2C0_SCL, COM1, EVENTOUT, LPTIMER0_IN1, TIMER0_CH1, SPI1_MISO, TIMER14_BRKIN, I2C1_SCL, I2C2_SMBA
PA10	43	I/O	5VT	Default: PA10 Alternate: USART0_RX, I2C0_SDA, COM2, EVENTOUT, TIMER0_CH2, I2C1_SDA, SPI1_MOSI, I2S1_SD
PA11	44	I/O	5VT	Default: PA11 Alternate: CMP0_OUT, USART0_CTS, SPI0_MISO, EVENTOUT, TIMER0_CH3, TIMER0_BRKIN, I2C1_SCL, CAN_RX, LPUART1_RTS, LPUART1_DE Additional: USBDM

GD32L235Rx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PA12	45	I/O	5VT	Default: PA12 Alternate: CMP1_OUT, USART0_RTS, USART0_DE, SPI0_MOSI, EVENTOUT, TIMER0_ETI, I2C1_SDA, CAN_TX, LPUART1_CTS Additional: USBDP
PA13	46	I/O	5VT	Default: SWDIO Alternate: LPUART0_RX, I2C0_SCL, USART0_TX, SPI0_IO2, SPI0_NSS, EVENTOUT, LPUART1_RX Additional: PA13
PD0	47	I/O	5VT	Default: PD0 Alternate: SPI1_NSS, I2S1_WS, LPTIMER0_OUT, USART1_CK, EVENTOUT, CTC_SYNC, TIMER8_CH0, CAN_RX
PD1	48	I/O	5VT	Default: PD1 Alternate: SPI1_SCK, I2S1_CK, SPI1_MISO, USART1_CTS, EVENTOUT, CAN_TX, TIMER11_CH0, TIMER40_CH1(3)
PA14	49	I/O	5VT	Default: SWCLK Alternate: LPUART0_TX, USART1_TX, I2C0_SDA, USART0_RX, SPI0_IO3, SPI1_NSS, I2S1_WS, EVENTOUT, LPUART1_TX Additional: PA14
PA15	50	I/O	5VT	Default: PA15 Alternate: SPI1_NSS, I2S1_WS, TIMER1_CH0, TIMER1_ETI, SPI0_NSS, USART1_RX, SEG17, EVENTOUT, I2C1_SMBA
PC10	51	I/O	5VT	Default: PC10 Alternate: UART3_TX, LPUART0_TX, SPI1_SCK, I2S1_CK, SEG28, COM4, EVENTOUT, TIMER0_CH2
PC11	52	I/O	5VT	Default: PC11 Alternate: UART3_RX, LPUART0_RX, SPI1_MISO, SEG29, COM5, EVENTOUT, TIMER0_CH3
PC12	53	I/O	5VT	Default: PC12 Alternate: UART4_TX(3), SPI1_MOSI, I2S1_SD, SEG30, COM6, EVENTOUT, LPTIMER0_IN0, TIMER8_CH0
PD2	54	I/O	5VT	Default: PD2 Alternate: LPUART0_RTS, LPUART0_DE, TIMER2_ETI, UART4_RX(3), SEG31, COM7, EVENTOUT, TIMER0_CH0_ON
PB3	55	I/O	5VT	Default: PB3 Alternate: UART4_TX(3), SPI1_SCK, I2S1_CK, TIMER1_CH1, SPI0_SCK, USART0_RTS, USART0_DE, SEG7, EVENTOUT, LPTIMER0_IN1, I2C2_SCL, I2C1_SCL, TIMER0_CH1 Additional: CMP1_IM6

GD32L235Rx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PB4	56	I/O	5VT	Default: PB4 Alternate: UART4_RX(3), SPI1_MISO, TIMER2_CH0, SPI0_MISO, USART0_CTS, SEG8, EVENTOUT, I2C2_SDA, I2C1_SDA, TIMER11_CH0 Additional: CMP1_IP1
PB5	57	I/O	5VT	Default: PB5 Alternate: LPTIMER0_IN0, I2C0_SMBA, SPI1_MOSI, I2S1_SD, SPI0_MOSI, USART0_CK, CMP1_OUT, SEG9, EVENTOUT, TIMER40_BRKIN(3), TIMER2_CH1 Additional: CMP1_IP2, WKUP4
PB6	58	I/O	5VT	Default: PB6 Alternate: LPTIMER0_ETI0, I2C1_SCL, I2C0_SCL, USART0_TX, SPI0_IO2, EVENTOUT, SPI1_MISO, TIMER0_CH2, TIMER40_CH0_ON(3), LPUART1_RX Additional: CMP1_IP3
PB7	59	I/O	5VT	Default: PB7 Alternate: I2C1_SDA, I2C0_SDA, USART0_RX, SPI0_IO3, EVENTOUT, SPI1_MOSI, I2S1_SD, LPTIMER0_IN1, LPUART1_TX, CK_OUT Additional: CMP1_IP4
BOOT0-PD3	60	I/O	5VT	Default: BOOT0 Alternate: USART1_CTS, SPI1_MISO, I2S1_MCK, TIMER0_CH1_ON, UART4_RX(3), EVENTOUT Additional: PD3
PB8	61	I/O	5VT	Default: PB8 Alternate: I2C1_SCL, I2C0_SCL, CMP0_OUT, SEG16, EVENTOUT, SPI1_SCK, I2S1_CK, TIMER14_BRKIN, CAN_RX, TIMER40_CH0(3)
PB9	62	I/O	5VT	Default: PB9 Alternate: I2C1_SDA, SPI1_NSS, I2S1_WS, I2C0_SDA, CMP1_OUT, COM3, EVENTOUT, CAN_TX, TIMER11_CH0, TIMER40_CH1(3)
PD4	63	I/O	5VT	Default: PD4 Alternate: SPI1_MOSI, I2S1_SD, USART1_RTS, USART1_DE, EVENTOUT, SEG28, TIMER0_CH2_ON
PD5	64	I/O	5VT	Default: PD5 Alternate: USART1_TX, EVENTOUT, SPI0_MISO, SEG29, TIMER0_BRKIN

Note:

(1) Type: I = input, O = output, A = analog, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Functions are available on GD32L235RB devices only.

2.6.2. GD32L235Rx QFN64 pin definitions

Table 2-5. GD32L235Rx QFN64 pin definitions

GD32L235Rx QFN64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PD6	1	I/O	-	Default: PD6 Alternate: LPTIMER0_IN1, LPTIMER1_OUT, USART1_RX, EVENTOUT, SPI0_MOSI Additional: VSLCD
VBAT	2	P	-	Default: VBAT
PC13-TAMPER-RTC	3	I/O	-	Default: PC13 Alternate: TIMER0_BRKIN, EVENTOUT Additional: RTC_TAMP0, RTC_OUT, RTC_TS, WKUP1
PC14-OSC32IN	4	I/O	-	Default: PC14 Alternate: TIMER0_BRKIN, EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	5	I/O	-	Default: PC15 Alternate: TIMER14_BRKIN, EVENTOUT Additional: OSC32OUT
OSCIN	6	I/O	-	Default: OSCIN Alternate: EVENTOUT, SPI1_NSS, I2S1_WS, CK_OUT, LPTIMER1_OUT, TIMER8_CH0, TIMER0_CH0 Additional: PF0
OSCOUT	7	I/O	-	Default: OSCOUT Alternate: EVENTOUT, SPI1_SCK, I2S1_CK, TIMER14_CH0_ON Additional: PF1
NRST	8	I/O	-	Default: NRST
PC0	9	I/O	5VT	Default: PC0 Alternate: SEG18, I2C2_SCL, LPUART0_RX, LPTIMER0_IN0, LPTIMER1_IN0, LPUART1_TX, EVENTOUT Additional: ADC_IN10
PC1	10	I/O	5VT	Default: PC1 Alternate: SEG19, I2C2_SDA, LPUART0_TX, EVENTOUT, LPTIMER0_OUT, LPUART1_RX, TIMER14_CH0, LPTIMER1_IN1 Additional: ADC_IN11
PC2	11	I/O	5VT	Default: PC2 Alternate: SPI1_MISO, I2S1_MCK, SEG20, EVENTOUT, LPTIMER0_IN1, TIMER14_CH1 Additional: ADC_IN12
PC3	12	I/O	5VT	Default: PC3 Alternate: SPI1_MOSI, I2S1_SD, SEG21, LPTIMER0_ETI0, EVENTOUT, LPTIMER1_ETI0 Additional: ADC_IN13

GD32L235Rx QFN64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
VSS	13	P	-	Default: VSS
VREFP	14	P	-	Default: VREFP
VDD	15	P	-	Default: VDD
PA0	16	I/O	5VT	Default: PA0 Alternate: USART1_CTS, TIMER1_CH0, TIMER1_ETI, CMP0_OUT, EVENTOUT, UART3_TX, SPI1_SCK, I2S1_CK, LPTIMER0_OUT, CAN_RX Additional: WKUP0, ADC_IN0, RTC_TAMP1, CMP0_IM4
PA1	17	I/O	5VT	Default: PA1 Alternate: USART1_RTS, USART1_DE, TIMER1_CH1, I2C0_SMBA, SPI0_SCK, SEG0, EVENTOUT, UART3_RX, TIMER14_CH0_ON, CAN_TX Additional: ADC_IN1, CMP0_IP
PA2	18	I/O	5VT	Default: PA2 Alternate: USART1_TX, TIMER8_CH0, TIMER1_CH2, SPI0_IO2, CMP1_OUT, LPUART0_TX, SEG1, EVENTOUT, SPI0_MOSI, TIMER14_CH0 Additional: ADC_IN2, CMP1_IM4, RTC_TAMP2, WKUP2
PA3	19	I/O	5VT	Default: PA3 Alternate: USART1_RX, TIMER1_CH3, TIMER8_CH1, SPI0_IO3, LPUART0_RX, SEG2, EVENTOUT, SPI1_MISO, I2S1_MCK, TIMER14_CH1 Additional: ADC_IN3, CMP1_IP0
PD8	20	I/O	5VT	Default: PD8 Alternate: LPTIMER0_ETI0, LPUART0_TX, EVENTOUT, SEG30, LPTIMER0_OUT, SPI0_SCK
PD9	21	I/O	5VT	Default: PD9 Alternate: LPTIMER0_IN0, LPUART0_RX, EVENTOUT, SEG31, TIMER0_BRKIN, SPI0_NSS
PA4	22	I/O		Default: PA4 Alternate: SPI0_NSS, USART1_CK, SPI1_NSS, I2S1_WS, LPTIMER0_OUT, EVENTOUT, SPI1_MOSI, I2S1_SD, LPTIMER1_OUT, TIMER8_CH0, TIMER40_CH1(3), CAN_RX Additional: ADC_IN4, DAC0_OUT0
PA5	23	I/O	5VT	Default: PA5 Alternate: SPI0_SCK, TIMER1_CH0, TIMER1_ETI, LPTIMER0_ETI0, EVENTOUT, TIMER40_CH0(3), LPTIMER1_ETI0, CAN_TX Additional: ADC_IN5
PA6	24	I/O	5VT	Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, LPTIMER0_IN0, CMP0_OUT, LPUART0_CTS, SEG3, EVENTOUT, TIMER0_BRKIN, I2C2_SDA, TIMER11_CH0, TIMER

GD32L235Rx QFN64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				40_CH0(3), I2C1_SDA Additional: ADC_IN6
PA7	25	I/O	5VT	Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, LPTIMER0_ETI0, I2C2_SCL, CMP1_OUT, SEG4, EVENTOUT, TIMER0_CH0_ON, TIMER11_CH1, TIMER11_CH0, TIMER8_CH0, I2C1_SCL Additional: ADC_IN7
PC4	26	I/O	5VT	Default: PC4 Alternate: LPUART0_TX, USART0_TX, TIMER1_CH0, TIMER1_ETI, SEG22, EVENTOUT, CAN_RX Additional: ADC_IN14
PC5	27	I/O	5VT	Default: PC5 Alternate: LPUART0_RX, USART0_RX, TIMER1_CH1, SEG23, EVENTOUT, CAN_TX Additional: ADC_IN15
PB0	28	I/O	5VT	Default: PB0 Alternate: TIMER2_CH2, LPTIMER0_OUT, SPI0_NSS, CMP0_OUT, SEG5, EVENTOUT, UART4_TX(3), LPUART1_CTS, TIMER0_CH1_ON, LPTIMER1_IN1 Additional: ADC_IN8, VREF_OUT
PB1	29	I/O	5VT	Default: PB1 Alternate: TIMER2_CH3, LPUART0_RTS, LPUART0_DE, LPTIMER0_IN0, SEG6, EVENTOUT, UART4_RX(3), LPUART1_RTS, LPUART1_DE, LPTIMER1_IN0, TIMER0_CH2_ON, TIMER8_CH0 Additional: ADC_IN9, VREF_OUT
BOOT1-PB2	30	I/O	5VT	Default: BOOT1, PB2 Alternate: LPTIMER0_OUT, EVENTOUT, RTC_OUT, I2C2_SMBA Additional: PB2, WKUP3
PB10	31	I/O	5VT	Default: PB10 Alternate: SPI1_SCK, I2S1_CK, LPUART0_TX, I2C1_SCL, LPUART0_RX, TIMER1_CH2, CMP0_OUT, SEG10, EVENTOUT
PB11	32	I/O	5VT	Default: PB11 Alternate: LPUART0_RX, I2C1_SDA, LPUART0_TX, TIMER1_CH3, CMP1_OUT, SEG11, EVENTOUT, SPI1_MOSI, I2S1_SD
PB12	33	I/O	5VT	Default: PB12 Alternate: SPI1_NSS, I2S1_WS, I2C1_SMBA, LPUART0_RTS, LPUART0_DE, SEG12, EVENTOUT, TIMER0_BRKIN, TIMER14_BRKIN
PB13	34	I/O	5VT	Default: PB13 Alternate: CK_OUT, SPI1_SCK, I2S1_CK, LPUART0_CTS, I2C1_SCL, SEG13, EVENTOUT, TIMER8_C

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Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
				H0, TIMER0_CH0_ON, TIMER14_CH0_ON
PB14	35	I/O	5VT	Default: PB14 Alternate: SPI1_MISO, LPUART0_RTS, LPUART0_DE, I2C1_SDA, TIMER11_CH0, SEG14, EVENTOUT, RTC_OUT, TIMER8_CH1, TIMER0_CH1_ON, TIMER14_CH0
PB15	36	I/O	5VT	Default: PB15 Alternate: SPI1_MOSI, I2S1_SD, TIMER11_CH1, SEG15, EVENTOUT, TIMER0_CH2_ON, TIMER14_CH0_ON, TIMER14_CH1 Additional: RTC_REFIN
PC6	37	I/O	5VT	Default: PC6 Alternate: I2S1_MCK, TIMER2_CH0, SEG24, EVENTOUT, TIMER11_CH0, LPUART1_TX, TIMER1_CH2 Additional: WKUP4
PC7	38	I/O	5VT	Default: PC7 Alternate: TIMER2_CH1, SEG25, EVENTOUT, TIMER11_CH1, LPUART1_RX, TIMER1_CH3
PC8	39	I/O	5VT	Default: PC8 Alternate: TIMER2_CH2, I2C2_SDA, SEG26, EVENTOUT, TIMER0_CH0, LPUART1_CTS
PC9	40	I/O	5VT	Default: PC9 Alternate: TIMER2_CH3, I2C2_SCL, SEG27, EVENTOUT, TIMER0_CH1, I2C2_SDA, LPUART1_RTS, LPUART1_DE
PA8	41	I/O	5VT	Default: PA8 Alternate: USART0_CK, CK_OUT, LPTIMER0_OUT, I2C2_SMBA, COM0, EVENTOUT, CTC_SYNC, TIMER0_CH0, SPI1_NSS, I2S1_WS, LPTIMER1_OUT, I2C1_SMBA, I2C2_SCL
PA9	42	I/O	5VT	Default: PA9 Alternate: CK_OUT, USART0_TX, I2C0_SCL, COM1, EVENTOUT, LPTIMER0_IN1, TIMER0_CH1, SPI1_MISO, TIMER14_BRKIN, I2C1_SCL, I2C2_SMBA
PA10	43	I/O	5VT	Default: PA10 Alternate: USART0_RX, I2C0_SDA, COM2, EVENTOUT, TIMER0_CH2, I2C1_SDA, SPI1_MOSI, I2S1_SD
PA11	44	I/O	5VT	Default: PA11 Alternate: CMP0_OUT, USART0_CTS, SPI0_MISO, EVENTOUT, TIMER0_CH3, TIMER0_BRKIN, I2C1_SCL, CAN_RX, LPUART1_RTS, LPUART1_DE Additional: USBDM
PA12	45	I/O	5VT	Default: PA12 Alternate: CMP1_OUT, USART0_RTS, USART0_DE, SPI0_MOSI, EVENTOUT, TIMER0_ETI, I2C1_SDA,

GD32L235Rx QFN64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				CAN_TX, LPUART1_CTS Additional: USBDP
PA13	46	I/O	5VT	Default: SWDIO Alternate: LPUART0_RX, I2C0_SCL, USART0_TX, SPI0_IO2, SPI0_NSS, EVENTOUT, LPUART1_RX Additional: PA13
PD0	47	I/O	5VT	Default: PD0 Alternate: SPI1_NSS, I2S1_WS, LPTIMER0_OUT, USART1_CK, EVENTOUT, CTC_SYNC, TIMER8_CH0, CAN_RX
PD1	48	I/O	5VT	Default: PD1 Alternate: SPI1_SCK, I2S1_CK, SPI1_MISO, USART1_CTS, EVENTOUT, CAN_TX, TIMER11_CH0, TIMER40_CH1(3)
PA14	49	I/O	5VT	Default: SWCLK Alternate: LPUART0_TX, USART1_TX, I2C0_SDA, USART0_RX, SPI0_IO3, SPI1_NSS, I2S1_WS, EVENTOUT, LPUART1_TX Additional: PA14
PA15	50	I/O	5VT	Default: PA15 Alternate: SPI1_NSS, I2S1_WS, TIMER1_CH0, TIMER1_ETI, SPI0_NSS, USART1_RX, SEG17, EVENTOUT, I2C1_SMBA
PC10	51	I/O	5VT	Default: PC10 Alternate: UART3_TX, LPUART0_TX, SPI1_SCK, I2S1_CK, SEG28, COM4, EVENTOUT, TIMER0_CH2
PC11	52	I/O	5VT	Default: PC11 Alternate: UART3_RX, LPUART0_RX, SPI1_MISO, SEG29, COM5, EVENTOUT, TIMER0_CH3
PC12	53	I/O	5VT	Default: PC12 Alternate: UART4_TX(3), SPI1_MOSI, I2S1_SD, SEG30, COM6, EVENTOUT, LPTIMER0_IN0, TIMER8_CH0
PD2	54	I/O	5VT	Default: PD2 Alternate: LPUART0_RTS, LPUART0_DE, TIMER2_ETI, UART4_RX(3), SEG31, COM7, EVENTOUT, TIMER0_CH0_ON
PB3	55	I/O	5VT	Default: PB3 Alternate: UART4_TX(3), SPI1_SCK, I2S1_CK, TIMER1_CH1, SPI0_SCK, USART0_RTS, USART0_DE, SEG7, EVENTOUT, LPTIMER0_IN1, I2C2_SCL, I2C1_SCL, TIMER0_CH1 Additional: CMP1_IM6
PB4	56	I/O	5VT	Default: PB4 Alternate: UART4_RX(3), SPI1_MISO, TIMER2_CH0, SPI0_MISO, USART0_CTS, SEG8, EVENTOUT, I2

GD32L235Rx QFN64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				C2_SDA, I2C1_SDA, TIMER11_CH0 Additional: CMP1_IP1
PB5	57	I/O	5VT	Default: PB5 Alternate: LPTIMER0_IN0, I2C0_SMBA, SPI1_MOSI, I2S1_SD, SPI0_MOSI, USART0_CK, CMP1_OUT, SEG9, EVENTOUT, TIMER40_BRKIN(3), TIMER2_CH1 Additional: CMP1_IP2, WKUP4
PB6	58	I/O	5VT	Default: PB6 Alternate: LPTIMER0_ETI0, I2C1_SCL, I2C0_SCL, USART0_TX, SPI0_IO2, EVENTOUT, SPI1_MISO, TIMER0_CH2, TIMER40_CH0_ON(3), LPUART1_RX Additional: CMP1_IP3
PB7	59	I/O	5VT	Default: PB7 Alternate: I2C1_SDA, I2C0_SDA, USART0_RX, SPI0_IO3, EVENTOUT, SPI1_MOSI, I2S1_SD, LPTIMER0_IN1, LPUART1_TX, CK_OUT Additional: CMP1_IP4
BOOT0-PD3	60	I/O	5VT	Default: BOOT0 Alternate: USART1_CTS, SPI1_MISO, I2S1_MCK, TIMER0_CH1_ON, UART4_RX(3), EVENTOUT Additional: PD3
PB8	61	I/O	5VT	Default: PB8 Alternate: I2C1_SCL, I2C0_SCL, CMP0_OUT, SEG16, EVENTOUT, SPI1_SCK, I2S1_CK, TIMER14_BRKIN, CAN_RX, TIMER40_CH0(3)
PB9	62	I/O	5VT	Default: PB9 Alternate: I2C1_SDA, SPI1_NSS, I2S1_WS, I2C0_SDA, CMP1_OUT, COM3, EVENTOUT, CAN_TX, TIMER11_CH0, TIMER40_CH1(3)
PD4	63	I/O	5VT	Default: PD4 Alternate: SPI1_MOSI, I2S1_SD, USART1_RTS, USART1_DE, EVENTOUT, SEG28, TIMER0_CH2_ON
PD5	64	I/O	5VT	Default: PD5 Alternate: USART1_TX, EVENTOUT, SPI0_MISO, SEG29, TIMER0_BRKIN

Note:

(1) Type: I = input, O = output, A = analog, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Functions are available on GD32L235RB devices only.

2.6.3. GD32L235Cx LQFP48 pin definitions

Table 2-6. GD32L235Cx LQFP48 pin definitions

GD32L235Cx LQFP48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
VBAT	1	P	-	Default: VBAT
PC13-TAMPER-RTC	2	I/O		Default: PC13 Alternate: TIMER0_BRKIN, EVENTOUT Additional: RTC_TAMP0, RTC_OUT, RTC_TS, WKUP1
PC14-OSC32IN	3	I/O		Default: PC14 Alternate: TIMER0_BRKIN, EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	4	I/O		Default: PC15 Alternate: TIMER14_BRKIN, EVENTOUT Additional: OSC32OUT
OSCIN	5	I/O		Default: OSCIN Alternate: EVENTOUT, SPI1_NSS, I2S1_WS, CK_OUT, LPTIMER1_OUT, TIMER8_CH0, TIMER0_CH0 Additional: PF0
OSCOUT	6	I/O		Default: OSCOUT Alternate: EVENTOUT, SPI1_SCK, I2S1_CK, TIMER14_CH0_ON Additional: PF1
NRST	7	I/O		Default: NRST
VSS	8	P	-	Default: VSS
VREFP	9	P	-	Default: VREFP
VDD	10	P	-	Default: VDD
PA0	11	I/O	5VT	Default: PA0 Alternate: USART1_CTS, TIMER1_CH0, TIMER1_ETI, CMP0_OUT, EVENTOUT, UART3_TX, SPI1_SCK, I2S1_CK, LPTIMER0_OUT, CAN_RX Additional: WKUP0, ADC_IN0, RTC_TAMP1, CMP0_IM4
PA1	12	I/O	5VT	Default: PA1 Alternate: USART1_RTS, USART1_DE, TIMER1_CH1, I2C0_SMBA, SPI0_SCK, EVENTOUT, UART3_RX, TIMER14_CH0_ON, CAN_TX Additional:ADC_IN1, CMP0_IP
PA2	13	I/O	5VT	Default: PA2 Alternate: USART1_TX, TIMER8_CH0, TIMER1_CH2, SPI0_IO2, CMP1_OUT, LPUART0_TX, EVENTOUT, SPI0_MOSI, TIMER14_CH0 Additional: ADC_IN2, CMP1_IM4, RTC_TAMP2, WKUP2
PA3	14	I/O	5VT	Default: PA3 Alternate: USART1_RX, TIMER1_CH3, TIMER8_CH

GD32L235Cx LQFP48				
Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
				1, SPI0_IO3, LPUART0_RX, EVENTOUT, SPI1_MISO, I2S1_MCK, TIMER14_CH1 Additional: ADC_IN3, CMP1_IP0
PA4	15	I/O		Default: PA4 Alternate: SPI0_NSS, USART1_CK, SPI1_NSS, I2S1_WS, LPTIMER0_OUT, EVENTOUT, SPI1_MOSI, I2S1_SD, LPTIMER1_OUT, TIMER8_CH0, TIMER40_CH1[3], CAN_RX Additional: ADC_IN4, DAC0_OUT0
PA5	16	I/O	5VT	Default: PA5 Alternate: SPI0_SCK, TIMER1_CH0, TIMER1_ETI, LPTIMER0_ETI0, EVENTOUT, TIMER40_CH0[3], LPTIMER1_ETI0, CAN_TX Additional: ADC_IN5
PA6	17	I/O	5VT	Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, LPTIMER0_IN0, CMP0_OUT, LPUART0_CTS, EVENTOUT,TIMER0_BRKIN, I2C2_SDA, TIMER11_CH0, TIMER40_CH0[3], I2C1_SDA Additional: ADC_IN6
PA7	18	I/O	5VT	Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, LPTIMER0_ETI0, I2C2_SCL, CMP1_OUT, EVENTOUT, TIMER0_CH0_ON, TIMER11_CH1, TIMER11_CH0, TIMER8_CH0, I2C1_SCL Additional: ADC_IN7
PB0	19	I/O	5VT	Default: PB0 Alternate: TIMER2_CH2, LPTIMER0_OUT, SPI0_NSS, CMP0_OUT, EVENTOUT, UART4_TX[3], LPUART1_CTS, TIMER0_CH1_ON, LPTIMER1_IN1 Additional: ADC_IN8, VREF_OUT
PB1	20	I/O	5VT	Default: PB1 Alternate: TIMER2_CH3, LPUART0_RTS, LPUART0_DE, LPTIMER0_IN0, EVENTOUT, UART4_RX[3], LPUART1_RTS, LPUART1_DE, LPTIMER1_IN0, TIMER0_CH2_ON, TIMER8_CH0 Additional: ADC_IN9, VREF_OUT
BOOT1-PB2	21	I/O	5VT	Default: BOOT1 Alternate: LPTIMER0_OUT, EVENTOUT, RTC_OUT, I2C2_SMBA Additional: PB2, WKUP3
PB10	22	I/O	5VT	Default: PB10 Alternate: SPI1_SCK, I2S1_CK, LPUART0_TX, I2C1_SCL, LPUART0_RX, TIMER1_CH2, CMP0_OUT, EVENTOUT
PB11	23	I/O	5VT	Default: PB11

GD32L235Cx LQFP48				
Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
				Alternate: LPUART0_RX, I2C1_SDA, LPUART0_TX, TIMER1_CH3, CMP1_OUT, EVENTOUT, SPI1_MOSI, I2S1_SD
PB12	24	I/O	5VT	Default: PB12 Alternate: SPI1_NSS, I2S1_WS, I2C1_SMBA, LPUART0_RTS, LPUART0_DE, EVENTOUT, TIMER0_BRKIN, TIMER14_BRKIN
PB13	25	I/O	5VT	Default: PB13 Alternate: CK_OUT, SPI1_SCK, I2S1_CK, LPUART0_CTS, I2C1_SCL, EVENTOUT, TIMER8_CH0, TIMER0_CH0_ON, TIMER14_CH0_ON
PB14	26	I/O	5VT	Default: PB14 Alternate: SPI1_MISO, LPUART0_RTS, LPUART0_DE, I2C1_SDA, TIMER11_CH0, EVENTOUT, RTC_OUT, TIMER8_CH1, TIMER0_CH1_ON, TIMER14_CH0
PB15	27	I/O	5VT	Default: PB15 Alternate: SPI1_MOSI, I2S1_SD, TIMER11_CH1, EVENTOUT, TIMER0_CH2_ON, TIMER14_CH0_ON, TIMER14_CH1 Additional: RTC_REFIN
PC6	28	I/O	5VT	Default: PC6 Alternate: I2S1_MCK, TIMER2_CH0, EVENTOUT, TIMER11_CH0, LPUART1_TX, TIMER1_CH2 Additional: WKUP4
PC7	29	I/O	5VT	Default: PC7 Alternate: TIMER2_CH1, EVENTOUT, TIMER11_CH1, LPUART1_RX, TIMER1_CH3
PA8	30	I/O	5VT	Default: PA8 Alternate: USART0_CK, CK_OUT, LPTIMER0_OUT, I2C2_SMBA, EVENTOUT, CTC_SYNC, TIMER0_CH0, SPI1_NSS, I2S1_WS, LPTIMER1_OUT, I2C1_SMBA, I2C2_SCL
PA9	31	I/O	5VT	Default: PA9 Alternate: CK_OUT, USART0_TX, I2C0_SCL, EVENTOUT, LPTIMER0_IN1, TIMER0_CH1, SPI1_MISO, TIMER14_BRKIN, I2C1_SCL, I2C2_SMBA
PA10	32	I/O	5VT	Default: PA10 Alternate: USART0_RX, I2C0_SDA, EVENTOUT, TIMER0_CH2, I2C1_SDA, SPI1_MOSI, I2S1_SD
PA11	33	I/O	5VT	Default: PA11 Alternate: CMP0_OUT, USART0_CTS, SPI0_MISO, EVENTOUT, TIMER0_CH3, TIMER0_BRKIN, I2C1_SCL, CAN_RX, LPUART1_RTS, LPUART1_DE Additional: USBDM
PA12	34	I/O	5VT	Default: PA12

GD32L235Cx LQFP48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: CMP1_OUT, USART0_RTS, USART0_DE, SPI0_MOSI, EVENTOUT, TIMER0_ETI, I2C1_SDA, CAN_TX, LPUART1_CTS Additional: USBDP
PA13	35	I/O	5VT	Default: SWDIO Alternate: LPUART0_RX, I2C0_SCL, USART0_TX, SPI0_IO2, SPI0_NSS, EVENTOUT, LPUART1_RX Additional: PA13
PA14	36	I/O	5VT	Default: SWCLK Alternate: LPUART0_TX, USART1_TX, I2C0_SDA, USART0_RX, SPI0_IO3, SPI1_NSS, I2S1_WS, EVENTOUT, LPUART1_TX Additional: PA14
PA15	37	I/O	5VT	Default: PA15 Alternate: SPI1_NSS, I2S1_WS, TIMER1_CH0, TIMER1_ETI, SPI0_NSS, USART1_RX, EVENTOUT, I2C1_SMBA
PC10	38	I/O	5VT	Default: PC10 Alternate: UART3_TX, LPUART0_TX, SPI1_SCK, I2S1_CK, EVENTOUT, TIMER0_CH2
PC11	39	I/O	5VT	Default: PC11 Alternate: UART3_RX, LPUART0_RX, SPI1_MISO, EVENTOUT, TIMER0_CH3
PC12	40	I/O	5VT	Default: PC12 Alternate: UART4_TX(3), SPI1_MOSI, I2S1_SD, EVENTOUT, LPTIMER0_IN0, TIMER8_CH0
PB3	41	I/O	5VT	Default: PB3 Alternate: UART4_TX(3), SPI1_SCK, I2S1_CK, TIMER1_CH1, SPI0_SCK, USART0_RTS, USART0_DE, EVENTOUT, LPTIMER0_IN1, I2C2_SCL, I2C1_SCL, TIMER0_CH1 Additional: CMP1_IM6
PB4	42	I/O	5VT	Default: PB4 Alternate: UART4_RX(3), SPI1_MISO, TIMER2_CH0, SPI0_MISO, USART0_CTS, EVENTOUT, I2C2_SDA, I2C1_SDA, TIMER11_CH0 Additional: CMP1_IP1
PB5	43	I/O	5VT	Default: PB5 Alternate: LPTIMER0_IN0, I2C0_SMBA, SPI1_MOSI, I2S1_SD, SPI0_MOSI, USART0_CK, CMP1_OUT, EVENTOUT, TIMER40_BRKIN(3), TIMER2_CH1 Additional: CMP1_IP2, WKUP4
PB6	44	I/O	5VT	Default: PB6 Alternate: LPTIMER0_ETI0, I2C1_SCL, I2C0_SCL, USART0_TX, SPI0_IO2, EVENTOUT, SPI1_MISO,

GD32L235Cx LQFP48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				TIMER0_CH2, TIMER40_CH0_ON(3), LPUART1_RX Additional: CMP1_IP3
PB7	45	I/O	5VT	Default: PB7 Alternate: I2C1_SDA, I2C0_SDA, USART0_RX, SPI0_IO3, EVENTOUT, SPI1_MOSI, I2S1_SD, LPTIMER0_IN1, LPUART1_TX, CK_OUT Additional: CMP1_IP4
BOOT0-PD3	46	I/O	5VT	Default: BOOT0 Alternate: USART1_CTS, SPI1_MISO, I2S1_MCK, TIMER0_CH1_ON, UART4_RX(3), EVENTOUT Additional: PD3
PB8	47	I/O	5VT	Default: PB8 Alternate: I2C1_SCL, I2C0_SCL, CMP0_OUT, EVENTOUT, SPI1_SCK, I2S1_CK, TIMER14_BRKIN, CAN_RX, TIMER40_CH0(3)
PB9	48	I/O	5VT	Default: PB9 Alternate: I2C1_SDA, SPI1_NSS, I2S1_WS, I2C0_SDA, CMP1_OUT, EVENTOUT, CAN_TX, TIMER11_CH0, TIMER40_CH1(3)

Note:

(1) Type: I = input, O = output, A = analog, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Functions are available on GD32L235CB devices only.

2.6.4. GD32L235Cx QFN48 pin definitions

Table 2-7. GD32L235Cx QFN48 pin definitions

GD32L235Cx QFN48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
VBAT	1	P	-	Default: VBAT
PC13-TAMPER-RTC	2	I/O		Default: PC13 Alternate: TIMER0_BRKIN, EVENTOUT Additional: RTC_TAMP0, RTC_OUT, RTC_TS, WKUP1
PC14-OSC32IN	3	I/O		Default: PC14 Alternate: TIMER0_BRKIN, EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	4	I/O		Default: PC15 Alternate: TIMER14_BRKIN, EVENTOUT Additional: OSC32OUT
OSCIN	5	I/O		Default: OSCIN Alternate: EVENTOUT, SPI1_NSS, I2S1_WS, CK_OUT, LPTIMER1_OUT, TIMER8_CH0, TIMER0_CH0 Additional: PF0
OSCOUT	6	I/O		Default: OSCOUT Alternate: EVENTOUT, SPI1_SCK, I2S1_CK, TIMER14_CH0_ON Additional: PF1
NRST	7	I/O		Default: NRST
VSS	8	P	-	Default: VSS
VREFP	9	P	-	Default: VREFP
VDD	10	P	-	Default: VDD
PA0	11	I/O	5VT	Default: PA0 Alternate: USART1_CTS, TIMER1_CH0, TIMER1_ETI, CMP0_OUT, EVENTOUT, UART3_TX, SPI1_SCK, I2S1_CK, LPTIMER0_OUT, CAN_RX Additional: WKUP0, ADC_IN0, RTC_TAMP1, CMP0_IM4
PA1	12	I/O	5VT	Default: PA1 Alternate: USART1_RTS, USART1_DE, TIMER1_CH1, I2C0_SMBA, SPI0_SCK, EVENTOUT, UART3_RX, TIMER14_CH0_ON, CAN_TX Additional:ADC_IN1, CMP0_IP
PA2	13	I/O	5VT	Default: PA2 Alternate: USART1_TX, TIMER8_CH0, TIMER1_CH2, SPI0_IO2, CMP1_OUT, LPUART0_TX, EVENTOUT, SPI0_MOSI, TIMER14_CH0 Additional: ADC_IN2, CMP1_IM4, RTC_TAMP2, WKUP2
PA3	14	I/O	5VT	Default: PA3 Alternate: USART1_RX, TIMER1_CH3, TIMER8_CH

GD32L235Cx QFN48				
Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
				1, SPI0_IO3, LPUART0_RX, EVENTOUT, SPI1_MISO, I2S1_MCK, TIMER14_CH1 Additional: ADC_IN3, CMP1_IP0
PA4	15	I/O		Default: PA4 Alternate: SPI0_NSS, USART1_CK, SPI1_NSS, I2S1_WS, LPTIMER0_OUT, EVENTOUT, SPI1_MOSI, I2S1_SD, LPTIMER1_OUT, TIMER8_CH0, TIMER40_CH1[3], CAN_RX Additional: ADC_IN4, DAC0_OUT0
PA5	16	I/O	5VT	Default: PA5 Alternate: SPI0_SCK, TIMER1_CH0, TIMER1_ETI, LPTIMER0_ETI0, EVENTOUT, TIMER40_CH0[3], LPTIMER1_ETI0, CAN_TX Additional: ADC_IN5
PA6	17	I/O	5VT	Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, LPTIMER0_IN0, CMP0_OUT, LPUART0_CTS, EVENTOUT,TIMER0_BRKIN, I2C2_SDA, TIMER11_CH0, TIMER40_CH0[3], I2C1_SDA Additional: ADC_IN6
PA7	18	I/O	5VT	Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, LPTIMER0_ETI0, I2C2_SCL, CMP1_OUT, EVENTOUT, TIMER0_CH0_ON, TIMER11_CH1, TIMER11_CH0, TIMER8_CH0, I2C1_SCL Additional: ADC_IN7
PB0	19	I/O	5VT	Default: PB0 Alternate: TIMER2_CH2, LPTIMER0_OUT, SPI0_NSS, CMP0_OUT, EVENTOUT, UART4_TX[3], LPUART1_CTS, TIMER0_CH1_ON, LPTIMER1_IN1 Additional: ADC_IN8, VREF_OUT
PB1	20	I/O	5VT	Default: PB1 Alternate: TIMER2_CH3, LPUART0_RTS, LPUART0_DE, LPTIMER0_IN0, EVENTOUT, UART4_RX[3], LPUART1_RTS, LPUART1_DE, LPTIMER1_IN0, TIMER0_CH2_ON, TIMER8_CH0 Additional: ADC_IN9, VREF_OUT
BOOT1-PB2	21	I/O	5VT	Default: BOOT1 Alternate: LPTIMER0_OUT, EVENTOUT, RTC_OUT, I2C2_SMBA Additional: PB2, WKUP3
PB10	22	I/O	5VT	Default: PB10 Alternate: SPI1_SCK, I2S1_CK, LPUART0_TX, I2C1_SCL, LPUART0_RX, TIMER1_CH2, CMP0_OUT, EVENTOUT
PB11	23	I/O	5VT	Default: PB11

GD32L235Cx QFN48				
Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
				Alternate: LPUART0_RX, I2C1_SDA, LPUART0_TX, TIMER1_CH3, CMP1_OUT, EVENTOUT, SPI1_MOSI, I2S1_SD
PB12	24	I/O	5VT	Default: PB12 Alternate: SPI1_NSS, I2S1_WS, I2C1_SMBA, LPUART0_RTS, LPUART0_DE, EVENTOUT, TIMER0_BRKIN, TIMER14_BRKIN
PB13	25	I/O	5VT	Default: PB13 Alternate: CK_OUT, SPI1_SCK, I2S1_CK, LPUART0_CTS, I2C1_SCL, EVENTOUT, TIMER8_CH0, TIMER0_CH0_ON, TIMER14_CH0_ON
PB14	26	I/O	5VT	Default: PB14 Alternate: SPI1_MISO, LPUART0_RTS, LPUART0_DE, I2C1_SDA, TIMER11_CH0, EVENTOUT, RTC_OUT, TIMER8_CH1, TIMER0_CH1_ON, TIMER14_CH0
PB15	27	I/O	5VT	Default: PB15 Alternate: SPI1_MOSI, I2S1_SD, TIMER11_CH1, EVENTOUT, TIMER0_CH2_ON, TIMER14_CH0_ON, TIMER14_CH1 Additional: RTC_REFIN
PC6	28	I/O	5VT	Default: PC6 Alternate: I2S1_MCK, TIMER2_CH0, EVENTOUT, TIMER11_CH0, LPUART1_TX, TIMER1_CH2 Additional: WKUP4
PC7	29	I/O	5VT	Default: PC7 Alternate: TIMER2_CH1, EVENTOUT, TIMER11_CH1, LPUART1_RX, TIMER1_CH3
PA8	30	I/O	5VT	Default: PA8 Alternate: USART0_CK, CK_OUT, LPTIMER0_OUT, I2C2_SMBA, EVENTOUT, CTC_SYNC, TIMER0_CH0, SPI1_NSS, I2S1_WS, LPTIMER1_OUT, I2C1_SMBA, I2C2_SCL
PA9	31	I/O	5VT	Default: PA9 Alternate: CK_OUT, USART0_TX, I2C0_SCL, EVENTOUT, LPTIMER0_IN1, TIMER0_CH1, SPI1_MISO, TIMER14_BRKIN, I2C1_SCL, I2C2_SMBA
PA10	32	I/O	5VT	Default: PA10 Alternate: USART0_RX, I2C0_SDA, EVENTOUT, TIMER0_CH2, I2C1_SDA, SPI1_MOSI, I2S1_SD
PA11	33	I/O	5VT	Default: PA11 Alternate: CMP0_OUT, USART0_CTS, SPI0_MISO, EVENTOUT, TIMER0_CH3, TIMER0_BRKIN, I2C1_SCL, CAN_RX, LPUART1_RTS, LPUART1_DE Additional: USBDM
PA12	34	I/O	5VT	Default: PA12

GD32L235Cx QFN48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: CMP1_OUT, USART0_RTS, USART0_DE, SPI0_MOSI, EVENTOUT, TIMER0_ETI, I2C1_SDA, CAN_TX, LPUART1_CTS Additional: USBDP
PA13	35	I/O	5VT	Default: SWDIO Alternate: LPUART0_RX, I2C0_SCL, USART0_TX, SPI0_IO2, SPI0_NSS, EVENTOUT, LPUART1_RX Additional: PA13
PA14	36	I/O	5VT	Default: SWCLK Alternate: LPUART0_TX, USART1_TX, I2C0_SDA, USART0_RX, SPI0_IO3, SPI1_NSS, I2S1_WS, EVENTOUT, LPUART1_TX Additional: PA14
PA15	37	I/O	5VT	Default: PA15 Alternate: SPI1_NSS, I2S1_WS, TIMER1_CH0, TIMER1_ETI, SPI0_NSS, USART1_RX, EVENTOUT, I2C1_SMBA
PC10	38	I/O	5VT	Default: PC10 Alternate: UART3_TX, LPUART0_TX, SPI1_SCK, I2S1_CK, EVENTOUT, TIMER0_CH2
PC11	39	I/O	5VT	Default: PC11 Alternate: UART3_RX, LPUART0_RX, SPI1_MISO, EVENTOUT, TIMER0_CH3
PC12	40	I/O	5VT	Default: PC12 Alternate: UART4_TX(3), SPI1_MOSI, I2S1_SD, EVENTOUT, LPTIMER0_IN0, TIMER8_CH0
PB3	41	I/O	5VT	Default: PB3 Alternate: UART4_TX(3), SPI1_SCK, I2S1_CK, TIMER1_CH1, SPI0_SCK, USART0_RTS, USART0_DE, EVENTOUT, LPTIMER0_IN1, I2C2_SCL, I2C1_SCL, TIMER0_CH1 Additional: CMP1_IM6
PB4	42	I/O	5VT	Default: PB4 Alternate: UART4_RX(3), SPI1_MISO, TIMER2_CH0, SPI0_MISO, USART0_CTS, EVENTOUT, I2C2_SDA, I2C1_SDA, TIMER11_CH0 Additional: CMP1_IP1
PB5	43	I/O	5VT	Default: PB5 Alternate: LPTIMER0_IN0, I2C0_SMBA, SPI1_MOSI, I2S1_SD, SPI0_MOSI, USART0_CK, CMP1_OUT, EVENTOUT, TIMER40_BRKIN(3), TIMER2_CH1 Additional: CMP1_IP2, WKUP4
PB6	44	I/O	5VT	Default: PB6 Alternate: LPTIMER0_ETI0, I2C1_SCL, I2C0_SCL, USART0_TX, SPI0_IO2, EVENTOUT, SPI1_MISO,

GD32L235Cx QFN48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				TIMER0_CH2, TIMER40_CH0_ON(3), LPUART1_RX Additional: CMP1_IP3
PB7	45	I/O	5VT	Default: PB7 Alternate: I2C1_SDA, I2C0_SDA, USART0_RX, SPI0_IO3, EVENTOUT, SPI1_MOSI, I2S1_SD, LPTIMER0_IN1, LPUART1_TX, CK_OUT Additional: CMP1_IP4
BOOT0-PD3	46	I/O	5VT	Default: BOOT0 Alternate: USART1_CTS, SPI1_MISO, I2S1_MCK, TIMER0_CH1_ON, UART4_RX(3), EVENTOUT Additional: PD3
PB8	47	I/O	5VT	Default: PB8 Alternate: I2C1_SCL, I2C0_SCL, CMP0_OUT, EVENTOUT, SPI1_SCK, I2S1_CK, TIMER14_BRKIN, CAN_RX, TIMER40_CH0(3)
PB9	48	I/O	5VT	Default: PB9 Alternate: I2C1_SDA, SPI1_NSS, I2S1_WS, I2C0_SDA, CMP1_OUT, EVENTOUT, CAN_TX, TIMER11_CH0, TIMER40_CH1(3)

Note:

(1) Type: I = input, O = output, A = analog, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Functions are available on GD32L235CB devices only.

2.6.5. GD32L235Kx LQFP32 pin definitions

Table 2-8. GD32L235Kx LQFP32 pin definitions

GD32L235Kx LQFP32				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
VDD	1	P		Default: VDD
OSCIN	2	I/O		Default: OSCIN Alternate: EVENTOUT, SPI1_NSS, I2S1_WS, CK_OUT, LPTIMER1_OUT, TIMER8_CH0, TIMER0_CH0 Additional: PF0
OSCOUT	3	I/O		Default: OSCOUT Alternate: EVENTOUT, SPI1_SCK, I2S1_CK, TIMER14_CH0_ON Additional: PF1
NRST	4	I/O		Default: NRST
VDDA	5	P	-	Default: VDDA
PA0	6	I/O	5VT	Default: PA0 Alternate: USART1_CTS, TIMER1_CH0, TIMER1_ETI, CMP0_OUT, EVENTOUT, UART3_TX, SPI1_SCK, I2S1_CK, LPTIMER0_OUT, CAN_RX Additional: WKUP0, ADC_IN0, RTC_TAMP1, CMP0_IM4
PA1	7	I/O	5VT	Default: PA1 Alternate: USART1_RTS, USART1_DE, TIMER1_CH1, I2C0_SMBA, SPI0_SCK, EVENTOUT, UART3_RX, TIMER14_CH0_ON, CAN_TX Additional:ADC_IN1, CMP0_IP
PA2	8	I/O	5VT	Default: PA2 Alternate: USART1_TX, TIMER8_CH0, TIMER1_CH2, SPI0_IO2, CMP1_OUT, LPUART0_TX, EVENTOUT, SPI0_MOSI, TIMER14_CH0 Additional: ADC_IN2, CMP1_IM4, RTC_TAMP2, WKUP2
PA3	9	I/O	5VT	Default: PA3 Alternate: USART1_RX, TIMER1_CH3, TIMER8_CH1, SPI0_IO3, LPUART0_RX, EVENTOUT, SPI1_MISO, I2S1_MCK, TIMER14_CH1 Additional: ADC_IN3, CMP1_IP0
PA4	10	I/O		Default: PA4 Alternate: SPI0_NSS, USART1_CK, SPI1_NSS, I2S1_WS, LPTIMER0_OUT, EVENTOUT, SPI1_MOSI, I2S1_SD, LPTIMER1_OUT, TIMER8_CH0, TIMER40_CH1(3) , CAN_RX Additional: ADC_IN4, DAC0_OUT0
PA5	11	I/O	5VT	Default: PA5 Alternate: SPI0_SCK, TIMER1_CH0, TIMER1_ETI, LPTIMER0_ETI0, EVENTOUT, TIMER40_CH0(3), LP

GD32L235Kx LQFP32				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				TIMER1_ETI0 , CAN_TX Additional: ADC_IN5
PA6	12	I/O	5VT	Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, LPTIMER0_IN0, CMP0_OUT, LPUART0_CTS, EVENTOUT,TIMER0_BRKIN, I2C2_SDA, TIMER11_CH0, TIMER40_CH0(3), I2C1_SDA Additional: ADC_IN6
PA7	13	I/O	5VT	Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, LPTIMER0_ETI0, I2C2_SCL, CMP1_OUT, EVENTOUT, TIMER0_CH0_ON, TIMER11_CH1, TIMER11_CH0, TIMER8_CH0, I2C1_SCL Additional: ADC_IN7
PB0	14	I/O	5VT	Default: PB0 Alternate: TIMER2_CH2, LPTIMER0_OUT, SPI0_NSS, CMP0_OUT, EVENTOUT, UART4_TX(3), LPUART1_CTS, TIMER0_CH1_ON, LPTIMER1_IN1 Additional: ADC_IN8, VREF_OUT
PB1	15	I/O	5VT	Default: PB1 Alternate: TIMER2_CH3, LPUART0_RTS, LPUART0_DE, LPTIMER0_IN0, EVENTOUT, UART4_RX(3), LPUART1_RTS, LPUART1_DE, LPTIMER1_IN0, TIMER0_CH2_ON, TIMER8_CH0 Additional: ADC_IN9, VREF_OUT
BOOT1-PB2	16	I/O	5VT	Default: BOOT1 Alternate: LPTIMER0_OUT, EVENTOUT, RTC_OUT, I2C2_SMBA Additional: PB2, WKUP3
VDD	17	P		Default: VDD
PA8	18	I/O	5VT	Default: PA8 Alternate: USART0_CK, CK_OUT, LPTIMER0_OUT, I2C2_SMBA, EVENTOUT, CTC_SYNC, TIMER0_CH0, SPI1_NSS, I2S1_WS, LPTIMER1_OUT, I2C1_SMBA, I2C2_SCL
PA9	19	I/O	5VT	Default: PA9 Alternate: CK_OUT, USART0_TX, I2C0_SCL, EVENTOUT, LPTIMER0_IN1, TIMER0_CH1, SPI1_MISO, TIMER14_BRKIN, I2C1_SCL, I2C2_SMBA
PA10	20	I/O	5VT	Default: PA10 Alternate: USART0_RX, I2C0_SDA, EVENTOUT, TIMER0_CH2, I2C1_SDA, SPI1_MOSI, I2S1_SD
PA11	21	I/O	5VT	Default: PA11 Alternate: CMP0_OUT, USART0_CTS, SPI0_MISO, EVENTOUT, TIMER0_CH3, TIMER0_BRKIN, I2C1_SCL, LPUART1_RTS, LPUART1_DE, CAN_RX

GD32L235Kx LQFP32				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Additional: USBDM
PA12	22	I/O	5VT	Default: PA12 Alternate: CMP1_OUT, USART0_RTS, USART0_DE, SPI0_MOSI, EVENTOUT, TIMER0_ETI, I2C1_SDA, LPUART1_CTS, CAN_TX Additional: USBDP
PA13	23	I/O	5VT	Default: SWDIO Alternate: LPUART0_RX, I2C0_SCL, USART0_TX, SPI0_IO2, SPI0_NSS, EVENTOUT, LPUART1_RX Additional: PA13
PA14	24	I/O	5VT	Default: SWCLK Alternate: LPUART0_TX, USART1_TX, I2C0_SDA, USART0_RX, SPI0_IO3, SPI1_NSS, I2S1_WS, EVENTOUT, LPUART1_TX Additional: PA14
PA15	25	I/O	5VT	Default: PA15 Alternate: SPI1_NSS, I2S1_WS, TIMER1_CH0, TIMER1_ETI, SPI0_NSS, USART1_RX, EVENTOUT, I2C1_SMBA
PB3	26	I/O	5VT	Default: PB3 Alternate: UART4_TX(3), SPI1_SCK, I2S1_CK, TIMER1_CH1, SPI0_SCK, USART0_RTS, USART0_DE, EVENTOUT, LPTIMER0_IN1, I2C2_SCL, I2C1_SCL, TIMER0_CH1 Additional: CMP1_IM6
PB4	27	I/O	5VT	Default: PB4 Alternate: UART4_RX(3), SPI1_MISO, TIMER2_CH0, SPI0_MISO, USART0_CTS, EVENTOUT, I2C2_SDA, I2C1_SDA, TIMER11_CH0 Additional: CMP1_IP1
PB5	28	I/O	5VT	Default: PB5 Alternate: LPTIMER0_IN0, I2C0_SMBA, SPI1_MOSI, I2S1_SD, SPI0_MOSI, USART0_CK, CMP1_OUT, EVENTOUT, TIMER40_BRKIN(3), TIMER2_CH1 Additional: CMP1_IP2, WKUP4
PB6	29	I/O	5VT	Default: PB6 Alternate: LPTIMER0_ETI0, I2C1_SCL, I2C0_SCL, USART0_TX, SPI0_IO2, EVENTOUT, SPI1_MISO, TIMER0_CH2, TIMER40_CH0_ON(3), LPUART1_RX Additional: CMP1_IP3
PB7	30	I/O	5VT	Default: PB7 Alternate: I2C1_SDA, I2C0_SDA, USART0_RX, SPI0_IO3, EVENTOUT, SPI1_MOSI, I2S1_SD, LPTIMER0_IN1, LPUART1_TX, CK_OUT Additional: CMP1_IP4

GD32L235Kx LQFP32				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
BOOT0-PD3	31	I/O	5VT	Default: BOOT0 Alternate: USART1_CTS, SPI1_MISO, I2S1_MCK, TIMER0_CH1_ON, UART4_RX(3), EVENTOUT Additional: PD3
VSS	32	P	-	Default: VSS

Note:

(1) Type: I = input, O = output, A = analog, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Functions are available on GD32L235KB devices only.

2.6.6. GD32L235Kx QFN32 pin definitions

Table 2-9. GD32L235Kx QFN32 pin definitions

GD32L235Kx QFN32				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PC14-OSC32IN	1	I/O		Default: PC14 Alternate: TIMER0_BRKIN, EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	2	I/O		Default: PC15 Alternate: TIMER14_BRKIN, EVENTOUT Additional: OSC32OUT
OSCIN	3	I/O		Default: OSCIN Alternate: EVENTOUT, SPI1_NSS, I2S1_WS, CK_OUT, LPTIMER1_OUT, TIMER8_CH0, TIMER0_CH0 Additional: PF0
OSCOUT	4	I/O		Default: OSCOUT Alternate: EVENTOUT, SPI1_SCK, I2S1_CK, TIMER14_CH0_ON Additional: PF1
NRST	5	I/O		Default: NRST
VDD	6	P	-	Default: VDD
PA0	7	I/O	5VT	Default: PA0 Alternate: USART1_CTS, TIMER1_CH0, TIMER1_ETI, CMP0_OUT, EVENTOUT, UART3_TX, SPI1_SCK, I2S1_CK, LPTIMER0_OUT, CAN_RX Additional: WKUP0, ADC_IN0, RTC_TAMP1, CMP0_IM4
PA1	8	I/O	5VT	Default: PA1 Alternate: USART1_RTS, USART1_DE, TIMER1_CH1, I2C0_SMBA, SPI0_SCK, EVENTOUT, UART3_RX, TIMER14_CH0_ON, CAN_TX Additional:ADC_IN1, CMP0_IP
PA2	9	I/O	5VT	Default: PA2 Alternate: USART1_TX, TIMER8_CH0, TIMER1_CH2, SPI0_IO2, CMP1_OUT, LPUART0_TX, EVENTOUT, SPI0_MOSI, TIMER14_CH0 Additional: ADC_IN2, CMP1_IM4, RTC_TAMP2, WKUP2
PA3	10	I/O	5VT	Default: PA3 Alternate: USART1_RX, TIMER1_CH3, TIMER8_CH1, SPI0_IO3, LPUART0_RX, EVENTOUT, SPI1_MISO, I2S1_MCK, TIMER14_CH1 Additional: ADC_IN3, CMP1_IP0
PA4	11	I/O		Default: PA4 Alternate: SPI0_NSS, USART1_CK, SPI1_NSS, I2S1_WS, LPTIMER0_OUT, EVENTOUT, SPI1_MOSI, I2S1_SD, LPTIMER1_OUT, TIMER8_CH0, TIMER40

GD32L235Kx QFN32				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				_CH1(3) , CAN_RX Additional: ADC_IN4, DAC0_OUT0
PA5	12	I/O	5VT	Default: PA5 Alternate: SPI0_SCK, TIMER1_CH0, TIMER1_ETI, LPTIMER0_ETI0, EVENTOUT, TIMER40_CH0(3), LPTIMER1_ETI0 , CAN_TX Additional: ADC_IN5
PA6	13	I/O	5VT	Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, LPTIMER0_IN0, CMP0_OUT, LPUART0_CTS, EVENTOUT,TIMER0_BRKIN, I2C2_SDA, TIMER11_CH0, TIMER40_CH0(3), I2C1_SDA Additional: ADC_IN6
PA7	14	I/O	5VT	Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, LPTIMER0_ETI0, I2C2_SCL, CMP1_OUT, EVENTOUT, TIMER0_CH0_ON, TIMER11_CH1, TIMER11_CH0, TIMER8_CH0, I2C1_SCL Additional: ADC_IN7
PB0	15	I/O	5VT	Default: PB0 Alternate: TIMER2_CH2, LPTIMER0_OUT, SPI0_NSS, CMP0_OUT, EVENTOUT, UART4_TX(3), LPUART1_CTS, TIMER0_CH1_ON, LPTIMER1_IN1 Additional: ADC_IN8, VREF_OUT
PB1	16	I/O	5VT	Default: PB1 Alternate: TIMER2_CH3, LPUART0_RTS, LPUART0_DE, LPTIMER0_IN0, EVENTOUT, UART4_RX(3), LPUART1_RTS, LPUART1_DE, LPTIMER1_IN0, TIMER0_CH2_ON, TIMER8_CH0 Additional: ADC_IN9, VREF_OUT
BOOT1-PB2	17	I/O	5VT	Default: BOOT1 Alternate: LPTIMER0_OUT, EVENTOUT, RTC_OUT, I2C2_SMBA Additional: PB2, WKUP3
PA8	18	I/O	5VT	Default: PA8 Alternate: USART0_CK, CK_OUT, LPTIMER0_OUT, I2C2_SMBA, EVENTOUT, CTC_SYNC, TIMER0_CH0, SPI1_NSS, I2S1_WS, LPTIMER1_OUT, I2C1_SMBA, I2C2_SCL
PA9	19	I/O	5VT	Default: PA9 Alternate: CK_OUT, USART0_TX, I2C0_SCL, EVENTOUT, LPTIMER0_IN1, TIMER0_CH1, SPI1_MISO, TIMER14_BRKIN, I2C1_SCL, I2C2_SMBA
PA10	20	I/O	5VT	Default: PA10 Alternate: USART0_RX, I2C0_SDA, EVENTOUT, TIMER0_CH2, I2C1_SDA, SPI1_MOSI, I2S1_SD

GD32L235Kx QFN32				
Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
PA11	21	I/O	5VT	Default: PA11 Alternate: CMP0_OUT, USART0_CTS, SPI0_MISO, EVENTOUT, TIMER0_CH3, TIMER0_BRKIN, I2C1_SCL, LPUART1_RTS, LPUART1_DE, CAN_RX Additional: USBDM
PA12	22	I/O	5VT	Default: PA12 Alternate: CMP1_OUT, USART0_RTS, USART0_DE, SPI0_MOSI, EVENTOUT, TIMER0_ETI, I2C1_SDA, LPUART1_CTS, CAN_TX Additional: USBDP
PA13	23	I/O	5VT	Default: SWDIO Alternate: LPUART0_RX, I2C0_SCL, USART0_TX, SPI0_IO2, SPI0_NSS, EVENTOUT, LPUART1_RX Additional: PA13
PA14	24	I/O	5VT	Default: SWCLK Alternate: LPUART0_TX, USART1_TX, I2C0_SDA, USART0_RX, SPI0_IO3, SPI1_NSS, I2S1_WS, EVENTOUT, LPUART1_TX Additional: PA14
PA15	25	I/O	5VT	Default: PA15 Alternate: SPI1_NSS, I2S1_WS, TIMER1_CH0, TIMER1_ETI, SPI0_NSS, USART1_RX, EVENTOUT, I2C1_SMBA
PB3	26	I/O	5VT	Default: PB3 Alternate: UART4_TX[3], SPI1_SCK, I2S1_CK, TIMER1_CH1, SPI0_SCK, USART0_RTS, USART0_DE, EVENTOUT, LPTIMER0_IN1, I2C2_SCL, I2C1_SCL, TIMER0_CH1 Additional: CMP1_IM6
PB4	27	I/O	5VT	Default: PB4 Alternate: UART4_RX[3], SPI1_MISO, TIMER2_CH0, SPI0_MISO, USART0_CTS, EVENTOUT, I2C2_SDA, I2C1_SDA, TIMER11_CH0 Additional: CMP1_IP1
PB5	28	I/O	5VT	Default: PB5 Alternate: LPTIMER0_IN0, I2C0_SMBA, SPI1_MOSI, I2S1_SD, SPI0_MOSI, USART0_CK, CMP1_OUT, EVENTOUT, TIMER40_BRKIN[3], TIMER2_CH1 Additional: CMP1_IP2, WKUP4
PB6	29	I/O	5VT	Default: PB6 Alternate: LPTIMER0_ETI0, I2C1_SCL, I2C0_SCL, USART0_TX, SPI0_IO2, EVENTOUT, SPI1_MISO, TIMER0_CH2, TIMER40_CH0_ON[3], LPUART1_RX Additional: CMP1_IP3
PB7	30	I/O	5VT	Default: PB7 Alternate: I2C1_SDA, I2C0_SDA, USART0_RX, SPI

GD32L235Kx QFN32				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				0_IO3, EVENTOUT, SPI1_MOSI, I2S1_SD, LPTIMER0_IN1, LPUART1_TX, CK_OUT Additional: CMP1_IP4
BOOT0-PD3	31	I/O	5VT	Default: BOOT0 Alternate: USART1_CTS, SPI1_MISO, I2S1_MCK, TIMER0_CH1_ON, UART4_RX(3), EVENTOUT Additional: PD3
VBAT	32	P	-	Default: VBAT

Note:

(1) Type: I = input, O = output, A = analog, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Functions are available on GD32L235KB devices only.

2.6.7. GD32L235KxxxP QFN32 VREFP pin definitions

Table 2-10. GD32L235KxxxP QFN32 VREFP pin definitions

GD32L235KxxxP QFN32 VREFP				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PC14-OSC32IN	1	I/O		Default: PC14 Alternate: TIMER0_BRKIN, EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	2	I/O		Default: PC15 Alternate: TIMER14_BRKIN, EVENTOUT Additional: OSC32OUT
OSCIN	3	I/O		Default: OSCIN Alternate: EVENTOUT, SPI1_NSS, I2S1_WS, CK_OUT, LPTIMER1_OUT, TIMER8_CH0, TIMER0_CH0 Additional: PF0
OSCOUT	4	I/O		Default: OSCOUT Alternate: EVENTOUT, SPI1_SCK, I2S1_CK, TIMER14_CH0_ON Additional: PF1
NRST	5	I/O		Default: NRST
VREFP	6	P	-	Default: VREFP
VDD	7	P	-	Default: VDD
PA0	8	I/O	5VT	Default: PA0 Alternate: USART1_CTS, TIMER1_CH0, TIMER1_ETI, CMP0_OUT, EVENTOUT, UART3_TX, SPI1_SCK, I2S1_CK, LPTIMER0_OUT, CAN_RX Additional: WKUP0, ADC_IN0, RTC_TAMP1, CMP0_IM4
PA1	9	I/O	5VT	Default: PA1 Alternate: USART1_RTS, USART1_DE, TIMER1_CH1, I2C0_SMBA, SPI0_SCK, EVENTOUT, UART3_RX, TIMER14_CH0_ON, CAN_TX Additional:ADC_IN1, CMP0_IP
PA2	10	I/O	5VT	Default: PA2 Alternate: USART1_TX, TIMER8_CH0, TIMER1_CH2, SPI0_IO2, CMP1_OUT, LPUART0_TX, EVENTOUT, SPI0_MOSI, TIMER14_CH0 Additional: ADC_IN2, CMP1_IM4, RTC_TAMP2, WKUP2
PA3	11	I/O	5VT	Default: PA3 Alternate: USART1_RX, TIMER1_CH3, TIMER8_CH1, SPI0_IO3, LPUART0_RX, EVENTOUT, SPI1_MISO, I2S1_MCK, TIMER14_CH1 Additional: ADC_IN3, CMP1_IP0
PA4	12	I/O		Default: PA4 Alternate: SPI0_NSS, USART1_CK, SPI1_NSS, I2S1_WS, LPTIMER0_OUT, EVENTOUT, SPI1_MOSI, I

GD32L235KxxxP QFN32 VREFP				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				2S1_SD, LPTIMER1_OUT, TIMER8_CH0, TIMER40_CH1(3) , CAN_RX Additional: ADC_IN4, DAC0_OUT0
PA5	13	I/O	5VT	Default: PA5 Alternate: SPI0_SCK, TIMER1_CH0, TIMER1_ETI, LPTIMER0_ETI0, EVENTOUT, TIMER40_CH0(3), LPTIMER1_ETI0 , CAN_TX Additional: ADC_IN5
PA6	14	I/O	5VT	Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, LPTIMER0_IN0, CMP0_OUT, LPUART0_CTS, EVENTOUT,TIMER0_BRKIN, I2C2_SDA, TIMER11_CH0, TIMER40_CH0(3), I2C1_SDA Additional: ADC_IN6
PA7	15	I/O	5VT	Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, LPTIMER0_ETI0, I2C2_SCL, CMP1_OUT, EVENTOUT, TIMER0_CH0_ON, TIMER11_CH1, TIMER11_CH0, TIMER8_CH0, I2C1_SCL Additional: ADC_IN7
PB0	16	I/O	5VT	Default: PB0 Alternate: TIMER2_CH2, LPTIMER0_OUT, SPI0_NSS, CMP0_OUT, EVENTOUT, UART4_TX(3), LPUART1_CTS, TIMER0_CH1_ON, LPTIMER1_IN1 Additional: ADC_IN8, VREF_OUT
PB1	17	I/O	5VT	Default: PB1 Alternate: TIMER2_CH3, LPUART0_RTS, LPUART0_DE, LPTIMER0_IN0, EVENTOUT, UART4_RX(3), LPUART1_RTS, LPUART1_DE, LPTIMER1_IN0, TIMER0_CH2_ON, TIMER8_CH0 Additional: ADC_IN9, VREF_OUT
BOOT1-PB2	18	I/O	5VT	Default: BOOT1 Alternate: LPTIMER0_OUT, EVENTOUT, RTC_OUT, I2C2_SMBA Additional: PB2, WKUP3
PA8	19	I/O	5VT	Default: PA8 Alternate: USART0_CK, CK_OUT, LPTIMER0_OUT, I2C2_SMBA, EVENTOUT, CTC_SYNC, TIMER0_CH0, SPI1_NSS, I2S1_WS, LPTIMER1_OUT, I2C1_SMBA, I2C2_SCL
PA9	20	I/O	5VT	Default: PA9 Alternate: CK_OUT, USART0_TX, I2C0_SCL, EVENTOUT, LPTIMER0_IN1, TIMER0_CH1, SPI1_MISO, TIMER14_BRKIN, I2C1_SCL, I2C2_SMBA
PA11	21	I/O	5VT	Default: PA11 Alternate: CMP0_OUT, USART0_CTS, SPI0_MISO,

GD32L235KxxxP QFN32 VREFP				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				EVENTOUT, TIMER0_CH3, TIMER0_BRKIN, I2C1_SCL, LPUART1_RTS, LPUART1_DE, CAN_RX Additional: USBDM
PA12	22	I/O	5VT	Default: PA12 Alternate: CMP1_OUT, USART0_RTS, USART0_DE, SPI0_MOSI, EVENTOUT, TIMER0_ETI, I2C1_SDA, LPUART1_CTS, CAN_TX Additional: USBDP
PA13	23	I/O	5VT	Default: SWDIO Alternate: LPUART0_RX, I2C0_SCL, USART0_TX, SPI0_IO2, SPI0_NSS, EVENTOUT, LPUART1_RX Additional: PA13
PA14	24	I/O	5VT	Default: SWCLK Alternate: LPUART0_TX, USART1_TX, I2C0_SDA, USART0_RX, SPI0_IO3, SPI1_NSS, I2S1_WS, EVENTOUT, LPUART1_TX Additional: PA14
PA15	25	I/O	5VT	Default: PA15 Alternate: SPI1_NSS, I2S1_WS, TIMER1_CH0, TIMER1_ETI, SPI0_NSS, USART1_RX, EVENTOUT, I2C1_SMBA
PB3	26	I/O	5VT	Default: PB3 Alternate: UART4_TX(3), SPI1_SCK, I2S1_CK, TIMER1_CH1, SPI0_SCK, USART0_RTS, USART0_DE, EVENTOUT, LPTIMER0_IN1, I2C2_SCL, I2C1_SCL, TIMER0_CH1 Additional: CMP1_IM6
PB4	27	I/O	5VT	Default: PB4 Alternate: UART4_RX(3), SPI1_MISO, TIMER2_CH0, SPI0_MISO, USART0_CTS, EVENTOUT, I2C2_SDA, I2C1_SDA, TIMER11_CH0 Additional: CMP1_IP1
PB5	28	I/O	5VT	Default: PB5 Alternate: LPTIMER0_IN0, I2C0_SMBA, SPI1_MOSI, I2S1_SD, SPI0_MOSI, USART0_CK, CMP1_OUT, EVENTOUT, TIMER40_BRKIN(3), TIMER2_CH1 Additional: CMP1_IP2, WKUP4
PB6	29	I/O	5VT	Default: PB6 Alternate: LPTIMER0_ETI0, I2C1_SCL, I2C0_SCL, USART0_TX, SPI0_IO2, EVENTOUT, SPI1_MISO, TIMER0_CH2, TIMER40_CH0_ON(3), LPUART1_RX Additional: CMP1_IP3
PB7	30	I/O	5VT	Default: PB7 Alternate: I2C1_SDA, I2C0_SDA, USART0_RX, SPI0_IO3, EVENTOUT, SPI1_MOSI, I2S1_SD, LPTIME

GD32L235KxxxP QFN32 VREFP				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				R0_IN1, LPUART1_TX, CK_OUT Additional: CMP1_IP4
BOOT0-PD3	31	I/O	5VT	Default: BOOT0 Alternate: USART1_CTS, SPI1_MISO, I2S1_MCK, TIMER0_CH1_ON, UART4_RX(3), EVENTOUT Additional: PD3
VBAT	32	P	-	Default: VBAT

Note:

(1) Type: I = input, O = output, A = analog, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Functions are available on GD32L235KB devices only.

2.6.8. GD32L235Ex WLCSP25 pin definitions

Table 2-11. GD32L235Ex WLCSP25 pin definitions

GD32L235Ex WLCSP25				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PC14-OSC32IN	C3	I/O		Default: PC14 Alternate: TIMER0_BRKIN, EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	B4	I/O		Default: PC15 Alternate: TIMER14_BRKIN, EVENTOUT Additional: OSC32OUT
OSCIN	B5	I/O		Default: OSCIN Alternate: EVENTOUT, SPI1_NSS, I2S1_WS, CK_OUT, LPTIMER1_OUT, TIMER8_CH0, TIMER0_CH0 Additional: PF0
NRST	C5	I/O		Default: NRST
PA0	E5	I/O	5VT	Default: PA0 Alternate: USART1_CTS, TIMER1_CH0, TIMER1_ETI, CMP0_OUT, EVENTOUT, UART3_TX, SPI1_SCK, I2S1_CK, LPTIMER0_OUT, CAN_RX Additional: WKUP0, ADC_IN0, RTC_TAMP1, CMP0_IM4
PA1	D5	I/O	5VT	Default: PA1 Alternate: USART1_RTS, USART1_DE, TIMER1_CH1, I2C0_SMBA, SPI0_SCK, EVENTOUT, UART3_RX, TIMER14_CH0_ON, CAN_TX Additional:ADC_IN1, CMP0_IP
PA2	C4	I/O	5VT	Default: PA2 Alternate: USART1_TX, TIMER8_CH0, TIMER1_CH2, SPI0_IO2, CMP1_OUT, LPUART0_TX, EVENTOUT, SPI0_MOSI, TIMER14_CH0 Additional: ADC_IN2, CMP1_IM4, RTC_TAMP2, WKUP2
PA3	E4	I/O	5VT	Default: PA3 Alternate: USART1_RX, TIMER1_CH3, TIMER8_CH1, SPI0_IO3, LPUART0_RX, EVENTOUT, SPI1_MISO, I2S1_MCK, TIMER14_CH1 Additional: ADC_IN3, CMP1_IP0
PA4	D4	I/O		Default: PA4 Alternate: SPI0_NSS, USART1_CK, SPI1_NSS, I2S1_WS, LPTIMER0_OUT, EVENTOUT, SPI1_MOSI, I2S1_SD, LPTIMER1_OUT, TIMER8_CH0, TIMER40_CH1(3) , CAN_RX Additional: ADC_IN4, DAC0_OUT0
PA5	D3	I/O	5VT	Default: PA5 Alternate: SPI0_SCK, TIMER1_CH0, TIMER1_ETI, LPTIMER0_ETI0, EVENTOUT, TIMER40_CH0(3), LP

GD32L235Ex WLCSP25				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				TIMER1_ETI0 , CAN_TX Additional: ADC_IN5
PA6	E3	I/O	5VT	Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, LPTIMER0_IN0, CMP0_OUT, LPUART0_CTS, EVENTOUT,TIMER0_BRKIN, I2C2_SDA, TIMER11_CH0, TIMER40_CH0(3), I2C1_SDA Additional: ADC_IN6
PA7	D2	I/O	5VT	Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, LPTIMER0_ETI0, I2C2_SCL, CMP1_OUT, EVENTOUT, TIMER0_CH0_ON, TIMER11_CH1, TIMER11_CH0, TIMER8_CH0, I2C1_SCL Additional: ADC_IN7
PB0	E2	I/O	5VT	Default: PB0 Alternate: TIMER2_CH2, LPTIMER0_OUT, SPI0_NSS, CMP0_OUT, EVENTOUT, UART4_TX(3), LPUART1_CTS, TIMER0_CH1_ON, LPTIMER1_IN1 Additional: ADC_IN8, VREF_OUT
PB1	D1	I/O	5VT	Default: PB1 Alternate: TIMER2_CH3, LPUART0_RTS, LPUART0_DE, LPTIMER0_IN0, EVENTOUT, UART4_RX(3), LPUART1_RTS, LPUART1_DE, LPTIMER1_IN0, TIMER0_CH2_ON, TIMER8_CH0 Additional: ADC_IN9, VREF_OUT
BOOT1-PB2	E1	I/O	5VT	Default: BOOT1 Alternate: LPTIMER0_OUT, EVENTOUT, RTC_OUT, I2C2_SMBA Additional: PB2, WKUP3
PA13	B1	I/O	5VT	Default: SWDIO Alternate: LPUART0_RX, I2C0_SCL, USART0_TX, SPI0_IO2, SPI0_NSS, EVENTOUT, LPUART1_RX Additional: PA13
PA14	A1	I/O	5VT	Default: SWCLK Alternate: LPUART0_TX, USART1_TX, I2C0_SDA, USART0_RX, SPI0_IO3, SPI1_NSS, I2S1_WS, EVENTOUT, LPUART1_TX Additional: PA14
PA15	C1	I/O	5VT	Default: PA15 Alternate: SPI1_NSS, I2S1_WS, TIMER1_CH0, TIMER1_ETI, SPI0_NSS, USART1_RX, EVENTOUT, I2C1_SMBA
PB3	A2	I/O	5VT	Default: PB3 Alternate: UART4_TX(3), SPI1_SCK, I2S1_CK, TIMER1_CH1, SPI0_SCK, USART0_RTS, USART0_DE, EVENTOUT, LPTIMER0_IN1, I2C2_SCL, I2C1_SCL,

GD32L235Ex WLCSP25				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				TIMER0_CH1 Additional: CMP1_IM6
PB4	B2	I/O	5VT	Default: PB4 Alternate: UART4_RX(3), SPI1_MISO, TIMER2_CH0, SPI0_MISO, USART0_CTS, EVENTOUT, I2C2_SDA, I2C1_SDA, TIMER11_CH0 Additional: CMP1_IP1
PB5	A3	I/O	5VT	Default: PB5 Alternate: LPTIMER0_IN0, I2C0_SMBA, SPI1_MOSI, I2S1_SD, SPI0_MOSI, USART0_CK, CMP1_OUT, EVENTOUT, TIMER40_BRKIN(3), TIMER2_CH1 Additional: CMP1_IP2, WKUP4
PB7	C2	I/O	5VT	Default: PB7 Alternate: I2C1_SDA, I2C0_SDA, USART0_RX, SPI0_IO3, EVENTOUT, SPI1_MOSI, I2S1_SD, LPTIMER0_IN1, LPUART1_TX, CK_OUT Additional: CMP1_IP4
BOOT0-PD3	B3	I/O	5VT	Default: BOOT0 Alternate: USART1_CTS, SPI1_MISO, I2S1_MCK, TIMER0_CH1_ON, UART4_RX(3), EVENTOUT Additional: PD3
VSS	A4	P	-	Default: VSS
VDD	A5	P	-	Default: VDD

Note:

(1) Type: I = input, O = output, A = analog, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Functions are available on GD32L235EB devices only.

2.6.9. GD32L235xx pin alternate functions

Table 2-12. Port A alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11
PA0		TIMER1_CH0/TIMER1_ETI	LPTIMER0_OUT			SPI1_SCK/I2S1_CK	CMP0_OUT	USART1_CTS	UART3_TX	EVENTOUT		CAN_RX
PA1		TIMER1_CH1		SEG0(2)	I2C0_SMBA	SPI0_SCK		USART1_RTS/USART1_DE	UART3_RX	EVENTOUT	TIMER14_CH0_ON	CAN_TX
PA2	SPI0_MOSI	TIMER1_CH2	TIMER8_CH0	SEG1(2)		SPI0_IO2	CMP1_OUT	USART1_TX	LPUART0_TX	EVENTOUT	TIMER14_CH0	
PA3	SPI1_MISO/I2S1_MCK	TIMER1_CH3	TIMER8_CH1	SEG2(2)		SPI0_IO3		USART1_RX	LPUART0_RX	EVENTOUT	TIMER14_CH1	
PA4	SPI1_MOSI/I2S1_SD	TIMER40_CH1(1)	LPTIMER0_OUT			SPI0_NSS	SPI1_NSS/I2S1_WS	USART1_CK	LPTIMER1_OUT	EVENTOUT	TIMER8_CH0	CAN_RX
PA5		TIMER1_CH0/TIMER1_ETI	LPTIMER0_ETI0			SPI0_SCK			LPTIMER1_ETI0	EVENTOUT	TIMER40_CH0(1)	CAN_TX
PA6	TIMER0_BRKIN	TIMER2_CH0	LPTIMER0_IN0	SEG3(2)	I2C2_SDA	SPI0_MISO	CMP0_OUT	TIMER11_CH0	LPUART0_CTS	EVENTOUT	TIMER40_CH0(1)	I2C1_SDA
PA7	TIMER0_CH0_ON	TIMER2_CH1	LPTIMER0_ETI0	SEG4(2)	I2C2_SCL	SPI0_MOSI	CMP1_OUT	TIMER11_CH1	TIMER11_CH0	EVENTOUT	TIMER8_CH0	I2C1_SCL
PA8	CK_OUT	TIMER0_CH0	LPTIMER0_OUT	COM0(2)	I2C2_SMBA	SPI1_NSS/I2S1_WS	LPTIMER1_OUT	USART0_CK	CTC_SYNC	EVENTOUT	I2C1_SMBA	I2C2_SCL
PA9	CK_OUT	TIMER0_CH1	LPTIMER0_IN1	COM1(2)	I2C0_SCL	SPI1_MISO	TIMER14_BRKIN	USART0_TX		EVENTOUT	I2C1_SCL	I2C2_SMBA
PA10		TIMER0_CH2		COM2(2)	I2C0_SDA	SPI1_MOSI/I2S1_SD		USART0_RX		EVENTOUT	I2C1_SDA	
PA11		TIMER0_CH3	TIMER0_BRKIN		I2C1_SCL	SPI0_MISO	CMP0_OUT	USART0_CTS	CAN_RX	EVENTOUT	LPUART1_RTS/LPUART1_DE	
PA12		TIMER0_ETI			I2C1_SDA	SPI0_MOSI	CMP1_OUT	USART0_RTS/USART0_DE	CAN_TX	EVENTOUT	LPUART1_CTS	
PA13	SWDIO		LPUART0_RX		I2C0_SCL	SPI0_IO2	SPI0_NSS	USART0_TX		EVENTOUT	LPUART1_RX	
PA14	SWCLK		LPUART0_TX		I2C0_SDA	SPI0_IO3	SPI1_NSS/I2S1_WS	USART0_RX	USART1_TX	EVENTOUT	LPUART1_TX	
PA15		TIMER1_CH0/TIMER1_ETI		SEG17(2)	I2C1_SMBA	SPI0_NSS	SPI1_NSS/I2S1_WS	USART1_RX		EVENTOUT		

Table 2-13. Port B alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11
PB0	LPTIMER1_IN1	TIMER2_CH2	LPTIMER0_OUT	SEG5(2)	UART4_TX(1)	SPI0_NSS	CMP0_OUT	LPUART1_CTS		EVENTOUT		TIMER0_CH1_ON
PB1	LPTIMER1_IN0	TIMER2_CH3	LPTIMER0_IN0	SEG6(2)	UART4_RX(1)			LPUART1_RTS/LPUART1_DE	LPUART0_RTS/LPUART0_DE	EVENTOUT	TIMER8_CH0	TIMER0_CH2_ON
PB2	RTC_OUT		LPTIMER0_OUT		I2C2_SMBA	SPI1_MISO/I2S1_MCK				EVENTOUT		
PB3		TIMER1_CH1	LPTIMER0_IN1	SEG7(2)	I2C2_SCL	SPI0_SCK	SPI1_SCK/I2S1_CK	USART0_RTS/USART0_DE	UART4_TX(1)	EVENTOUT	I2C1_SCL	TIMER0_CH1

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11
PB4		TIMER2_CH0		SEG8(2)	I2C2_SDA	SPI0_MISO	SPI1_MISO	USART0_CTS	UART4_RX(1)	EVENTOUT	I2C1_SDA	TIMER11_CH0
PB5		TIMER2_CH1	LPTIMER0_IN0	SEG9(2)	I2C0_SMBA	SPI0_MOSI	SPI1_MOSI/I2S1_SD	USART0_CK	CMP1_OUT	EVENTOUT		TIMER40_BRKIN(1)
PB6		TIMER0_CH2	LPTIMER0_ETI0		I2C0_SCL	SPI0_IO2	SPI1_MISO	USART0_TX	I2C1_SCL	EVENTOUT	LPUART1_RX	TIMER40_CH0_ON(1)
PB7	CK_OUT	LPTIMER0_IN1			I2C0_SDA	SPI0_IO3	SPI1_MOSI/I2S1_SD	USART0_RX	I2C1_SDA	EVENTOUT	LPUART1_TX	
PB8			TIMER14_BRKIN	SEG16(2)	I2C0_SCL	SPI1_SCK/I2S1_CK	CMP0_OUT	CAN_RX(3)	I2C1_SCL	EVENTOUT		TIMER40_CH0(1)
PB9		TIMER11_CH0		COM3(2)	I2C0_SDA	SPI1_NSS/I2S1_WS	CMP1_OUT	CAN_TX(3)	I2C1_SDA	EVENTOUT		TIMER40_CH1(1)
PB10		TIMER1_CH2		SEG10(2)	I2C1_SCL	SPI1_SCK/I2S1_CK	CMP0_OUT	LPUART0_TX	LPUART0_RX	EVENTOUT		
PB11		TIMER1_CH3		SEG11(2)	I2C1_SDA	SPI1_MOSI/I2S1_SD	CMP1_OUT	LPUART0_RX	LPUART0_TX	EVENTOUT		
PB12				SEG12(2)	I2C1_SMBA		SPI1_NSS/I2S1_WS		LPUART0_RTS/LPUART0_DE	EVENTOUT	TIMER14_BRKIN	TIMER0_BRKIN
PB13	CK_OUT	TIMER8_CH0		SEG13(2)	I2C1_SCL		SPI1_SCK/I2S1_CK		LPUART0_CTS	EVENTOUT	TIMER14_CH0_ON	TIMER0_CH0_ON
PB14	RTC_OUT	TIMER8_CH1	TIMER11_CH0	SEG14(2)	I2C1_SDA		SPI1_MISO		LPUART0_RTS/LPUART0_DE	EVENTOUT	TIMER14_CH0	TIMER0_CH1_ON
PB15	TIMER14_CH0_ON		TIMER11_CH1	SEG15(2)			SPI1_MOSI/I2S1_SD			EVENTOUT	TIMER14_CH1	TIMER0_CH2_ON

Table 2-14. Port C alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11
PC0		LPTIMER1_IN0	LPTIMER0_IN0	SEG18(2)	I2C2_SCL			LPUART1_TX	LPUART0_RX	EVENTOUT		
PC1	TIMER14_CH0	LPTIMER1_IN1	LPTIMER0_OUT	SEG19(2)	I2C2_SDA			LPUART1_RX	LPUART0_TX	EVENTOUT		
PC2	TIMER14_CH1		LPTIMER0_IN1	SEG20(2)		SPI1_MISO	I2S1_MCK			EVENTOUT		
PC3		LPTIMER1_ETI0	LPTIMER0_ETI0	SEG21(2)		SPI1_MOSI/I2S1_SD				EVENTOUT		
PC4		TIMER1_CH0/TIMER1_ETI		SEG22(2)	CAN_RX(2)			USART0_TX	LPUART0_TX	EVENTOUT		
PC5		TIMER1_CH1		SEG23(2)	CAN_TX(2)			USART0_RX	LPUART0_RX	EVENTOUT		
PC6		TIMER2_CH0	TIMER11_CH0	SEG24(2)		I2S1_MCK		LPUART1_TX		EVENTOUT	TIMER1_CH2	
PC7		TIMER2_CH1	TIMER11_CH1	SEG25(2)				LPUART1_RX		EVENTOUT	TIMER1_CH3	
PC8		TIMER2_CH2	TIMER0_CH0	SEG26(2)	I2C2_SDA			LPUART1_CTS		EVENTOUT		
PC9		TIMER2_CH3	TIMER0_CH1	SEG27(2)	I2C2_SCL	I2C2_SDA		LPUART1_RTS/LPUART1_DE		EVENTOUT		
PC10			TIMER0_CH2	SEG28/COM4(2)		SPI1_SCK/I2S1_C		UART3_TX	LPUART0_TX	EVENTOUT		

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11
						K						
PC11			TIMER0_CH3	SEG29/COM5(2)		SPI1_MISO		UART3_RX	LPUART0_RX	EVENTOUT		
PC12		LPTIMER0_IN0		SEG30/COM6(2)		SPI1_MOSI/I2S1_SD		UART4_TX(1)		EVENTOUT	TIMER8_CH0	
PC13			TIMER0_BRKIN							EVENTOUT		
PC14			TIMER0_BRKIN							EVENTOUT		
PC15		TIMER14_BRKIN								EVENTOUT		

Table 2-15. Port D alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11
PD0		TIMER8_CH0	LPTIMER0_OUT		CAN_RX(2)		SPI1_NSS/I2S1_WS	USART1_CK	CTC_SYNC	EVENTOUT		TIMER40_CH0(1)
PD1					CAN_TX(2)	SPI1_MISO	SPI1_SCK/I2S1_CK	USART1_CTS		EVENTOUT	TIMER11_CH0	TIMER40_CH1(1)
PD2		TIMER2_ETI	TIMER0_CH0_ON	SEG31/COM7(2)				UART4_RX(1)	LPUART0_RTS/LPUART0_DE	EVENTOUT		
PD3			TIMER0_CH1_ON			SPI1_MISO	I2S1_MCK	USART1_CTS	UART4_TX(1)	EVENTOUT		
PD4			TIMER0_CH2_ON	SEG28(2)		SPI1_MOSI/I2S1_SD		USART1_RTS/USART1_DE		EVENTOUT		
PD5			TIMER0_BRKIN	SEG29(2)		SPI0_MISO		USART1_TX		EVENTOUT		
PD6		LPTIMER1_OUT	LPTIMER0_IN1			SPI0_MOSI		USART1_RX		EVENTOUT		
PD8		LPTIMER0_OUT	LPTIMER0_ETI0	SEG30(2)		SPI0_SCK			LPUART0_TX	EVENTOUT		
PD9		TIMER0_BRKIN	LPTIMER0_IN0	SEG31(2)		SPI0_NSS			LPUART0_RX	EVENTOUT		

Table 2-16. Port F alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11
PF0	CK_OUT	LPTIMER1_OUT				SPI1_NSS/I2S1_WS				EVENTOUT	TIMER8_CH0	TIMER0_CH0
PF1	TIMER14_CH0_ON					SPI1_SCK/I2S1_CK				EVENTOUT		

Note:

(1) Functions are available on GD32L235xB devices only.

(2) Functions are available on GD32L235Rx devices only.

(3) Functions are available on GD32L235Rx/Cx devices only.

3. Functional description

3.1. Arm® Cortex®-M23 core

The Cortex-M23 processor is an energy-efficient processor with a very low gate count. It is intended to be used for microcontroller and deeply embedded applications that require an area-optimized processor. The processor is highly configurable enabling a wide range of implementations from those requiring memory protection and powerful trace technology to cost sensitive devices requiring minimal area, while delivering outstanding computational performance and an advanced system response to interrupts.

32-bit ARM® Cortex®-M23 processor core

- Up to 64 MHz operation frequency.
- Single-cycle multiplication and hardware divider.
- Ultra-low power, energy-efficient operation.
- Excellent code density.
- Integrated Nested Vectored Interrupt Controller (NVIC).
- 24-bit SysTick timer.

The Cortex®-M23 processor is based on the ARMv8-M architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M23:

- Internal Bus Matrix connected with AHB master, Serial Wire Debug Port and Single-cycle IO port.
- Nested Vectored Interrupt Controller (NVIC).
- Breakpoint Unit(BPU).
- Data Watchpoint and Trace (DWT).
- Serial Wire Debug Port.

3.2. Embedded memory

- Up to 128 Kbytes of Flash memory.
- Up to 24 Kbytes of SRAM with hardware parity checking.
- Flash ECC check supported.

128 Kbytes of inner Flash memory, and 24 Kbytes of inner SRAM at most is available for storing programs and data, and Flash is accessed (read) at CPU clock speed with 0~2 wait states. ***Table 2-3. GD32L235xx memory map*** shows the memory map of the GD32L235xx series of devices, including code, SRAM, peripheral, and other pre-defined regions.

3.3. Clock, reset and supply management

- Internal 16 MHz factory-trimmed RC and external 4 to 48 MHz crystal oscillator.
- Internal 48 MHz factory-trimmed RC.
- Internal 32 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator.
- Integrated system clock PLL.
- 1.71 to 3.63 V application supply and I/Os.
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD).

The Clock Control Unit (CCTL) provides a range of oscillator and clock functions. These include speed internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and two APB domains. The maximum frequency of the AHB, APB2 and APB1 domains is 64 MHz/64 MHz/32 MHz. See ***Figure 2-10. GD32L235xx clock tree*** for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from 1.56 V and down to 1.48V. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- V_{DD} range: 1.71 to 3.63 V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SS} is 0 V.
- V_{DDA} range: 1.71 to 3.63 V, external analog power supplies for ADC, reset blocks, RCs and PLL.
- V_{BAT} range: 1.71 to 3.63 V, power supply for RTC unit, LXTAL oscillator, BPOR, and two pads, including PC13 to PC15 when V_{DD} is not present.

3.4. Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main Flash memory (default).
- Boot from system memory.
- Boot from on-chip SRAM.

In default condition, boot from main Flash memory is selected. The boot loader is located in the internal boot ROM memory (system memory). It is used to reprogram the Flash memory by using USART0 (PA9 and PA10) or USART1 (PA2 and PA3) or USBD (PA11 and PA12).

3.5. Power saving modes

The MCU supports six kinds of power saving modes to achieve even lower power consumption. They are Run, Sleep, Deep-sleep, Deep-sleep 1, Deep-sleep 2 and Standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Run mode**

  After system reset/ power reset or wakeup from standby mode, the MCU enters Run mode. And the NPLDO (normal power LDO) works in 1.1V mode.

- **Sleep mode**

  The Sleep mode is corresponding to the SLEEPING mode of the Cortex®-M23. In Sleep mode, only clock of Cortex®-M23 is off. To enter the Sleep mode, it is only necessary to clear the SLEEPDEEP bit in the Cortex®-M23 System Control Register, and execute a WFI or WFE instruction. If the Sleep mode is entered by executing a WFI instruction, any interrupt can wake up the system. If it is entered by executing a WFE instruction, any wakeup event can wake up the system (If SEVONPEND is 1, any interrupt can wake up the system, refer to Cortex®-M23 Technical Reference Manual). The mode offers the lowest wakeup time as no time is wasted in interrupt entry or exit.

- **Deep-sleep mode**

  The Deep-sleep mode is based on the SLEEPDEEP mode of the Cortex®-M23. In Deep-sleep mode, all clocks in the V_{CORE} domain are off, and all of IRC16M, IRC48M, HXTAL and PLLs are disabled. The contents of SRAM and registers are preserved. The NPLDO can operate normally or in low driver mode depending on the LDNPDSP bit in the PMU_CTL0 register. Before entering the Deep-sleep mode, it is necessary to set the SLEEPDEEP bit in the Cortex®-M23 System Control Register, and set LPMOD bits to “00” in the PMU_CTL0 register. Then, the device enters the Deep-sleep mode after a WFI or WFE instruction is executed. If the Deep-sleep mode is entered by executing a WFI instruction, any interrupt from EXTI lines can wake up the system. If it is entered by executing a WFE instruction, any wakeup event from EXTI lines can wake up the system (If SEVONPEND is 1, any interrupt from EXTI lines can wake up the system, refer to Cortex®-M23 Technical Reference Manual). When exiting the Deep-sleep mode, the IRC16M is selected as the system clock. Notice that an additional wakeup delay will be incurred if the LDO operates in low driver mode.

- **Deep-sleep 1 mode**

  The Deep-sleep 1 mode is based on the SLEEPDEEP mode of the Cortex®-M23. In Deep-sleep 1 mode, all clocks in the V_{CORE} domain are off, and all of IRC16M, IRC48M, HXTAL and PLLs are disabled. The LPLDO (low power LDO) can operate normally instead of NPLDO. Before entering the Deep-sleep 1 mode, it is necessary to set the SLEEPDEEP bit in the Cortex®-M23 System Control Register, set LPMOD bits to “01” in the PMU_CTL0 register. Then, the device enters the Deep-sleep 1 mode after a WFI or WFE instruction is executed. If the Deep-sleep 1 mode is entered by executing a WFI instruction, any interrupt from EXTI lines can wake up the system. If it is entered by executing a WFE instruction, any wakeup event from EXTI lines can wake up the system (If SEVONPEND is 1, any interrupt from EXTI lines can wake up the system, refer to

Cortex®-M23 Technical Reference Manual). When exiting the Deep-sleep 1 mode, the IRC16M is selected as the system clock. Waking up from Deep-sleep 1 mode needs an additional delay to wakeup NPLDO.

- **Deep-sleep 2 mode**

  The Deep-sleep 2 mode is based on the SLEEPDEEP mode of the Cortex®-M23. In Deep-sleep 2 mode, all clocks in the V_{CORE} domain are off, and all of IRC16M, IRC48M, HXTAL and PLLs are disabled. The power of COREOFF0 / SRAM1 domain is cut off and the contents of COREOFF0 / SRAM1 domain are lost. The LPLDO can operate normally instead of NPLDO. Before entering the Deep-sleep 2 mode, it is necessary to set the SLEEPDEEP bit in the Cortex®-M23 System Control Register, set LPMOD bits to “10” in the PMU_CTL0 register. Then, the device enters the Deep-sleep 2 mode after a WFI or WFE instruction is executed. If the Deep-sleep 2 mode is entered by executing a WFI instruction, any interrupt from EXTI lines can wake up the system. If it is entered by executing a WFE instruction, any wakeup event from EXTI lines can wake up the system (If SEVONPEND is 1, any interrupt from EXTI lines can wake up the system, refer to Cortex®-M23 Technical Reference Manual). When exiting the Deep-sleep 2 mode, the IRC16M is selected as the system clock. Waking up from Deep-sleep 2 mode needs an additional delay to wakeup NPLDO.

- **Standby mode**

  The Standby mode is based on the SLEEPDEEP mode of the Cortex®-M23 too. In Standby mode, the whole V_{CORE} domain is power off, the NPLDO / LPLDO is shut down, and all of IRC16M, IRC48M, HXTAL and PLLs are disabled. Before entering the Standby mode, it is necessary to set the LPMOD bits to “11” in the PMU_CTL0 register, and clear WUF bit in the PMU_CS register, and set the SLEEPDEEP bit in the Cortex®-M23 System Control Register. Then, the device enters the Standby mode after a WFI or WFE instruction is executed, and the STBF status flag in the PMU_CS register indicates that the MCU has been in Standby mode. There are four wakeup sources for the Standby mode, including the external reset from NRST pin, the RTC alarm / time stamp / tamper / auto wakeup events, the FWDGT reset, and the rising edge on WKUP pins. The Standby mode achieves the lowest power consumption, but spends longest time to wake up. Besides, the contents of SRAM and registers in V_{CORE} power domain are lost in Standby mode. When exiting from the Standby mode, a power-on reset occurs and the Cortex®-M23 will execute instruction code from the 0x00000000 address.

3.6. Clock trim controller (CTC)

- Two external reference signal source: GPIO, LXTAL clock.
- Provide software reference sync pulse.
- Automatically trimmed by hardware without any software action.
- 16 bits trim counter with reference signal source capture and reload.
- 8 bits clock trim base value to frequency evaluation and automatically trim.

The Clock Trim Controller (CTC) is used to trim internal 48MHz RC oscillator (IRC48M) automatically by hardware. The CTC unit trim the frequency of the IRC48M based on an external accurate reference signal source. It can automatically adjust the trim value to

provide a precise IRC48M clock.

3.7. General-purpose inputs/outputs (GPIOs)

- Up to 59 fast GPIOs, all mappable on 16 external interrupt lines.
- Analog input/output configurable.
- Alternate function input/output configurable.

There are up to 59 general purpose I/O pins (GPIO) in GD32L235xx, named PA0 ~ PA15, PB0 ~ PB15, PC0 ~ PC15, PD0 ~ PD6, PD8 ~ PD9, PF0 ~ PF1 to implement logic input/output functions. Each GPIO port has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt/Event Controller Unit (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins.

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), input, peripheral alternate function or analog mode. Most of the GPIO pins are shared with digital or analog alternate functions.

3.8. CRC calculation unit (CRC)

- Supports 7/8/16/32-bit data input.
- For 7(8)/16/32 bit input data length, the calculation cycles are 1/2/4 AHB clock cycles.
- Free 8-bit register is unrelated to calculation and can be used for any other goals by any other peripheral devices.
- User configurable polynomial value and size.

A cyclic redundancy check (CRC) is an error-detecting code commonly used in digital networks and storage devices to detect accidental changes to raw data. This CRC calculation unit can be used to calculate 7/8/16/32 bit CRC code within user configurable polynomial.

3.9. True Random number generator (TRNG)

- About 40 periods of TRNG_CLK are needed between two consecutive random numbers.
- 32-bit random value seed is generated from analog noise, so the random number is a true random number.

The true random number generator (TRNG) module can generate a 32-bit random value by using continuous analog noise.

3.10. Direct memory access controller (DMA)

- 7 channels for DMA controller.
- DMA request from DMAMUX: peripherals (Timers, ADC, DAC, SPIs, I2S, I2Cs, USARTs, CAU and LPUARTs) and request generator.

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby increasing system performance by off-loading the MCU from copying large amounts of data and avoiding frequent interrupts to serve peripherals needing more data or having available data. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory.

Each channel is connected to flexible hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

3.11. DMA request multiplexer (DMAMUX)

- 7 channels for DMAMUX request multiplexer.
- 4 channels for DMAMUX request generator.
- Support 21 trigger inputs and 21 synchronization inputs.

DMAMUX is a transmission scheduler for DMA requests. The DMAMUX request multiplexer is used for routing a DMA request line between the peripherals / generated DMA request (from the DMAMUX request generator) and the DMA controller. Each DMAMUX request multiplexer channel selects a unique DMA request line, unconditionally or synchronously with events from its DMAMUX synchronization inputs. The DMA request is pending until it is served by the DMA controller which generates a DMA acknowledge signal (the DMA request signal is de-asserted).

3.12. Analog to digital converter (ADC)

- 12-bit SAR ADC's conversion rate is up to 1.067 MSPS.
- Hardware oversampling ratio adjustable from 2x to 256x improves resolution to 16-bit.
- Input voltage range: V_{SS}/V_{SSA} to V_{REFP}.
- Temperature sensor.
- Single-ended and differential input channels

A 12-bit multi-channel ADC is integrated in the device. It has a total of 20 multiplexed channels: up to 16 external channels, 1 channel for internal temperature sensor (V_{SENSE}), 1 channel for internal reference voltage (V_{REFINT}), 1 channel for external battery power supply (V_{BAT}), and 1 channel for SLCD voltage (V_{SLCD}). The input voltage range is between V_{SS}/V_{SSA} and V_{DD}/V_{DDA}. An on-chip hardware oversampling scheme improves performance while off-loading the related computational burden from the CPU. The analog watchdog allows the

application to detect whether the input voltage goes outside the user-defined higher or lower thresholds. A configurable channel management block can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced use.

The ADC can be triggered from the events generated by the general level 0 timers (TIMERx, x=1, 2) and the general level 1 timers (TIMERx, x=8, 11) and the advanced TIMER0 and the general level 3 TIMER14 with internal connection. The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage in a digital value.

To ensure a high accuracy on ADC and DAC, the ADC/DAC independent external reference voltage should be connected to VREFP pins. According to the different packages, VREFP pin can be connected to VDDA pin, or external reference voltage. For packages without VREFP pin, VREFP is internally connected to VDDA.

3.13. Digital to analog converter (DAC)

- One12-bit DAC with one output channel.
- 8-bit or 12-bit mode in conjunction with the DMA controller.
- Support references from internal precision reference or external VREFP pin.

The 12-bit buffered DAC is used to generate variable analog outputs. The DAC channels can be triggered by the timer or EXTI with DMA support. The maximum output value of the DAC is V_{REFP}.

3.14. Real time clock (RTC)

- Independent binary-coded decimal (BCD) format timer/counter with five 32-bit backup registers.
- Calendar with sub-second, second, minute, hour, week day, day, month and year automatically correction.
- Alarm function with wake up from deep-sleep and standby mode capability.
- On-the-fly correction for synchronization with master clock. Digital calibration with 0.95 ppm resolution for compensation of quartz crystal inaccuracy.

The real time clock is an independent timer which provides a set of continuously running counters in backup registers to provide a real calendar function, and provides an alarm interrupt or an expected interrupt. It is not reset by a system or power reset, or when the device wakes up from standby mode. In the RTC unit, there are two prescalers used for implementing the calendar and other functions. One prescaler is a 7-bit asynchronous prescaler and the other is a 15-bit synchronous prescaler.

3.15. Timers and PWM generation

- Up to six 16-bit general timers (TIMER1, TIMER2, TIMER8, TIMER11, TIMER14,

TIMER40), two 16-bit basic timers (TIMER5, TIMER6), one 16-bit advanced timer (TIMER0) and two 16-bit low power timers (LPTIMER0, LPTIMER1).

- Up to 4 independent channels of PWM, output compare or input capture for each general timer and external trigger input.
- Encoder interface controller with two inputs using quadrature decoder.
- 24-bit SysTick timers down counter.
- 2 watchdog timers (free watchdog timer and window watchdog timer).

The LPTIMER0 and LPTIMER1 are 16-bit timers and it is able to keep running in all power modes except for Standby mode with its diversity of clock sources. The LPTIMER provides one PWM out and also supports an encoder interface with two inputs using quadrature decoder.

The advanced timer (TIMER0) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general timer. The 4 independent channels can be used for input capture, output compare, PWM generation (edge- or center- aligned counting modes) and single pulse mode output. If configured as a general 16-bit timer, it has the same functions as the TIMERx timer. It can be synchronized with external signals or to interconnect with other general timers together which have the same architecture and features.

The general timer can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TIMER1 and TIMER2 are based on a 16-bit auto-reload up/down/center-aligned counter and a 16-bit prescaler. TIMER8, TIMER11, TIMER14 and TIMER40 are based on a 16-bit auto-reload up counter and a 16-bit prescaler. The general timer also supports an encoder interface with two inputs using quadrature decoder.

The basic timer TIMER5 and TIMER6, are mainly used as a simple 16-bit time base.

The GD32L235xx have two watchdog peripherals, free watchdog timer and window watchdog timer. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-stage prescaler. It is clocked from an independent 32 KHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wakeup interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. The features are shown below:

- A 24-bit down counter.
- Auto reload capability.
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source.

3.16. Universal synchronous/asynchronous receiver transmitter (USART/UART)

- Maximum speed up to 8 MBits/s for USART0.
- Maximum speed up to 4 MBits/s for USART1, UART3 and UART4.
- Supports both asynchronous and clocked synchronous serial communication modes.
- IrDA SIR encoder and decoder support.
- LIN break generation and detection.
- ISO 7816-3 compliant smart card interface.
- Dual clock domain.
- Wake up from Deep-sleep mode.

The USART (USART0, USART1) and UART (UART3, UART4) are used to translate data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART/UART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART/UART transmitter and receiver. The USART/UART also supports DMA function for high speed data communication.

3.17. Universal asynchronous receiver transmitter (LPUART)

- Maximum speed up to 10 MBits/s.
- Supports asynchronous serial communication modes.
- Supports hardware modem operations (CTS/RTS) and RS485 drive.
- Dual clock domain.
- Wake up from Deep-sleep mode.

The Low-power universal Asynchronous Receiver/Transmitter (LPUART) provides a flexible serial data exchange interface with a limited power consumption. LPUART can perform asynchronous serial communication even with low power consumption. Data frames can be transferred in full duplex or half duplex mode, asynchronously through this interface. A programmable baud rate generator divides the clock to produces a dedicated wide range baudrate clock for the LPUART transmitter and receiver.

3.18. Inter-integrated circuit (I2C)

- Support both master and slave mode with a frequency up to 1 MHz (Fast mode plus).

- Provide arbitration function, optional PEC (packet error checking) generation and checking.
- Supports 7-bit and 10-bit addressing mode and general call addressing mode.
- Multiple 7-bit slave addresses (2 addresses with configurable mask).
- SMBus 3.0 and PMBus 1.3 compatible.
- Wakeup from Deep-sleep / Deep-sleep1 / Deep-sleep2 mode on I2C address match.

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two-line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides different data transfer rates: up to 100 KHz in standard mode, up to 400 KHz in the fast mode and up to 1 MHz in the fast mode plus. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

3.19. Serial peripheral interface (SPI)

- Support both master and slave mode.
- Hardware CRC calculation and transmit automatic CRC error checking.
- Separate transmit and receive 32-bit FIFO with DMA capability (only in SPI0).
- Data frame size can be 4 to 16 bits (only in SPI0).
- Quad-SPI configuration available in master mode (only in SPI0).

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). All SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking. Quad-SPI master mode is also supported in SPI0.

3.20. Inter-IC sound (I2S)

- Sampling frequency from 8 KHz to 192 KHz.
- Support either master or slave mode.

The Inter-IC sound (I2S) bus provides a standard communication interface for digital audio applications by 4-wire serial lines. GD32L235xx contain an I2S-bus interface that can be operated with 16/32-bit resolution in master or slave mode, pin multiplexed with SPI1. The audio sampling frequency from 8 KHz to 192 KHz is supported.

3.21. Cryptographic acceleration Unit (CAU)

- Supports DES, TDES or AES (128, 192, or 256) algorithms.
- DES / TDES supports Electronic codebook (ECB) or Cipher block chaining (CBC) mode.

- AES supports 128bits-key, 192bits-key or 256 bits-key.
- AES supports Electronic codebook (ECB), Cipher block chaining (CBC) mode, Counter mode (CTR) mode, Galois / counter mode (GCM), Galois message authentication code mode (GMAC), Counter with CBC-MAC (CCM), Cipher Feedback mode (CFB) and Output Feedback mode (OFB).
- DMA transfer for incoming and outgoing data is supported.

The Cryptographic Acceleration Unit supports acceleration of DES, TDES or AES (128, 192, or 256) algorithms. The DES / TDES supports Electronic codebook (ECB) or Cipher block chaining (CBC) mode. The AES supports Electronic codebook (ECB), Cipher block chaining (CBC) mode, Counter mode (CTR) mode, Galois/counter mode (GCM), Galois message authentication code mode (GMAC), Counter with CBC-MAC (CCM), Cipher Feedback mode (CFB) and Output Feedback mode (OFB).

3.22. Segment LCD controller (SLCD)

- Configurable frame frequency.
- Blinking of individual segments or all segments.
- Supports Static, 1/2, 1/3, 1/4, 1/6 and 1/8 duty.
- Supports 1/2, 1/3 and 1/4 bias.
- Double buffer up to 8x32 bits registers to store SLCD_DATAx.
- The contrast can also be adjusted by configuring dead time.

The SLCD controller directly drives LCD displays by creating the AC segment and common voltage signals automatically. It can drive the monochrome passive liquid crystal display (LCD) which composed of a plurality of segments (pixels or complete symbols) that can be converted to visible or invisible. The SLCD controller can support up to 32 segments and 8 commons.

3.23. Comparators (CMP)

- Two fast rail-to-rail low-power comparators with software configurable.
- Programmable reference voltage (internal or external I/O).

Two Comparators (CMP) is implemented within the device. It can wake up from deep-sleep mode to generate interrupts and also can be combined as a window comparator. The internal voltage reference is also connected to ADC_IN17 input channel of the ADC.

3.24. Controller area network (CAN)

- CAN2.0B interface with communication frequency up to 1 Mbit/s
- Internal main PLL for CAN CLK compliantly

Controller area network (CAN) is a method for enabling serial communication in field bus. The CAN protocol has been used extensively in industrial automation and automotive

applications. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. The CAN has three mailboxes for transmission and two FIFOs of three message deep for reception. It also provides 28 scalable/configurable identifier filter banks for selecting the incoming messages needed and discarding the others.

3.25. Universal serial bus full-speed device interface (USBD)

- USB 2.0 full-speed device controller.
- Support USB 2.0 Link Power Management.
- Dedicated 512-byte SRAM used for data packet buffer.
- Support embedded pull-up on the DP line.
- Integrated USB PHY.

The Universal Serial Bus full-speed device interface (USBD) module contains a full-speed internal USB PHY and no more external PHY chip is needed. USBD supports all the four types of transfer (control, bulk, interrupt and isochronous) defined in USB 2.0 protocol. USBD supports 8 USB bidirectional endpoints that can be individually configured.

3.26. Debug mode

- Serial wire debug port (SW-DP).

Debug capabilities can be accessed by a debug tool via Serial Wire (SW - Debug Port).

3.27. Package and operation temperature

- LQFP64 (GD32L235RxT6), LQFP64 (GD32L235RxT7), LQFP48 (GD32L235CxT6), LQFP48 (GD32L235CxT7), QFN48 (GD32L235CxO6), LQFP32 (GD32L235KxT6), QFN32 (GD32L235KxQ6), QFN32 (GD32L235KxQ7), QFN32 (GD32L235KxQ6P) and WLCPS25 (GD32L235ExY6).
- Operation temperature range: -40°C to +85°C (industrial level) for grade 6 devices, and -40°C to +105°C (industrial level) for grade 7 devices.

4 Electrical characteristics

To better understand this chapter, read the following before moving on to the rest of this chapter.

- T_A (Ambient temperature) tested condition.
- T_J (Junction temperature) tested condition.
- Value guaranteed by design, not 100% tested in production indicates that the value is derived from simulation of IC designers.
- Value guaranteed by characterization, not 100% tested in production indicates that the value is derived from random test.
- Value guaranteed by sample, not 100% tested in production indicates that the value is derived from a small number of sample tests.
- Guaranteed by characterization, the minimum and maximum values refer to random tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).
- Unless otherwise specified, all values given for V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C.
- If the value is not specially indicated, it means the value guaranteed by 100% tested in production.
- The devices will be damaged or work abnormally if the electrical parameters beyond the range of maximum and minimum values.

See the following table for some abbreviation terms and their descriptions in this chapter.

Table 4-1. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
CAN	Controller Area Network
DAC	Digital-to-Analog Converter
DMA	Direct Memory Access
GPIO	General Purpose Input/Output
PLL	Phase-Locked Loop
USB	Universal Serial Bus
SPI	Serial Peripheral Interface
SLCD	Segment LCD Controller

4.1 Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly beyond the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-2. Absolute maximum ratings (1)(2)(4)

Symbol	Parameter	Min	Max	Unit
V_{DD}	External voltage range	V_{SS} - 0.3	V_{SS} + 4.0	V
V_{DDA}	External analog supply voltage	V_{SSA} - 0.3	V_{SSA} + 4.0	V
V_{BAT}	External battery supply voltage	V_{SS} - 0.3	V_{SS} + 4.0	V
V_{IN}	Input voltage on 5V tolerant pin(3)	V_{SS} - 0.3	V_{DD} + 4.0	V
	Input voltage on other I/O	V_{SS} - 0.3	4.0	V
$\|\Delta V_{DDx}\|$	Variations between different VDD power pins	—	50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between different ground pins	—	50	mV
I_{IO}	Maximum current for GPIO pins	—	±20	mA
$\sum I_{IO}$	Maximum current sunk/sourced by all GPIO pin	—	100	
I_{DD}	Maximum current into each VDD pin	—	100	
I_{SS}	Maximum current into each VSS pin	—	100	
$\sum I_{DD}$	Total current into all VDD pins	—	140	
$\sum I_{SS}$	Total current into all VSS pins	—	140	
T_A	Operating temperature range for grade 6 device	-40	+85	°C
	Operating temperature range for grade 7 device	-40	+105	
P_D	Power dissipation at T_A = 85°C of LQFP64(5)	—	733	mW
	Power dissipation at T_A = 105°C of LQFP64(5)	—	367	
	Power dissipation at T_A = 85°C of QFN64(5)	—	1044	
	Power dissipation at T_A = 85°C of LQFP48(5)	—	574	
	Power dissipation at T_A = 105°C of LQFP48(5)	—	287	
	Power dissipation at T_A = 85°C of QFN48(5)	—	939	
	Power dissipation at T_A = 85°C of LQFP32(5)	—	724	
	Power dissipation at T_A = 85°C of QFN32(5)	—	940	
	Power dissipation at T_A = 105°C of QFN32(5)	—	470	
	Power dissipation at T_A = 85°C of WLCSP25(5)	—	570	
T_{STG}	Storage temperature range	-65	+150	°C
T_J	Maximum junction temperature	—	+125	°C

(1) Value guaranteed by design, not 100% tested in production.

(2) All main power and ground pins should be connected to an external power source within the allowable range.

(3) V_{IN} maximum value cannot exceed 5.5 V.

(4) It is recommended that V_{DD} and V_{DDA} are powered by the same source. The maximum difference between V_{DD} and V_{DDA} does not exceed 300 mV during power-up and operation.

(5) For grade 6 devices, the parameter of T_A=85°C, For grade 7 devices, the parameter of T_A=105°C.

4.2 Operating conditions characteristics

Table 4-3. DC operating conditions (1)

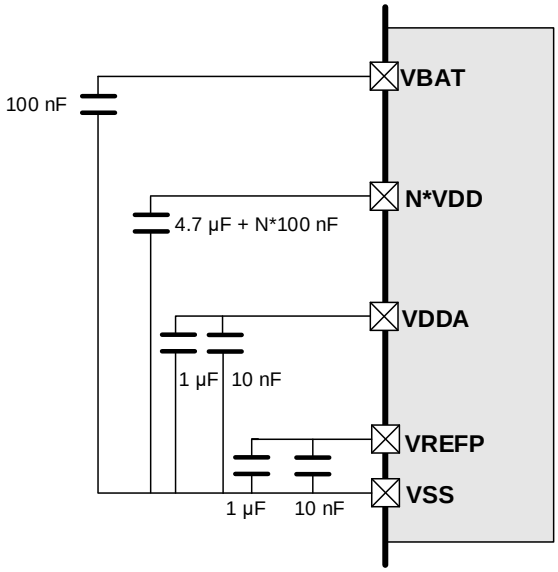
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD}	Supply voltage	—		1.71	3.3	3.63	V
V_{DDA}	Analog supply voltage	—		1.71	3.3	3.63	V
V_{BAT}(3)	Battery supply voltage	—		1.71 (2)	3.3	3.63	V
V_{CORE}	Core logic supply voltage powered by internal voltage regulator	NPLDO	LDOVS[1:0] =1x	—	1.1	—	V
		LPLDO		—	0.9	—	

(1) Value guaranteed by design, not 100% tested in production.

(2) In the application which V_{BAT} supply the backup domains, if the V_{BAT} voltage drops below the minimum value, when V_{DD} is powered on again, it is necessary to refresh the registers of backup domains and enable LXTAL again.

(3) When both V_{DD} and V_{BAT} are powered simultaneously, it is required that $V_{BAT} \leq V_{DD} + 0.3$ V.

Figure 4-1. Recommended power supply decoupling capacitors (1)



(1) All decoupling capacitors need to be as close as possible to the pins on the PCB board.

Table 4-4. Clock frequency (1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CPU}	Core clock frequency	—	—	64	MHz
f_{HCLK1}	AHB1 clock frequency	—	0	64	MHz
f_{APB1}	APB1 clock frequency	—	0	32	MHz
f_{APB2}	APB2 clock frequency	—	0	64	MHz

(1) Value guaranteed by design, not 100% tested in production.

Table 4-5. Operating conditions at Power up/ Power down (1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	—	0	∞	µs/V
	V_{DD} fall time rate		50	∞	
t_{VDDA}	V_{DDA} rise time rate	—	0	∞	
	V_{DDA} fall time rate		50	∞	

(1) Value guaranteed by design, not 100% tested in production.

Table 4-6. Start-up timings of Operating conditions (1)(2)(3)

Symbol	Parameter	Conditions	Typ	Unit
t_{ST}	Start-up time	Clock source from HXTAL=8MHz	1.62	ms
		Clock source from IRC16M	49.7	us

(1) Based on sample, not tested in production.

(2) After power-up, the start-up time is the time between the rising edge of NRST high and the first I/O instruction conversion in SystemInit function.

(3) PLL is off.

Table 4-7. Power saving mode wakeup timings characteristics (1)(2)

Symbol	Parameter	Typ	Unit
t_{Sleep}	Wakeup from Sleep mode	0.66	μs
$t_{Deep-sleep}$	Wakeup from Deep-sleep mode (NPLDO in normal driver mode)	1.50	
	Wakeup from Deep-sleep mode (NPLDO in low driver mode)	1.50	
	Wakeup from Deep-sleep 1 mode	5.53	
	Wakeup from Deep-sleep 2 mode	40.10	
$t_{Standby}$	Wakeup from Standby mode	53.06	

(1) Value guaranteed by sample, not 100% tested in production.

(2) The wakeup time is measured from the wakeup event to the point at which the application code reads the first instruction under the below conditions: V_{DD} = V_{DDA} = 3.3 V, IRC16M = System clock = 16MHz.

4.3 Power consumption

The power consumption is measured as described in ***Figure 4 2. Power consumption measurement diagram***. The current consumption values are derived from the tests powered by V_{DD} = V_{DDA} except BKP_ONLY mode, while the current is I_{SUM}. In BKP_ONLY mode, the RTC unit and LXTAL oscillator are powered by the V_{BAT}, while the current is I_{BAT}.

Figure 4-2. Power consumption measurement diagram

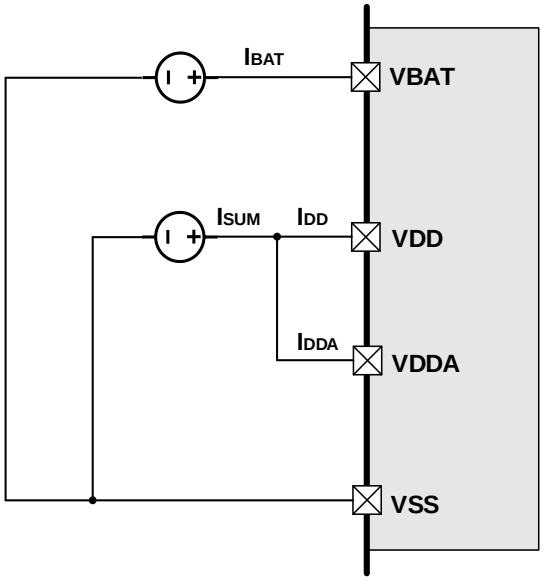


Table 4-8. Power consumption in Run mode[1][2][3][4]

Symbol	Description	Conditions				Typ				Max[5]				Unit
		Execute from	Peripherals	General	f_{HCLK1}	25°C	55°C	85°C	105°C	25°C	55°C	85°C	105°C	
I_{SUM}	Sum of supply current from VDD and VDDA (Run mode)	EFLASH	All disabled	HXTAL_bypass = 8 MHz, PLL on, System clock = f_{HCLK1}	64 MHz	3.72	3.74	3.75	3.77	3.90	3.93	3.94	3.97	mA
					48 MHz	2.97	2.98	2.99	3.02	3.12	3.13	3.14	3.17	
					36 MHz	2.41	2.41	2.43	2.45	2.52	2.53	2.54	2.58	
					24 MHz	1.85	1.85	1.86	1.88	1.93	1.94	1.95	1.98	
					16 MHz	1.47	1.47	1.48	1.50	1.53	1.54	1.55	1.59	
				IRC16M = 16 MHz, PLL off, System clock = 16 MHz	16 MHz	2.40	2.40	2.42	2.45	2.53	2.53	2.58	2.61	
					8 MHz	0.92	0.92	0.94	0.95	0.96	0.96	0.99	1.02	
					4 MHz	0.74	0.74	0.75	0.77	0.78	0.78	0.80	0.83	
					2 MHz	0.65	0.65	0.66	0.68	0.67	0.69	0.70	0.74	
					1 MHz	0.60	0.61	0.62	0.63	0.62	0.64	0.65	0.69	
			All enabled	HXTAL_bypass = 8 MHz, PLL on, System clock = f_{HCLK1}	64 MHz	12.37	12.41	12.46	12.50	12.97	13.02	13.07	13.13	
					48 MHz	9.54	9.59	9.61	9.65	9.97	10.04	10.06	10.11	
					36 MHz	6.31	6.32	6.33	6.36	6.60	6.63	6.64	6.67	
					24 MHz	5.45	5.47	5.49	5.52	5.71	5.72	5.74	5.78	
					16 MHz	4.03	4.05	4.07	4.11	4.21	4.23	4.25	4.30	
				IRC16M = 16 MHz, PLL off, System clock = 16 MHz	16 MHz	3.45	3.46	3.48	3.50	3.58	3.60	3.63	3.67	
					8 MHz	2.10	2.10	2.11	2.13	2.18	2.18	2.21	2.24	
					4 MHz	1.39	1.40	1.41	1.43	1.44	1.45	1.48	1.51	
					2 MHz	1.04	1.05	1.06	1.08	1.08	1.09	1.11	1.14	
					1 MHz	0.87	0.87	0.88	0.90	0.90	0.92	0.93	0.96	
		SRAM[6]	All disabled	HXTAL_bypass = 8 MHz, PLL	64 MHz	4.08	4.10	4.11	4.13	4.26	4.29	4.29	4.32	
					48 MHz	3.25	3.26	3.27	3.29	3.38	3.40	3.41	3.44	
					36 MHz	2.61	2.62	2.63	2.65	2.72	2.73	2.74	2.77	

Symbol	Description	Conditions				Typ				Max(5)				Unit
		Execute from	Peripherals	General	f_{HCLK1}	25°C	55°C	85°C	105°C	25°C	55°C	85°C	105°C	
				on, System clock = f_{HCLK1}	24 MHz	1.98	1.98	2.00	2.02	2.04	2.07	2.09	2.11	
					16 MHz	1.56	1.56	1.58	1.60	1.62	1.63	1.64	1.67	
				IRC16M = 16 MHz, PLL off, System clock = 16 MHz	16 MHz	1.25	1.26	1.27	1.28	1.31	1.32	1.33	1.36	
					8 MHz	0.91	0.91	0.92	0.94	0.95	0.96	0.97	1.00	
					4 MHz	0.73	0.74	0.74	0.76	0.77	0.78	0.79	0.82	
					2 MHz	0.65	0.65	0.66	0.67	0.68	0.69	0.70	0.73	
					1 MHz	0.60	0.60	0.61	0.63	0.63	0.64	0.65	0.69	
			All enabled	HXTAL_bypass = 8 MHz, PLL on, System clock = f_{HCLK1}	64 MHz	10.45	10.48	10.50	10.53	10.91	10.97	10.98	11.02	
					48 MHz	8.07	8.08	8.11	8.14	8.42	8.44	8.48	8.51	
					36 MHz	6.26	6.29	6.30	6.33	6.54	6.57	6.59	6.62	
					24 MHz	4.46	4.48	4.50	4.52	4.65	4.66	4.70	4.73	
					16 MHz	3.27	3.28	3.29	3.31	3.41	3.43	3.44	3.47	
				IRC16M = 16 MHz, PLL off, System clock = 16 MHz	16 MHz	3.56	3.56	3.58	3.60	3.71	3.72	3.74	3.77	
					8 MHz	2.13	2.14	2.15	2.17	2.23	2.23	2.24	2.27	
					4 MHz	1.42	1.42	1.43	1.45	1.48	1.49	1.50	1.52	
					2 MHz	1.06	1.06	1.07	1.09	1.11	1.12	1.12	1.15	
					1 MHz	0.88	0.88	0.89	0.91	0.92	0.93	0.94	0.97	

(1) Value guaranteed by characterization, not 100% tested in production.

(2) During power consumption test, GPIO needs to be configure as Analog Input mode.

(3) When the peripherals are enabled, APB2 clock = f_{HCLK1}, APB1 clock = f_{HCLK1} / 2.

(4) The Flash memory access time is adjusted with the correctly wait states number.

(5) V_{DD} = V_{DDA} = 3.63 V for values in Max columns.

(6) EFLASH power on in Run mode when executing from SRAM.

Table 4-9. Power consumption in Run mode with different codes(1)(2)(3)(4)

Symbol	Description	Conditions			Typ	Unit	Typ	Unit
		Execute from	General	Code				
I_{SUM}	Sum of supply current from VDD and VDDA (Run mode)	EFLASH	HXTAL_bypass = 8 MHz, PLL on, System clock = 64 MHz, f_{HCLK1} = 64 MHz	Coremark	5.88	mA	91.88	μA /MHz
				Dhrystone 2.1	5.68		88.75	
				While (1)(6)	3.72		58.13	
			IRC16M = 16 MHz, PLL off, System clock = 16 MHz, f_{HCLK1} = 16 MHz	Coremark	1.90		118.75	
				Dhrystone 2.1	1.96		122.50	
				While (1) (6)	2.40		150.00	
			IRC16M = 16 MHz, PLL off, System clock = 16 MHz, f_{HCLK1} = 2 MHz	Coremark	0.46		230.00	
				Dhrystone 2.1	0.49		245.00	
				While (1) (6)	0.65		325.00	
		SRAM(5)	HXTAL_bypass = 8 MHz, PLL on, System clock = 64 MHz, f_{HCLK1} = 64 MHz	Coremark	4.69		73.28	
				Dhrystone 2.1	4.66		72.81	
				While (1) (6)	4.08		63.75	
			IRC16M = 16 MHz, PLL off, System clock = 16 MHz, f_{HCLK1} = 16 MHz	Coremark	1.24		77.50	
				Dhrystone 2.1	1.30		81.25	
				While (1) (6)	1.25		78.13	
			IRC16M = 16 MHz, PLL off, System clock = 16 MHz, f_{HCLK1} = 2 MHz	Coremark	0.37		185.00	
				Dhrystone 2.1	0.39		195.00	
				While (1) (6)	0.65		325.00	

(1) Value guaranteed by characterization, not 100% tested in production.

(2) During power consumption test, GPIO needs to be configure as Analog Input mode.

(3) All peripherals disabled.

(4) The pre-fetch buffer is enabled when executing from EFLASH.

(5) EFLASH power on in Run mode when executing from SRAM.

(6) The code of While (1) used for results provided in ***Table 4-8***.

Table 4-10. Power consumption in Sleep mode(1)(2)(3)(4)

Symbol	Description	Conditions			Typ				Max(5)				Unit
		peripherals	General	f_{HCLK1}	25°C	55°C	85°C	105°C	25°C	55°C	85°C	105°C	
I_{SUM}	Sum of supply current from VDD and VDDA (Sleep mode)	All disabled	HXTAL_bypass = 8 MHz, PLL on, System Clock = f_{HCLK1}, CPU clock off	64 MHz	2.73	2.74	2.76	2.78	2.90	2.92	2.94	2.97	mA
				48 MHz	2.15	2.17	2.18	2.21	2.29	2.30	2.33	2.36	
				36 MHz	1.28	1.29	1.32	1.34	1.34	1.35	1.61	1.64	
				24 MHz	1.00	1.00	1.02	1.04	1.04	1.05	1.07	1.11	
				16 MHz	0.80	0.81	0.83	0.85	0.83	0.84	0.87	0.91	
			IRC16M = 16 MHz, System clock = 16 MHz, PLL off, CPU clock off	16 MHz	0.61	0.62	0.63	0.65	0.65	0.66	0.68	0.71	
				8 MHz	0.44	0.45	0.46	0.48	0.47	0.48	0.50	0.54	
				4 MHz	0.36	0.36	0.38	0.40	0.40	0.40	0.41	0.45	
				2 MHz	0.32	0.33	0.33	0.35	0.35	0.36	0.37	0.41	
				1 MHz	0.29	0.30	0.31	0.33	0.30	0.32	0.35	0.38	
		All enabled	HXTAL_bypass = 8 MHz, PLL on, System Clock = f_{HCLK1}, CPU clock off	64 MHz	9.30	9.35	9.39	9.43	9.80	9.86	9.92	9.96	
				48 MHz	7.10	7.14	7.18	7.21	7.51	7.56	7.59	7.63	
				36 MHz	5.45	5.48	5.51	5.54	5.68	5.71	5.76	5.81	
				24 MHz	3.80	3.81	3.84	3.86	3.97	3.99	4.01	4.05	
				16 MHz	2.69	2.70	2.72	2.75	2.80	2.81	2.84	2.88	
			IRC16M = 16 MHz, System clock = 16 MHz, PLL off, CPU clock off	16 MHz	2.89	2.90	2.92	2.95	3.00	3.03	3.06	3.09	
				8 MHz	1.60	1.61	1.63	1.65	1.67	1.68	1.71	1.74	
				4 MHz	0.95	0.96	0.98	1.00	1.00	1.01	1.03	1.07	
				2 MHz	0.63	0.64	0.66	0.68	0.67	0.68	0.70	0.73	
				1 MHz	0.47	0.48	0.49	0.51	0.50	0.52	0.53	0.57	

(1) Value guaranteed by characterization, not 100% tested in production.

(2) The Flash memory access time is adjusted with the correctly wait states number.

(3) During power consumption test, GPIO needs to be configure as Analog Input mode.

(4) When the peripherals are enabled, APB2 clock = f_{HCLK1}, APB1 clock = f_{HCLK1} / 2.

(5) V_{DD} = V_{DDA} = 3.63 V for values in Max columns.

Table 4-11. Power consumption in Deep-sleep mode(1)(2)

Symbol	Description	Conditions		Typ				Max				Unit
		General	V_{DD}	25°C	55°C	85°C	105°C	25°C	55°C	85°C	105°C	
I_{SUM}	Sum of supply current from VDD and VDDA (Deep-sleep mode)	NPLDO in normal driver mode, IRC32K off, RTC off	1.71V	144.51	150.49	163.64	180.25	155.18	162.07	185.78	219.21	μA
			2.6V	145.39	151.35	164.22	180.85	156.13	163.03	185.51	219.51	
			3.3V	146.26	152.21	165.16	181.90	157.07	163.91	186.44	220.59	
			3.63V	146.97	152.99	166.02	182.84	157.84	164.66	187.24	221.38	
		NPLDO in Low driver mode, IRC32K off, RTC off	1.71V	84.53	90.88	101.91	112.66	91.46	99.39	119.92	141.28	
			2.6V	85.68	91.98	102.86	113.33	92.67	100.56	120.71	141.74	
			3.3V	86.60	92.86	103.73	114.05	93.60	101.42	121.53	142.26	
			3.63V	87.24	93.50	104.41	114.64	94.26	102.02	122.07	142.62	
	Sum of supply current from VDD and VDDA (Deep-sleep 1 mode)	IRC32K off, RTC off, EFLASH power off	1.71V	3.48	5.58	11.68	20.63	14.49	24.26	60.60	115.80	
			2.6V	3.53	5.64	11.77	20.74	14.71	24.39	60.79	116.07	
			3.3V	3.62	5.77	12.01	21.05	15.00	24.71	61.67	116.84	
			3.63V	3.74	5.99	12.30	21.52	15.50	25.85	62.17	117.53	
	Sum of supply current from VDD and VDDA (Deep-sleep 2 mode)	IRC32K off, RTC off, EFLASH power off, CPU have retention register	1.71V	0.87	1.59	3.75	6.19	5.02	8.37	19.59	25.10	
			2.6V	0.94	1.71	3.88	6.28	5.65	9.01	20.02	23.63	
			3.3V	1.02	1.89	4.09	6.45	6.00	9.84	20.32	24.01	
			3.63V	1.16	2.17	4.41	6.62	6.18	11.29	20.87	31.51	

(1) Value guaranteed by characterization, not 100% tested in production.

(2) During power consumption test, GPIO needs to be configure as Analog Input mode.

Table 4-12. Power consumption in Standby mode(1)

Symbol	Description	Conditions		Typ				Max				Unit
		General	V_{DD}	25°C	55°C	85°C	105°C	25°C	55°C	85°C	105°C	
I_{SUM}	Sum of supply current from VDD and VDDA (Standby mode)	LXTAL off, IRC32K on, RTC on	1.71V	0.39	0.45	0.65	1.00	2.15	2.52	3.74	6.17	μA
			2.6V	0.54	0.62	0.85	1.24	2.96	3.41	4.83	7.57	
			3.3V	0.73	0.86	1.19	1.70	4.01	4.80	6.82	10.21	
			3.63V	0.91	1.11	1.55	2.21	5.38	6.67	9.48	13.78	

Symbol	Description	Conditions		Typ				Max				Unit
		General	V_{DD}	25°C	55°C	85°C	105°C	25°C	55°C	85°C	105°C	
		LXTAL off, IRC32K on, RTC off	1.71V	0.30	0.37	0.56	0.92	1.74	2.10	3.39	5.83	
			2.6V	0.40	0.48	0.71	1.10	2.29	2.75	4.16	6.88	
			3.3V	0.55	0.68	1.00	1.52	3.09	3.92	5.95	9.36	
			3.63V	0.71	0.91	1.34	2.01	4.35	5.70	8.50	12.95	
		LXTAL off, IRC32K off, RTC off	1.71V	0.18	0.24	0.44	0.80	1.12	1.49	2.77	5.19	
			2.6V	0.23	0.31	0.54	0.93	1.41	1.89	3.35	6.02	
			3.3V	0.32	0.46	0.78	1.29	2.00	2.80	4.82	8.20	
			3.63V	0.45	0.65	1.09	1.75	3.11	4.43	7.24	11.54	

(1) Value guaranteed by characterization, not 100% tested in production.

Table 4-13. Power consumption in BKP_ONLY mode(1)

Symbol	Description	Conditions		Typ				Unit
		General	V_{BAT}	25°C	55°C	85°C	105°C	
I_{BAT}	LXTAL+RTC current from VBAT (BKP_ONLY mode)	VDD off, LXTAL on with external crystal, RTC on, LXTAL High driving	1.71V	0.68	0.75	0.89	1.11	μA
			2.6V	0.77	0.84	0.99	1.23	
			3.3V	0.88	0.96	1.14	1.45	
			3.63V	0.97	1.07	1.28	1.60	
		VDD off, LXTAL on with external crystal, RTC on, LXTAL Medium High driving	1.71V	0.56	0.61	0.74	0.95	
			2.6V	0.65	0.71	0.84	1.07	
			3.3V	0.75	0.82	0.99	1.26	
			3.63V	0.83	0.92	1.13	1.44	
		VDD off, LXTAL on with external crystal, RTC on, LXTAL Medium Low driving	1.71V	0.37	0.41	0.52	0.72	
			2.6V	0.46	0.50	0.62	0.84	
			3.3V	0.56	0.62	0.77	1.02	
			3.63V	0.64	0.71	0.90	1.20	
			1.71V	0.31	0.34	0.45	0.66	

Symbol	Description	Conditions		Typ				Unit
		General	V_{BAT}	25°C	55°C	85°C	105°C	
		VDD off, LXTAL on with external crystal, RTC on, LXTAL Low driving	2.6V	0.40	0.44	0.56	0.78	
			3.3V	0.51	0.56	0.71	0.97	
			3.63V	0.59	0.66	0.84	1.15	

(1) Value guaranteed by sample, not 100% tested in production.

4.4 EMC characteristics

System level ESD (Electrostatic discharge, according to IEC 61000-4-2) and EFT (Electrical Fast Transient/burst, according to IEC 61000-4-4) testing result is given in the ***Table 4-14. System level ESD and EFT characteristics*** (1). System level ESD is for end-customer operation, it includes ESD field events on system level occur in an unprotected area (outside EPA). System level ESD protection necessary to satisfy higher ESD levels.

Table 4-14. System level ESD and EFT characteristics (1)

Symbol	Description	Conditions	Max	Level
V_{ESD}	Contact / Air mode high voltage stressed on few special I/O pins	V_{DD} = 3.3 V, T_A = 25 °C LQFP64, f_{HCLK} = 64 MHz IEC 61000-4-2	CD 6kV AD 8kV	3A
V_{EFT}	Fast transient high voltage burst stressed on Power and GND	V_{DD} = 3.3 V, T_A = 25 °C LQFP64, f_{HCLK} = 64 MHz IEC 61000-4-4	2kV	3A

(1) Value guaranteed by characterization, not 100% tested in production.

EMI (Electromagnetic Interference) emission test result is given in the ***Table 4-15. EMI characteristics*** (1), The electromagnetic field emitted by the device are monitored while an application, executing EEMBC code, is running. The test is compliant with SAE J1752-3:2017 standard which specifies the test board and the pin loading.

Table 4-15. EMI characteristics (1)

Symbol	Parameter	Conditions	Tested frequency band	Max vs. [f_{HXTAL}/f_{HCLK}]	Unit
				8/64 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = +25 °C, LQFP64, f_{HCLK} = 64 MHz, conforms to SAE J1752-3:2017	0.15 MHz to 30 MHz	-7.24	dBµV
			30 MHz to 130 MHz	3.87	
			130 MHz to 1 GHz	4.29	

(1) Value guaranteed by characterization, not 100% tested in production.

Component level ESD include HBM (Human body model, according to ANSI/ESDA/JEDEC JS-001) and CDM (ANSI/ESDA/JEDEC JS-002), that ESD field events during manufacturing in an ESD protected area, such as PCB assembly/repair, IC assembly/test and Fab environment. The ESD protected area (EPA) has many measures, for instance ESD protective packaging, grounding person wrist strap to ground (or flooring/footwear), grounded work surface and ionizer.

Table 4-16. Component level ESD characteristics (1)

Symbol	Description	Conditions	Max	Unit	Level
V_{HBM}	Human body model electrostatic discharge voltage (Any pin combination)	T_A = 25 °C; JS-001-2017	2000	V	2
V_{CDM}	Charge device model electrostatic discharge voltage (All pins)	T_A = 25 °C; JS-002-2018	500	V	C2a

(1) Value guaranteed by characterization, not 100% tested in production.

Latch-up (LU, according to JEDEC78) test is based on the two measurement methods, I/O current injection value (I-test) and power supply over-voltage value.

Table 4-17. Latch-up characteristics (1)

Symbol	Description	Conditions	Max	Unit	Class
LU	I-test	T_A = 125 °C; JESD78	200	mA	Class II Level A
	V_{supply} over voltage		5.4	V	

(1) Value guaranteed by characterization, not 100% tested in production.

4.5 Power supply supervisor characteristics

Table 4-18. Power supply supervisor characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LVD}	Low Voltage Detector Threshold	LVDT[2:0] = 000, rising edge	—	2.15	—	V
		LVDT[2:0] = 000, falling edge	—	2.05	—	V
		LVDT[2:0] = 001, rising edge	—	2.30	—	V
		LVDT[2:0] = 001, falling edge	—	2.20	—	V
		LVDT[2:0] = 010, rising edge	—	2.45	—	V
		LVDT[2:0] = 010, falling edge	—	2.35	—	V
		LVDT[2:0] = 011, rising edge	—	2.60	—	V
		LVDT[2:0] = 011, falling edge	—	2.50	—	V
		LVDT[2:0] = 100, rising edge	—	2.75	—	V
		LVDT[2:0] = 100, falling edge	—	2.65	—	V
		LVDT[2:0] = 101, rising edge	—	2.90	—	V
		LVDT[2:0] = 101, falling edge	—	2.80	—	V
		LVDT[2:0] = 110, rising edge	—	3.00	—	V
		LVDT[2:0] = 110, falling edge	—	2.90	—	V
$V_{LVD(HYST)}$	LVD hysteresis	—	—	100	—	mV
V_{BOR0}	Brown-out reset threshold 0	rising edge	—	1.56	—	V
		falling edge	—	1.48	—	
V_{BOR1}	Brown-out reset threshold 1	rising edge	—	2.10	—	V
		falling edge	—	2.00	—	
V_{BOR2}	Brown-out reset threshold 2	rising edge	—	2.30	—	V
		falling edge	—	2.20	—	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BOR3}	Brown-out reset threshold 3	rising edge	—	2.60	—	V
		falling edge	—	2.50	—	
V_{BOR4}	Brown-out reset threshold 4	rising edge	—	2.90	—	V
		falling edge	—	2.80	—	
$V_{BOR0(HYST)}$	BOR0 hysteresis	—	—	80	—	mV
$V_{BOR(HYST)}$	BOR hysteresis	—	—	100	—	mV
$t_{RST(TEMPO)}$	Reset temporization	—	—	550	—	μs

(1) Value guaranteed by design, not 100% tested in production.

4.6 External clock characteristics

Table 4-19. High speed external clock (HXTAL) generated from a crystal/ceramic characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL}	Crystal or ceramic frequency	V_{DD} = 3.3 V	4	8	48	MHz
R_F	Feedback resistor	V_{DD} = 3.3 V	—	400	—	kΩ
C_{HXTAL}(2)	Recommended matching capacitance on OSCIN and OSCOUT	—	—	20	30	pF
$Duty_{HXTAL}$	Crystal or ceramic duty cycle	—	30	50	70	%
g_m	Oscillator transconductance	Startup	—	25	—	mA/V
$I_{DD(HXTAL)}$	Crystal or ceramic operating current	V_{DD} = 3.3 V HXTAL = 8 MHz	—	0.35	—	mA
$t_{ST(HXTAL)}$	Crystal or ceramic startup time	V_{DD} = 3.3 V HXTAL = 8 MHz	—	1.4	—	ms

(1) Value guaranteed by design, not 100% tested in production.

(2) $C_{HXTAL1} = C_{HXTAL2} = 2*(C_{LOAD} - C_S)$, For C_{HXTAL1} and C_{HXTAL2}, it is recommended matching capacitance on OSCIN and OSCOUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

(3) More details about g_m could be found in ***AN052 GD32 MCU Resonator-Based Clock Circuits.***

Table 4-20. High speed external user clock characteristics (HXTAL in bypass mode) (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{HXTAL(EXT)}$	External clock source or oscillator frequency	V_{DD} = 3.3 V	1	8	50	MHz
$V_{H(HXTAL)}$	OSCIN input pin high level voltage	V_{DD} = 3.3 V	0.7 V_{DD}	—	V_{DD}	V
$V_{L(HXTAL)}$	OSCIN input pin low level voltage		V_{SS}	—	0.3 V_{DD}	
$t_{H/L(HXTAL)}$	OSCIN high or low time	—	5	—	—	ns
$t_{R/F(HXTAL)}$	OSCIN rise or fall time	—	—	—	10	
C_{IN}	OSCIN input capacitance	—	—	5	—	pF
$Duty_{HXTAL}$	Duty cycle	—	30	50	70	%

(1) Value guaranteed by design, not 100% tested in production.

Table 4-21. Low speed external clock (LXTAL) generated from a crystal/ceramic

characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LXTAL}	Crystal or ceramic frequency	V_{DD} = 3.3 V	—	32.768	—	kHz
C_{LXTAL}(2)	Recommended matching capacitance on OSC32IN and OSC32OUT	—	—	10	—	pF
$Duty_{LXTAL}$	Crystal or ceramic duty cycle	—	30	—	70	%
g_m	Oscillator transconductance	LXTALDRI[1:0]= 00	—	2.9	—	μA/V
		LXTALDRI[1:0]= 01	—	4.4	—	
		LXTALDRI[1:0]= 10	—	8.7	—	
		LXTALDRI[1:0]= 11	—	11.6	—	
$I_{DD(LXTAL)}$	Crystal or ceramic operating current	LXTALDRI[1:0]= 00	—	266	—	nA
		LXTALDRI[1:0]= 01	—	318	—	
		LXTALDRI[1:0]= 10	—	498	—	
		LXTALDRI[1:0]= 11	—	619	—	
$t_{ST(LXTAL)}$	Crystal or ceramic startup time	LXTALDRI[1:0]= 00	—	2	—	s
		LXTALDRI[1:0]= 01	—	1.2	—	
		LXTALDRI[1:0]= 10	—	0.7	—	
		LXTALDRI[1:0]= 11	—	0.5	—	

(1) Value guaranteed by design, not 100% tested in production.

(2) C_{LXTAL1} = C_{LXTAL2} = 2*(C_{LOAD} - C_S), For C_{LXTAL1} and C_{LXTAL2}, it is recommended matching capacitance on OSC32IN and OSC32OUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

(3) More details about g_m could be found in ***AN052 GD32 MCU Resonator-Based Clock Circuits.***

Table 4-22. Low speed external user clock characteristics (LXTAL in bypass mode) (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{LXTAL(EXT)}$	External clock source or oscillator frequency	V_{DD} = 3.3 V	—	32.768	1000	kHz
$V_{H(LXTAL)}$	OSC32IN input pin high level voltage	V_{DD} = 3.3 V	0.7 V_{DD}	—	V_{DD}	V
$V_{L(LXTAL)}$	OSC32IN input pin low level voltage		V_{SS}	—	0.3 V_{DD}	
$t_{H/L(LXTAL)}$	OSC32IN high or low time	—	250	—	—	ns
$t_{R/F(LXTAL)}$	OSC32IN rise or fall time	—	—	—	50	
C_{IN}	OSC32IN input capacitance	—	—	5	—	pF
$Duty_{LXTAL}$	Duty cycle	—	30	50	70	%

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-3. Recommended external OSCIN and OSCOUT pins circuit for crystal

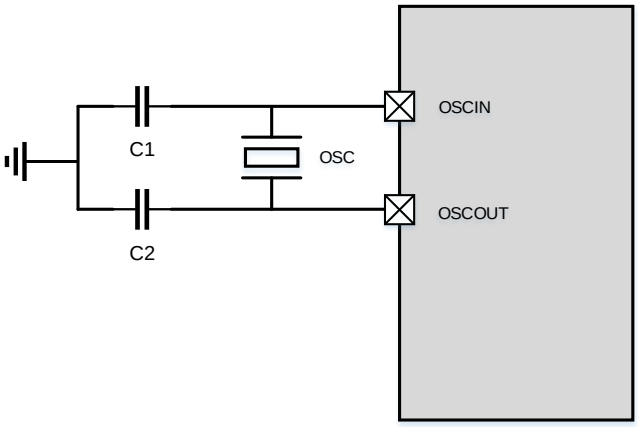
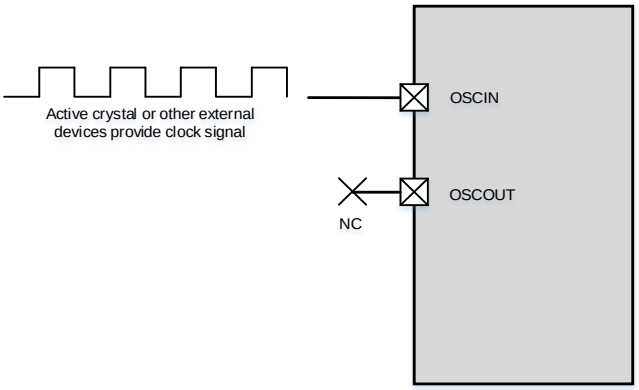


Figure 4-4. Recommended external OSCIN and OSCOUT pins circuit for oscillator



4.7 Internal clock characteristics

Table 4-23. High speed internal clock (IRC16M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC16M}	High Speed Internal Oscillator (IRC16M) frequency	V_{DD} = V_{DDA} = 3.3 V T_A = 25 °C	15.84	16	16.16	MHz
$Drift_{IRC16M}$	IRC16M oscillator Frequency Drift, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +85 °C	-2	—	2	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +105 °C	-3	—	3	%
	IRC16M oscillator Frequency accuracy, User trimming step(1)	—	—	0.3	—	%
$Duty_{IRC16M}$(1)	IRC16M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V	45	50	55	%
$I_{DDA(IRC16M)}$(1)	IRC16M oscillator operating current	V_{DD} = V_{DDA} = 3.3 V, f_{IRC16M} = 16 MHz	—	90	—	μA
$t_{ST(IRC16M)}$(1)	IRC16M oscillator startup time	V_{DD} = V_{DDA} = 3.3 V, f_{IRC16M} = 16 MHz	—	0.9	—	μs

(1) Value guaranteed by design, not 100% tested in production.

Table 4-24. High speed internal clock (IRC48M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC48M}	High Speed Internal Oscillator (IRC48M) frequency	V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C	47.04	48	48.96	MHz
$Drift_{IRC48M}$	IRC48M oscillator Frequency Drift, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +85 °C	-3	—	3	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +105 °C	-3	—	3	%
	IRC48M oscillator Frequency accuracy, User trimming step(1)	—	—	0.125	—	%
$Duty_{IRC48M}$(1)	IRC48M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V	45	50	55	%
$I_{DDA(IRC48M)}$(1)	IRC48M oscillator operating current	V_{DD} = V_{DDA} = 3.3 V, f_{IRC48M} = 48 MHz	—	285	—	μA
$t_{ST(IRC48M)}$(1)	IRC48M oscillator startup time	V_{DD} = V_{DDA} = 3.3 V, f_{IRC48M} = 48 MHz	—	1.6	—	μs

(1) Value guaranteed by design, not 100% tested in production.

Table 4-25. Low speed internal clock (IRC32K) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC32K}	Low Speed Internal oscillator (IRC32K) frequency	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ 85 °C	28	—	36	kHz
		V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ 105 °C	28	—	36	
		V_{DD} = V_{DDA} = 3.3 V T_A = 25 °C	29	32	35	
$I_{DDA(IRC32K)}$(1)	IRC32K oscillator operating current	V_{DD} = V_{DDA} = 3.3 V	—	220	—	nA
$t_{ST(IRC32K)}$(1)	IRC32K oscillator startup time	V_{DD} = V_{DDA} = 3.3 V	—	32	—	µs

(1) Value guaranteed by design, not 100% tested in production.

4.8 PLL characteristics

Table 4-26. PLL characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}	PLL input clock frequency	—	2	—	16	MHz
f_{PLLOUT}	PLL output clock frequency	—	16	—	64	MHz
t_{LOCK}	PLL lock time	—	—	—	200	µs
I_{DD}	Current consumption on V_{DD}	VCO freq = 64 MHz	—	450	—	µA
$Jitter_{PLL}$(2)	Cycle to cycle Jitter（rms）	System clock	—	200	—	ps
	Cycle to cycle Jitter（peak to peak）		—	1000	—	

(1) Value guaranteed by design, not 100% tested in production.

(2) Value given with main PLL running.

4.9 Memory characteristics

Table 4-27. Flash memory characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PE_{CYC}	Number of guaranteed program /erase cycles before failure (Endurance)	—	100	—	—	kcycles
t_{RET}	Data retention time	—	10	—	—	years
t_{PROG}	Double word programming time	T_A range(2)	—	20	—	µs
t_{ERASE}	Page erase time		1	—	20	ms
t_{MERASE}	Mass erase time		—	—	20	ms

(1) Value guaranteed by design, not 100% tested in production.

(2) For grade 6 devices, the parameter of T_A=85°C, For grade 7 devices, the parameter of T_A=105°C.

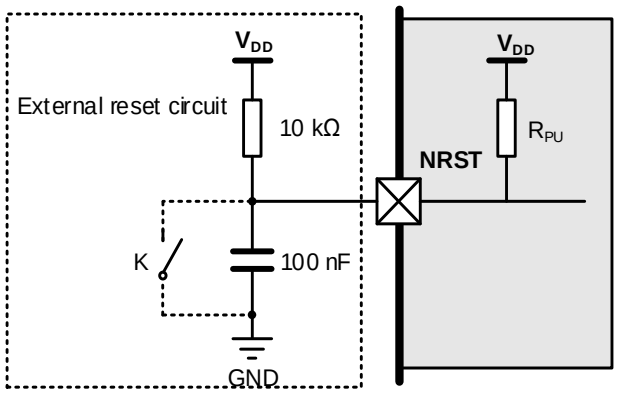
4.10 NRST pin characteristics

Table 4-28. NRST pin characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST Input low level voltage	V_{DD} = V_{DDA} = 1.71 V	-0.3	—	0.3 V_{DD}	V
$V_{IH(NRST)}$	NRST Input high level voltage		0.7 V_{DD}	—	V_{DD} + 0.3	
V_{HYST}	Schmidt trigger Voltage hysteresis		—	390	—	mV
$V_{IL(NRST)}$	NRST Input low level voltage	V_{DD} = V_{DDA} = 3.3 V	-0.3	—	0.3 V_{DD}	V
$V_{IH(NRST)}$	NRST Input high level voltage		0.7 V_{DD}	—	V_{DD} + 0.3	
V_{HYST}	Schmidt trigger Voltage hysteresis		—	509	—	mV
$V_{IL(NRST)}$	NRST Input low level voltage	V_{DD} = V_{DDA} = 3.63 V	-0.3	—	0.3 V_{DD}	V
$V_{IH(NRST)}$	NRST Input high level voltage		0.7 V_{DD}	—	V_{DD} + 0.3	
V_{HYST}	Schmidt trigger Voltage hysteresis		—	539	—	mV
R_{PU}	Pull-up equivalent resistor	—	—	40	—	kΩ

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-5. Recommended external NRST pin circuit (1)



(1) Unless the voltage on NRST pin go below $V_{IL(NRST)}$ level, the device would not generate a reliable reset.

4.11 VREF buffer characteristics

Table 4-29. VREF buffer characteristics (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Supply voltage	Normal mode, V_{DDA}=3.3V	VREFS = 0	1.71	—	3.63	V
			VREFS = 1	2.7	—	3.63	
		Degraded mode	VREFS = 0	—	—	—	
			VREFS = 1	1.71	—	2.7	
V_{REFBUF_OUT}	Voltage Reference Buffer Output	Normal mode, at V_{DDA}=3.3V, T_J = 30 °C	VREFS = 0	1.490	1.50	1.510	
			VREFS = 1	2.490	2.50	2.510	

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		Degraded mode	VREFS = 0	—	—	—	
			VREFS = 1	Min(V_{DDA}-150mV, 2.495)	—	2.505	
TRIM	Trim step resolution	—		—	0.13	—	%
C_L	Load capacitor	—		—	1	—	µF
ESR	Equivalent Serial Resistor of CL	—		—	—	2	Ω
I_{LOAD}	Static load current	—		—	—	4	mA
$t_{ST(VREFBUF)}$	Start-up time	C_L = 1 µF + 10 nF		—	—	800	µs
$I_{DDA(VREFBUF)}$	V_{REFBUF} consumption from V_{DDA}	I_{LOAD} = 0 µA	—	—	30	—	µA
		I_{LOAD} = 500 µA	—	—	30	—	
		I_{LOAD} = 4 mA	—	—	30	—	
I_{INRUSH}	Control of maximum DC current drive on V_{REFBUF_OUT} during startup phase	—		—	10	—	mA
$Regu_{(LINE)}$	Line regulation	2.8 V ≤ V_{DDA} ≤ 3.6 V	I_{load} = 500 µA	—	400	—	ppm / V
			I_{load} = 4 mA	—	400	—	
$Regu_{(LOAD)}$	Load regulation	500 µA ≤ I_{LOAD} ≤ 4 mA	Normal mode	—	60	—	ppm / mA
PSRR	Power supply rejection	DC	—	—	60	—	dB
		100kHz	—	—	30	—	

(1) Value guaranteed by design, not 100% tested in production.

4.12 GPIO characteristics

Table 4-30. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}(1)	Standard IO Low level input voltage	1.71 V < V_{DD} = V_{DDA} < 3.63 V	—	—	0.3 V_{DD}	V
	5V-tolerant IO Low level input voltage	1.71V < V_{DD} = V_{DDA} < 3.63 V	—	—	0.3 V_{DD}	V
V_{IH}(1)	Standard IO High level input voltage	1.71 V < V_{DD} = V_{DDA} < 3.63 V	0.7 V_{DD}	—	—	V
	5V-tolerant IO High level input voltage	1.71V < V_{DD} = V_{DDA} < 3.63 V	0.7 V_{DD}	—	—	V
V_{HYS}(1)	Input hysteresis	V_{DD} =3.3 V	—	320	—	mV
I_{LEAK}	Input leakage current	V_{SS} ≤ V_{IN} ≤ V_{DD}	-2	—	2	µA
R_{PU}(1)	Weak pull-up equivalent	V_{IN} = V_{SS}	—	40	—	kΩ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	resistor					
R_{PD}(1)	Weak pull-down equivalent resistor	V_{IN} = V_{DD}	—	40	—	kΩ

(1) Value guaranteed by design, not 100% tested in production.

Table 4-31. Output voltage characteristics for all I/Os except PC13, PC14, PC15 (1)(2)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL} (IO_speed=50MHz)	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.71 V	0.16	0.28	V
		V_{DD} = 3.3 V	0.10	0.21	
		V_{DD} = 3.63 V	0.10	0.20	
	Low level output voltage for an IO Pin (I_{IO} = +10 mA)	V_{DD} = 1.71 V	0.21	0.33	
		V_{DD} = 3.3 V	0.13	0.23	
		V_{DD} = 3.63 V	0.12	0.23	
	Low level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 1.71 V	0.49	0.77	
		V_{DD} = 3.3 V	0.25	0.42	
		V_{DD} = 3.63 V	0.24	0.41	
V_{OH} (IO_speed=50MHz)	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.71 V	1.27	1.46	V
		V_{DD} = 3.3 V	3.02	3.15	
		V_{DD} = 3.63 V	3.36	3.48	
	High level output voltage for an IO Pin (I_{IO} = +10 mA)	V_{DD} = 1.71 V	1.21	1.37	
		V_{DD} = 3.3 V	2.99	3.12	
		V_{DD} = 3.63 V	3.33	3.45	
	High level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 3.3 V	2.75	2.93	
		V_{DD} = 3.63 V	3.10	3.28	
V_{OL} (IO_speed=10MHz)	Low level output voltage for an IO Pin (I_{IO} = +4 mA)	V_{DD} = 1.71 V	0.23	0.33	V
		V_{DD} = 3.3 V	0.14	0.21	
		V_{DD} = 3.63 V	0.14	0.21	
	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.71 V	0.57	0.92	
		V_{DD} = 3.3 V	0.28	0.39	
		V_{DD} = 3.63 V	0.27	0.38	
	Low level output voltage for an IO Pin (I_{IO} = +15 mA)	V_{DD} = 1.71 V	1.02	1.12	
		V_{DD} = 3.3 V	0.54	0.69	
		V_{DD} = 3.63 V	0.52	0.66	
V_{OH} (IO_speed=10MHz)	High level output voltage for an IO Pin (I_{IO} = +4 mA)	V_{DD} = 1.71 V	1.13	1.30	V
		V_{DD} = 3.3 V	2.99	3.08	
		V_{DD} = 3.63 V	3.33	3.42	
	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 3.3 V	2.72	2.85	
		V_{DD} = 3.63 V	3.08	3.21	
	High level output voltage for an IO Pin (I_{IO} = +15 mA)	V_{DD} = 3.3 V	2.23	2.41	
		V_{DD} = 3.63 V	2.65	2.81	

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL} (IO_speed=2MHz)	Low level output voltage for an IO Pin (I_{IO} = +1 mA)	V_{DD} = 1.71 V	0.23	0.29	V
		V_{DD} = 3.3 V	0.13	0.18	
		V_{DD} = 3.63 V	0.13	0.18	
	Low level output voltage for an IO Pin (I_{IO} = +4 mA)	V_{DD} = 3.3 V	0.58	0.71	
		V_{DD} = 3.63 V	0.56	0.68	
V_{OH} (IO_speed=2MHz)	High level output voltage for an IO Pin (I_{IO} = +1 mA)	V_{DD} = 1.71 V	1.37	1.44	
		V_{DD} = 3.3 V	3.11	3.15	
		V_{DD} = 3.63 V	3.45	3.49	
	High level output voltage for an IO Pin (I_{IO} = +4 mA)	V_{DD} = 3.3 V	2.49	2.63	
		V_{DD} = 3.63 V	2.88	3.00	

(1) Value guaranteed by characterization, not 100% tested in production.

(2) All pins except PC13 / PC14 / PC15. Since PC13 to PC15 are supplied through the Power Switch, which can only be obtained by a small current(typical source capability:3 mA shared between these IOs, but sink capability is same as other IO), the speed of GPIOs PC13 to PC15 should not exceed 2 MHz when they are in output mode(maximum load: 30 pF).

Table 4-32. I/O port AC characteristics (1)(2)(3)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
x0	t_R/t_F	Output high to low level fall time and output low to high level rise time	2.5 ≤ V_{DD} ≤ 3.63 V, C_L = 10 pF	—	13.5	ns
			1.71 ≤ V_{DD} ≤ 2.5 V, C_L = 10 pF	—	21	
			2.5 ≤ V_{DD} ≤ 3.63 V, C_L = 30 pF	—	31.5	
			1.71 ≤ V_{DD} ≤ 2.5 V, C_L = 30 pF	—	48	
			2.5 ≤ V_{DD} ≤ 3.63 V, C_L = 50 pF	—	49.5	
			1.71 ≤ V_{DD} ≤ 2.5 V, C_L = 50 pF	—	76	
01	t_R/t_F	Output high to low level fall time and output low to high level rise time	2.5 ≤ V_{DD} ≤ 3.63 V, C_L = 10 pF	—	4.1	ns
			1.71 ≤ V_{DD} ≤ 2.5 V, C_L = 10 pF	—	6.7	
			2.5 ≤ V_{DD} ≤ 3.63 V, C_L = 30 pF	—	9.5	
			1.71 ≤ V_{DD} ≤ 2.5 V, C_L = 30 pF	—	15	
			2.5 ≤ V_{DD} ≤ 3.63 V, C_L = 50 pF	—	14.5	
			1.71 ≤ V_{DD} ≤ 2.5 V, C_L = 50 pF	—	23	
11	t_R/t_F	Output high to low	2.5 ≤ V_{DD} ≤ 3.63 V,	—	2.7	ns

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
		level fall time and output low to high level rise time	C_L = 10 pF			
			1.71 ≤ V_{DD} ≤ 2.5 V, C_L = 10 pF	—	4.4	
			2.5 ≤ V_{DD} ≤ 3.63 V, C_L = 30 pF	—	4	
			1.71 ≤ V_{DD} ≤ 2.5 V, C_L = 30 pF	—	6.4	
			2.5 ≤ V_{DD} ≤ 3.63 V, C_L = 50 pF	—	5.3	
			1.71 ≤ V_{DD} ≤ 2.5 V, C_L = 50 pF	—	8.6	

(1) The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.

(2) Value guaranteed by design, not 100% tested in production.

(3) The data is for reference only, and the specific values are related to PCB Layout.

4.13 ADC characteristics

Table 4-33. ADC characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage	—	1.71	3.3	3.63	V
V_{IN}	ADC input voltage range	—	0	—	V_{REFP}	V
V_{REFP}(2)	Reference Voltage	—	1.71	3.3	V_{DDA}	V
f_{ADC}	ADC clock	—	0.14	—	16	MHz
f_S	Sampling rate	12-bit	0.009	—	1.067	MSPS
		10-bit	0.01	—	1.23	
		8-bit	0.012	—	1.45	
		6-bit	0.015	—	1.78	
t_{TRIG}	External trigger period	f_{ADC} = 16 MHz, Resolution = 12 bits	—	—	19	$1/f_{ADC}$
R_{AIN}	External input impedance	See ***Equation 1***	—	—	387.5	kΩ
V_{CMIV}	Common mode input voltage	—	V_{REFP}/2-10%	V_{REFP}/2	V_{REFP}/2-10%	V
R_{ADC}	Input sampling switch resistance	V_{DDA} < 2.4V	—	—	5.7	kΩ
		V_{DDA} ≥ 2.4V	—	—	1.1	
C_{ADC}	Input capacitance	No pin/pad capacitance included	—	—	7.6	pF
t_{OFF_CAL}	Offset calibration time	—	46	—	—	$1/f_{ADC}$
t_{CAL}	Calibration time	f_{ADC} = 16 MHz	—	2.875	68.75	μs
t_S	Sampling time	f_{ADC} = 16 MHz	0.156	—	14.97	μs
t_{CONV}	Total conversion time(including sampling	12-bit	—	15	—	1/f_{ADC}
		10-bit	—	13	—	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	time)	8-bit	—	11	—	
		6-bit	—	9	—	
$I_{DDA\_S(ADC)}$	ADC consumption from V_{DDA} single ended mode	f_S = 1M	—	123	—	μA
		f_S = 0.5M	—	65	—	
		f_S = 10k	—	18	—	
$I_{DDA\_D(ADC)}$	ADC consumption from V_{DDA} differential ended mode	f_S = 1M	—	134	—	
		f_S = 0.5M	—	76	—	
		f_S = 10k	—	18	—	
$I_{DDV\_S(ADC)}$	ADC consumption from V_{REFP} single ended mode	f_S = 1M	—	10	—	μA
		f_S = 0.5M	—	5.6	—	
		f_S = 10k	—	1	—	
$I_{DDV\_D(ADC)}$	ADC consumption from V_{REFP} differential ended mode	f_S = 1M	—	20	—	
		f_S = 0.5M	—	10.5	—	
		f_S = 10k	—	1.1	—	
$t_{ST(ADC)}$	Startup time	—	—	5	—	μs

(1) Value guaranteed by design, not 100% tested in production.

(2) V_{REFP} should always be equal to or less than V_{DDA}, especially during power up.

Equation 1: R_{AIN} max formula $R_{AIN} < \frac{T_s}{f_{ADC} * C_{ADC} * \ln(2^{N+2})} - R_{ADC}$

The formula above (***Equation 1***) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 4-34. Internal reference voltage calibration values

Symbol	Test conditions	Memory address
V_{REFINT}(1)	V_{DD} = V_{DDA} = V_{REFP} = 3.3 V (± 3.65 mV), Temperature = 25 °C (± 4 °C)	0x1FFF F7FC - 0x1FFF F7FD

(1) V_{REFINT} is internally connected to the ADC_IN17 input channel.

Table 4-35. ADC RAIN max for f_{ADC} = 16 MHz (1)(2)

Resolution	Sampling cycles @16MHz	R_{AIN} max (kΩ)	
		V_{DDA} < 2.4V	V_{DDA} ≥ 2.4V
12 bits	2.5	N/A	1.0
	7.5	0.6	5.2
	13.5	5.7	10.3
	28.5	18.4	23.0
	41.5	29.4	34.0
	55.5	41.3	45.9
	71.5	54.8	59.4
	239.5	197.2	201.8
10 bits	2.5	N/A	1.3
	7.5	1.7	6.3
	13.5	7.6	12.2
	28.5	22.4	27.0

Resolution	Sampling cycles @16MHz	R_{AIN} max (kΩ)	
		V_{DDA} < 2.4V	V_{DDA} ≥ 2.4V
	41.5	35.3	39.9
	55.5	49.1	53.7
	71.5	64.9	69.5
	239.5	231.0	235.6
8 bits	2.5	N/A	1.8
	7.5	3.9	7.7
	13.5	11.6	14.9
	28.5	31.0	32.7
	41.5	47.7	48.1
	55.5	65.7	64.7
	71.5	86.4	83.7
	239.5	302.8	283.0
6 bits	2.5	N/A	2.6
	7.5	5.4	10.0
	13.5	14.3	18.9
	28.5	36.5	41.1
	41.5	55.8	60.4
	55.5	76.6	81.2
	71.5	100.3	104.9
	239.5	349.4	354.0

(1) Value guaranteed by design, not 100% tested in production.

(2) The R_{AIN} value was calculated by theory and stray capacitance of actual pcb has not been taken into account.

Table 4-36. ADC accuracy at f_{ADC} = 16 MHz (1)

Symbol	Parameter	Test conditions	Typ	Unit
EO	Offset error	Single ended	±1	LSB
		Differential	±1	
DNL	Differential linearity error	Single ended	±1	
		Differential	±1	
INL	Integral linearity error	Single ended	±1.5	
		Differential	±1.3	
ENOB	Effective number of bits	Single ended	10.75	Bits
		Differential	11.0	
SNDR	Signal-to-noise and distortion ratio	Single ended	66.5	dB
		Differential	68.3	
SNR	Signal-to-noise ratio	Single ended	68.2	
		Differential	70.5	
THD	Total harmonic distortion	Single ended	-70.5	
		Differential	-71.4	

(1) Value guaranteed by sample, not 100% tested in production.

4.14 DAC characteristics

Table 4-37. DAC characteristics (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Operating voltage	—		1.8	3.3	3.63	V
V_{REFP}	Positive Reference Voltage	—		1.8	—	V_{DDA}	V
R_{LOAD}	Resistive load	Resistive load with buffer ON	connected to V_{SSA}	5	—	—	kΩ
			connected to V_{DDA}	5	—	—	
Ro	output Impedance	output Impedance with buffer OFF		—	—	15	kΩ
C_{LOAD}	Capacitive load	DAC output buffer ON		—	—	50	pF
V_{DAC_OUT}	Lower Voltage on DAC_OUT output	DAC output buffer ON		0.2	—	—	V
		DAC output buffer OFF		0.5	—	—	mV
	Higher Voltage on DAC_OUT output	DAC output buffer ON		—	—	V_{DDA}-0.2	V
		DAC output buffer OFF		—	—	V_{DDA}-1LSB	V
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches the final value of ±0.5 LSB, ±1 LSB, ±2 LSB, ±4 LSB, ±8 LSB)	Normal mode, DAC output buffer ON, C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 5 kΩ	±0.5 LSB	—	1.2	1.4	µs
			±1 LSB	—	1.0	1.3	
			±2 LSB	—	0.9	1.2	
			±4 LSB	—	0.85	1.1	
			±8 LSB	—	0.80	1.0	
		Normal mode, DAC output buffer OFF, ±1 LSB, C_{LOAD} ≤ 10 pF		—	1.50	2.00	
t_{WAKEUP}	Wakeup time from off state (setting the DEN bit in the DAC Control register) until the final value of ±1LSB is reached	DAC output buffer ON, C_{LOAD} ≤ 50 pF, R_{LOAD} = 5 kΩ		—	5	10	µs
		DAC output buffer OFF, C_{LOAD} ≤ 10 pF		—	2	5	
PSRR	Power supply rejection ratio(to V_{DDA})	No R_{LOAD}, C_{LOAD}=50 pF		—	-80	—	dB
I_{DDA}	DAC current consumption in quiescent mode	DAC output buffer ON	No load, middle code (0x800)	—	430	—	µA

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
			No load, worst code (0xF1C)	—	450	—	
		DAC output buffer OFF	No load, middle code (0x800)	—	2	—	
$I_{DD(VREFP)}$	DAC current consumption in quiescent mode	DAC output buffer ON	No load, middle code (0x800)	—	85	—	µA
			No load, worst code (0xF1C)	—	375	—	
		DAC output buffer OFF	No load, middle code (0x800)	—	85	—	

(1) Value guaranteed by design, not 100% tested in production.

Table 4-38. DAC accuracy (1)

Symbol	Parameter	Test conditions		Min	Typ	Max	Unit
DNL	Differential non linearity	DAC output buffer ON		—	± 1.5	—	LSB
		DAC output buffer OFF		—	± 1.5	—	
INL	Integral non linearity	DAC output buffer ON C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 5 kΩ		—	± 3	—	LSB
		DAC output buffer OFF C_{LOAD} ≤ 50 pF, no R_{LOAD}		—	± 3	—	
Offset	Offset error at code 0x800	DAC output buffer ON C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 5 kΩ	V_{REFP} = 3.63 V	—	± 3	—	LSB
			V_{REFP} = 1.8 V	—	± 5	—	
		DAC output buffer OFF C_{LOAD} ≤ 50 pF, no R_{LOAD}		—	± 3	—	
GE	Gain error	DAC output buffer ON C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 5 kΩ		—	± 0.25	—	%
		DAC output buffer OFF C_{LOAD} ≤ 50 pF, no R_{LOAD}		—	± 0.25	—	

(1) Value guaranteed by sample, not 100% tested in production.

4.15 Temperature sensor characteristics

Table 4-39. Temperature sensor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{25}(1)	Voltage at T_A = 25 °C (± 4 °C)	V_{DD} = V_{DDA} = V_{REFP} = 3.3 V (± 3.65 mV)	0.925	1.01	1.088	mV
Avg_Slope(2)	Average slope	—	—	3.2	—	mV/°C
T_L(2)	V_{SENSE} linearity with temperature	T_J = -40 °C to 125 °C	—	-0.5 ~ 1	—	°C
t_{S_temp}(2)	ADC sampling time when reading the temperature	—	10	—	—	µs
t_{ON}(2)	Turn-on Time	f_{ADC} = 5 MHz, t_{S_temp} = 10 µs	—	37.8	—	µs
ETOT(2)	Temperature Sensor Total Error	T_J = -40 °C to 125 °C	—	-2 ~ 2.5	—	°C

(1) The V_{25} ADC conversion result is stored in the TS_CAL1 byte.

(2) Value guaranteed by design, not 100% tested in production.

Table 4-40. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	Temperature sensor raw data acquired value at 25 °C (± 4 °C), V_{DD} = V_{DDA} = V_{REFP} = 3.3V (± 3.65 mV)	0x1FFF F7F8 - 0x1FFF F7F9

4.16 Comparators characteristics

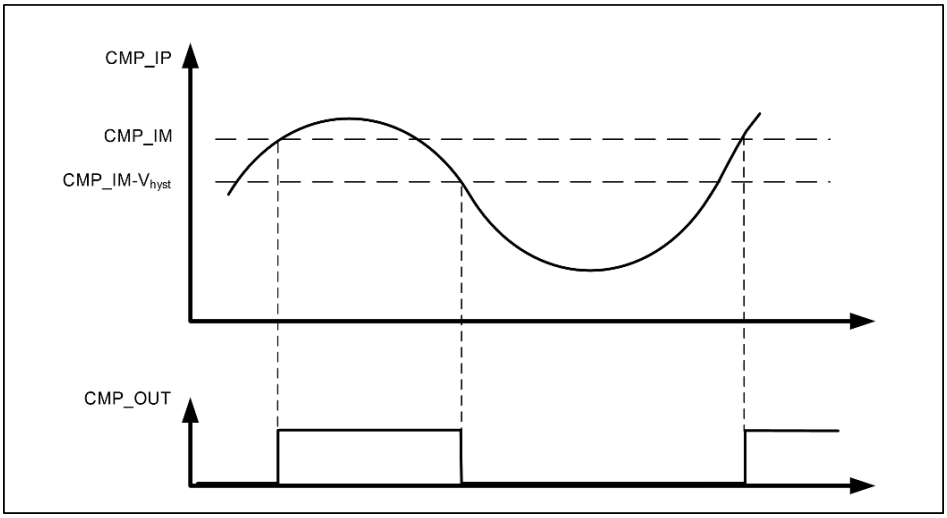
Table 4-41. CMP characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage	—	1.71	3.3	3.63	V
V_{IN}	Input voltage range	—	0	—	V_{DDA}	V
V_{SC}	Scaler offset voltage	—	—	±5	—	mV
$I_{DDA(SCALER)}$	Scaler static consumption from V_{DDA}	BEN=0 (bridge disable)	—	200	—	nA
		BEN=1 (bridge enable)	—	800	—	
$t_{ST(SCALER)}$	Scaler startup time	—	—	140	—	µs
t_D	Propagation delay for 200mV step with 100 mV overdrive	Ultra-low power mode	—	3	—	µs
		Medium power mode	—	181	—	ns
		High speed power mode	—	55	—	ns
	Propagation delay for step > 200 mV with 100 mV overdrive only on positive inputs	Ultra-low power mode	—	3.8	—	µs
		Medium power mode	—	334	—	ns
		High speed power mode	—	77	—	ns
$t_{ST(CMP)}$	Comparator startup time to	High-speed mode	—	—	1.85	µs

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
	reach propagation delay specification	Medium mode		—	—	3.8	
		Ultra-low-power mode		—	—	27	
$I_{DDA(CMP)}$	Current consumption from V_{DDA}	Ultra-low power mode	Static	—	500	—	nA
			With 50 kHz ±100 mV overdrive square signal	—	1330	—	
		Medium power mode	Static	—	4.4	—	µA
			With 50 kHz ±100 mV overdrive square signal	—	4.8	—	
		High speed power mode	Static	—	45.6	—	
			With 50 kHz ±100 mV overdrive square signal	—	42.7	—	
V_{OFFSET}	Offset error	—		—	±5	—	mV
V_{HYST}	Hysteresis Voltage	No Hysteresis		—	0	—	mV
		Low Hysteresis		—	8	—	
		Medium Hysteresis		—	16	—	
		High Hysteresis		—	32	—	

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-6. CMP hysteresis



4.17 CAN characteristics

Refer to ***Table 4-30. I/O static characteristics*** for more details on the input/output alternate function characteristics (CAN TX and CAN RX).

4.18 TIMER characteristics

Table 4-42. TIMER characteristics (1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{RES}	Timer resolution time	—	1	—	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 64 MHz	15.6	—	ns
f_{EXT}	Timer external clock frequency	—	0	$f_{TIMERxCLK}/2$	MHz
		$f_{TIMERxCLK}$ = 64 MHz	0	32	MHz
RES	Timer resolution	—	—	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	—	1	65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 64 MHz	0.0156	1024	μs
t_{MAX_COUNT}	Maximum possible count	—	—	65536 × 65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 64 MHz	—	67.11	s

(1) Value guaranteed by design, not 100% tested in production.

4.19 SLCD controller characteristics

Table 4-43. SLCD controller characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{SLCD}	SLCD external voltage		—	—	3.63	V
I_{VSLCD}(2)	Supply current from V_{SLCD} (V_{SLCD} = 3.3 V)	High drive	—	14.3	—	μA
		Low drive(SLCD_RSEL=00)	—	0.55	—	
		Low drive(SLCD_RSEL=01)		0.82		
		Low drive(SLCD_RSEL=10)	—	1.65	—	
		Low drive(SLCD_RSEL=11)	—	3.3	—	
R_{HN}	Total High Resistor value for Low drive resistive network	SLCD_RSEL=00	—	6	—	MΩ
		SLCD_RSEL=01	—	4	—	
		SLCD_RSEL=10	—	2	—	
		SLCD_RSEL=11	—	1	—	
R_{LN}	Total Low Resistor value for High drive resistive network		—	230	—	kΩ
V_{44}	Segment/Common highest level voltage		—	V_{SLCD}	—	V
V_{34}	Segment/Common 3/4 level voltage		—	3/4V_{SLCD}	—	
V_{23}	Segment/Common 2/3 level voltage		—	2/3V_{SLCD}	—	
V_{12}	Segment/Common 1/2 level voltage		—	1/2V_{SLCD}	—	
V_{13}	Segment/Common 1/3 level voltage		—	1/3V_{SLCD}	—	
V_{14}	Segment/Common 1/4 level voltage		—	1/4V_{SLCD}	—	
V_0	Segment/Common lowest level voltage		—	0	—	

(1) Value guaranteed by design, not 100% tested in production.

(2) SLCD enabled with 3.3V,1/8 duty,1/4 bias, division ratio= 64, all pixels active, no SLCD connected.

4.20 I2C characteristics

Table 4-44. I2C characteristics (1)(2)

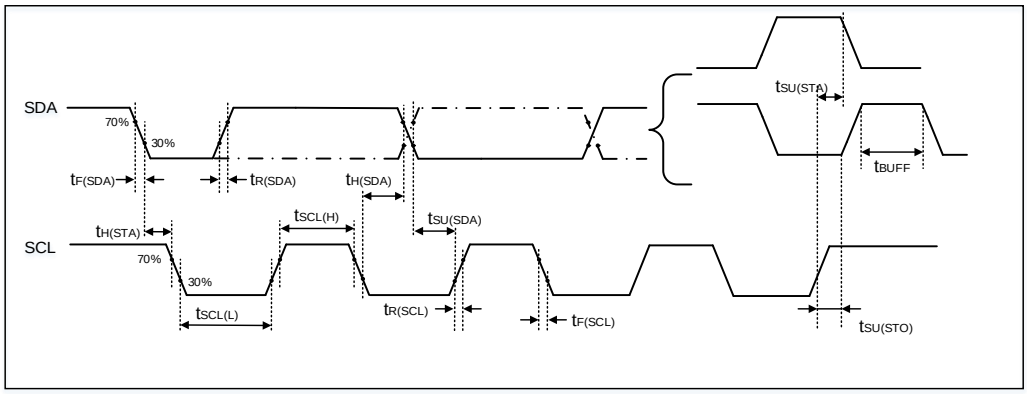
Symbol	Parameter	Conditions	Standard mode		Fast mode		Fast mode plus		Unit
			Min	Max	Min	Max	Min	Max	
$t_{SCL(H)}$	SCL clock high time	—	4.0	—	0.6	—	0.2	—	μs
$t_{SCL(L)}$	SCL clock low time	—	4.7	—	1.3	—	0.5	—	μs
$t_{SU(SDA)}$	SDA setup time	—	250	—	100	—	50	—	ns
$t_{H(SDA)}$	SDA data hold time	—	0(3)	3450	0	900	0	450	ns
$t_{R(SDA/SCL)}$	SDA and SCL rise time	—	—	1000	—	300	—	120	ns
$t_{F(SDA/SCL)}$	SDA and SCL fall time	—	—	300	—	300	—	120	ns
$t_{H(STA)}$	Start condition hold time	—	4.0	—	0.6	—	0.26	—	μs
$t_{SU(STA)}$	Repeated Start condition setup time	—	4.7	—	0.6	—	0.26	—	μs
$t_{SU(STO)}$	Stop condition setup time	—	4.0	—	0.6	—	0.26	—	μs
t_{BUFF}	Stop to Start condition time (bus free)	—	4.7	—	1.3	—	0.5	—	μs

(1) Value guaranteed by design, not 100% tested in production.

(2) To ensure the standard mode I2C frequency, f_{PCLK1} must be at least 2 MHz. To ensure the fast mode I2C frequency, f_{PCLK1} must be at least 4 MHz. To ensure the fast mode plus I2C frequency, f_{PCLK1} must be at least a multiple of 10 MHz.

(3) The device should provide a data hold time of 300 ns at least in order to bridge the undefined region of the falling edge of SCL.

Figure 4-7. I2C bus timing diagram



4.21 SPI characteristics

Table 4-45. Standard SPI characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	—	—	—	16	MHz
$t_{SCK(H)}$	SCK clock high time	Master mode, f_{PCLKx} = 64 MHz, presc = 4	—	20	—	ns
$t_{SCK(L)}$	SCK clock low time	Master mode, f_{PCLKx} = 64 MHz, presc = 4	—	20	—	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time	—	—	—	10	ns
$t_{H(MO)}$	Data output hold time	—	0	—	—	ns
$t_{SU(MI)}$	Data input setup time	—	1	—	—	ns
$t_{H(MI)}$	Data input hold time	—	0	—	—	ns
SPI slave mode						
$t_{SU(NSS)}$	NSS enable setup time	—	0	—	—	ns
$t_{H(NSS)}$	NSS enable hold time	—	1	—	—	ns
$t_{A(SO)}$	Data output access time	—	—	8	—	ns
$t_{DIS(SO)}$	Data output disable time	—	—	9	—	ns
$t_{V(SO)}$	Data output valid time	—	—	9	—	ns
$t_{SU(SI)}$	Data input setup time	—	0	—	—	ns
$t_{H(SI)}$	Data input hold time	—	1	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-8. SPI timing diagram - master mode

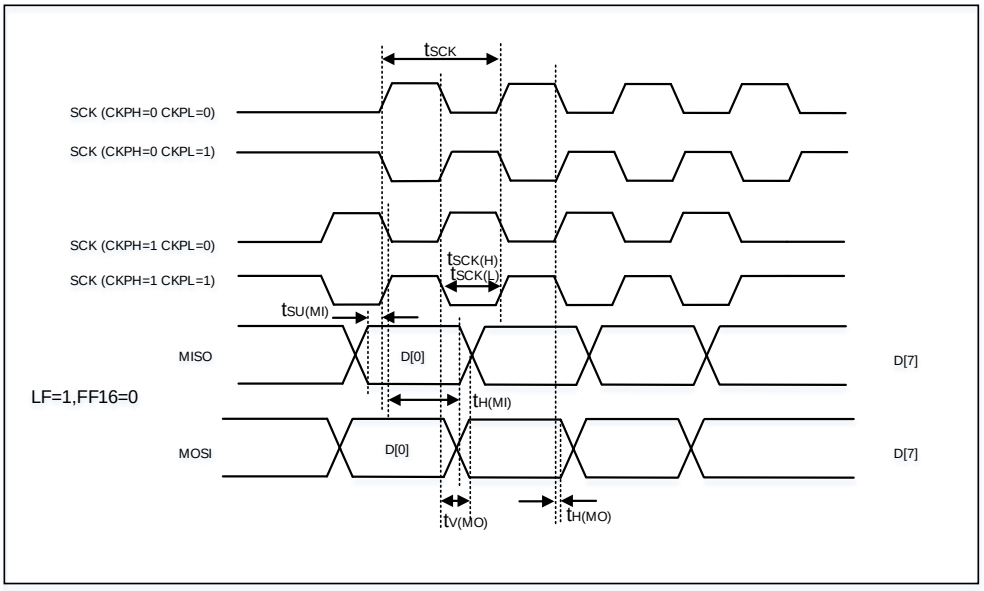
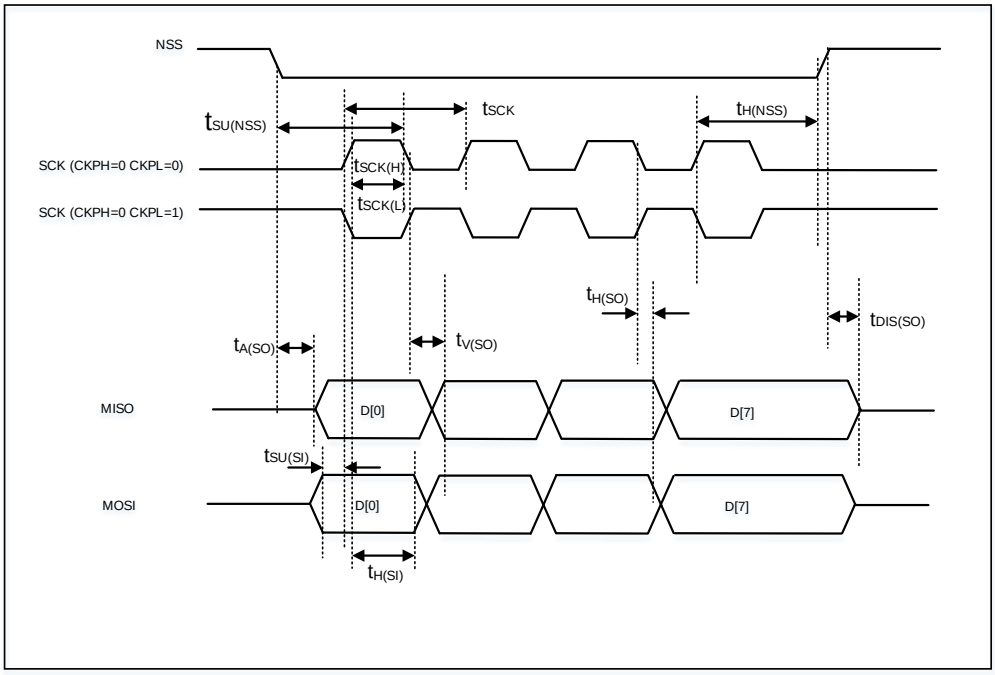


Figure 4-9. SPI timing diagram - slave mode



4.22 I2S characteristics

Table 4-46. I2S characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	Clock frequency	Master mode (data: 16 bits, Audio frequency = 96 kHz)	—	6.25	—	MHz
		Slave mode	—	—	12.5	
t_H	Clock high time	—	—	80	—	ns
t_L	Clock low time		—	80	—	ns
$t_{V(WS)}$	WS valid time	Master mode	—	3	—	ns
$t_{H(WS)}$	WS hold time	Master mode	—	3	—	ns
$t_{SU(WS)}$	WS setup time	Slave mode	0	—	—	ns
$t_{H(WS)}$	WS hold time	Slave mode	3	—	—	ns
$Duty_{(SCK)}$	I2S slave input clock duty cycle	Slave mode	—	50	—	%
$t_{SU(SD\_MR)}$	Data input setup time	Master mode	1	—	—	ns
$t_{SU(SD\_SR)}$	Data input setup time	Slave mode	0	—	—	ns
$t_{H(SD\_MR)}$	Data input hold time	Master receiver	0	—	—	ns
$t_{H(SD\_SR)}$		Slave receiver	1	—	—	ns
$t_{V(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	—	—	10	ns
$t_{H(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	3	—	—	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{V(SD\_MT)}$	Data output valid time	Master transmitter (after enable edge)	—	—	10	ns
$t_{H(SD\_MT)}$	Data output hold time	Master transmitter (after enable edge)	0	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-10. I2S timing diagram - master mode

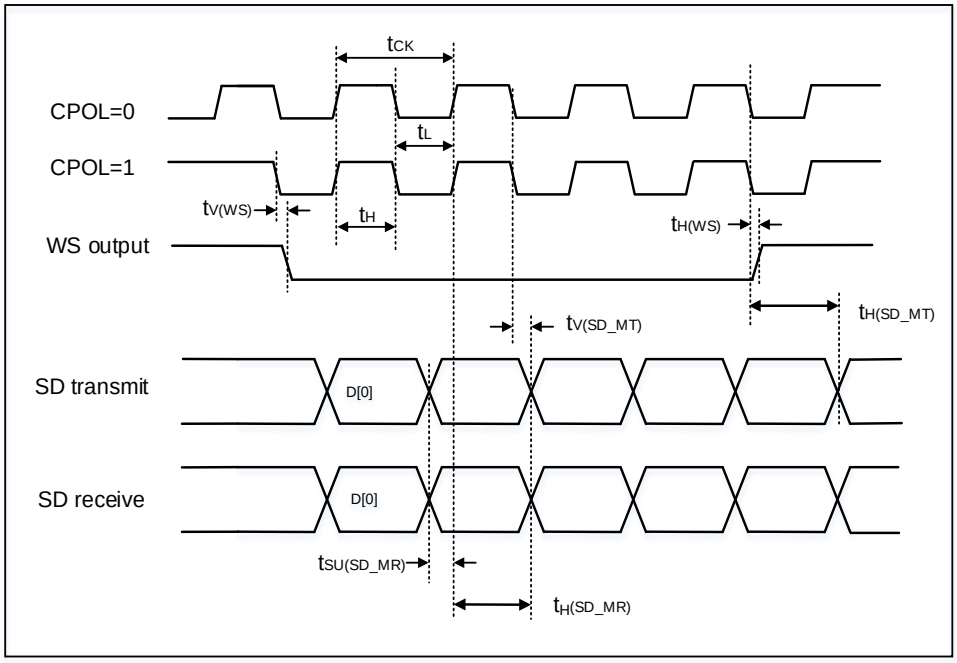
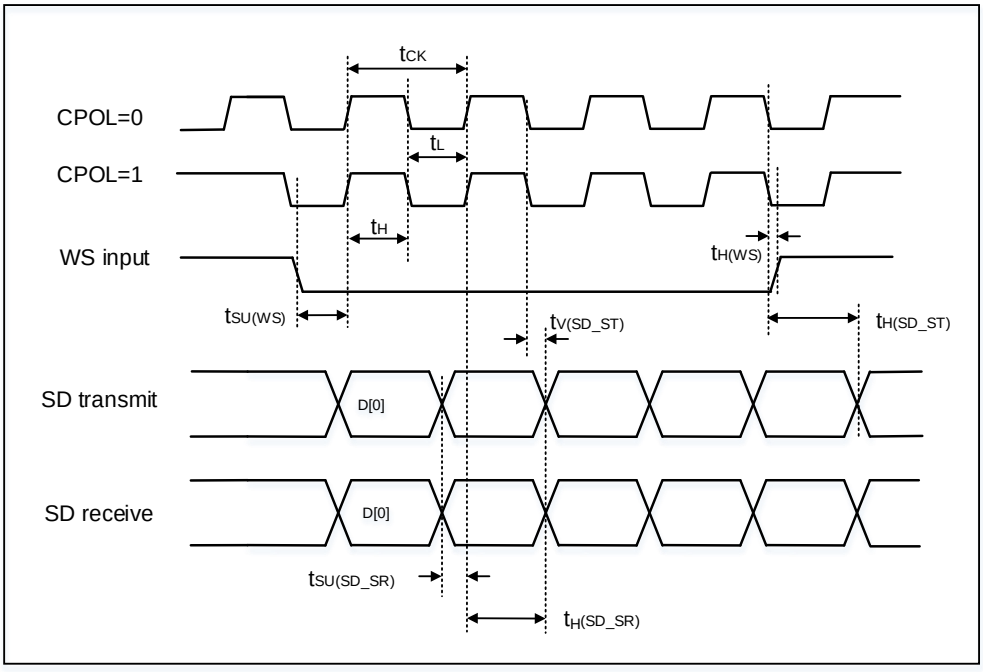


Figure 4-11. I2S timing diagram - slave mode



4.23 USART/LPUART characteristics

Table 4-47. USART/LPUART characteristics in Synchronous mode (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	f_{PCLKx} = 64 MHz	—	—	32	MHz
$t_{SCK(H)}$	SCK clock high time	f_{PCLKx} = 64 MHz	15.625	—	—	ns
$t_{SCK(L)}$	SCK clock low time	f_{PCLKx} = 64 MHz	15.625	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

Table 4-48. USART/LPUART characteristics in Smartcard mode (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	f_{PCLKx} = 64 MHz	—	—	32	MHz
$t_{SCK(H)}$	SCK clock high time	f_{PCLKx} = 64 MHz	15.625	—	—	ns
$t_{SCK(L)}$	SCK clock low time	f_{PCLKx} = 64 MHz	15.625	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

4.24 USBD characteristics

Table 4-49. USBD startup time

Symbol	Parameter	Max	Unit
$t_{ST(USBD)}$ (1)	USBD startup time	1	μs

(1) Value guaranteed by design, not 100% tested in production.

Table 4-50. USBD DC electrical characteristics (1)

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
Input levels	V_{DD}	USBD operating voltage	—	3.0	—	3.6	V
	V_{DI}	Differential input sensitivity	—	0.2	—	—	
	V_{CM}	Differential common mode range	Includes V_{DI} range	0.8	—	2.5	
	V_{ILSE}	Single ended receiver low level input voltage	—	—	—	0.8	
	V_{IHSE}	Single ended receiver high level input voltage	—	2.0	—	—	
Output levels	V_{OL}	Static output level low	R_L of 1.0 kΩ to 3.63 V	—	—	0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}	2.8	3.3	3.6	
R_{PU}		USBDP	V_{IN} = V_{SS}	1.2	1.5	1.8	KΩ

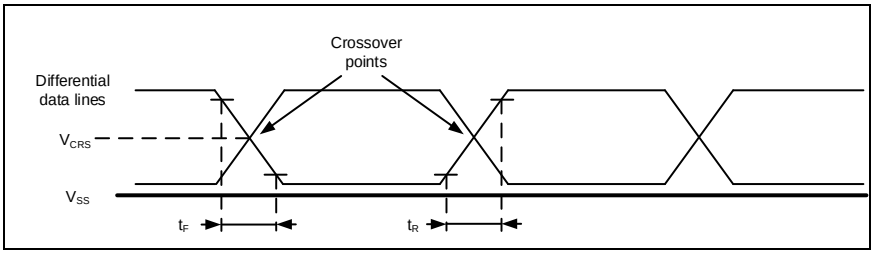
(1) Value guaranteed by design, not 100% tested in production.

Table 4-51. USBD full speed-electrical characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_R	Rise time	C_L = 50 pF	4	5	20	ns
t_F	Fall time	C_L = 50 pF	4	5	20	ns
t_{RFM}	Rise/ fall time matching	t_R / t_F	90	—	111	%
V_{CRS}	Output signal crossover voltage	—	1.3	—	2.0	V

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-12. USBD timings: definition of data signal rise and fall time



4.25 WDGT characteristics

Table 4-52. FWDGT min/max timeout period at 32 kHz (IRC32K) (1)

Prescaler divider	PSC[2:0] bits	Min timeout RLD[11:0]= 0x000	Max timeout RLD[11:0]= 0xFFF	Unit
1/4	000	0.03125	511.90625	ms
1/8	001	0.03125	1023.78125	
1/16	010	0.03125	2047.53125	
1/32	011	0.03125	4095.03125	
1/64	100	0.03125	8190.03125	
1/128	101	0.03125	16380.03125	
1/256	110 or 111	0.03125	32760.03125	

(1) Value guaranteed by design, not 100% tested in production.

Table 4-53. WWDGT min-max timeout value at 32 MHz (f_{PCLK1}) (1)

Prescaler divider	PSC[3:0]	Min timeout value CNT[6:0] = 0x40	Unit	Max timeout value CNT[6:0] = 0x7F	Unit
1/1	0000	128	µs	8.192	ms
1/2	0001	256		16.384	
1/4	0010	512		32.768	
1/8	0011	1.024	ms	65.536	
1/16	0100	2.048		131.072	
1/32	0101	4.096		262.144	
1/64	0110	8.192		524.288	
1/128	0111	16.384		1048.576	
1/256	1000	32.768		2097.152	
1/512	1001	65.536		4194.304	
1/1024	1010	131.072		8388.608	
1/2048	1011	262.144		16777.216	
1/4096	1100	524.288		33554.432	
1/8192	1101	1048.576		67108.864	
1/1	1110	128	µs	4.096	
1/1	1111	128		4.096	

(1) Value guaranteed by design, not 100% tested in production.

5 Package information

5.1 LQFP64 package outline dimensions

Figure 5-1. LQFP64 package outline

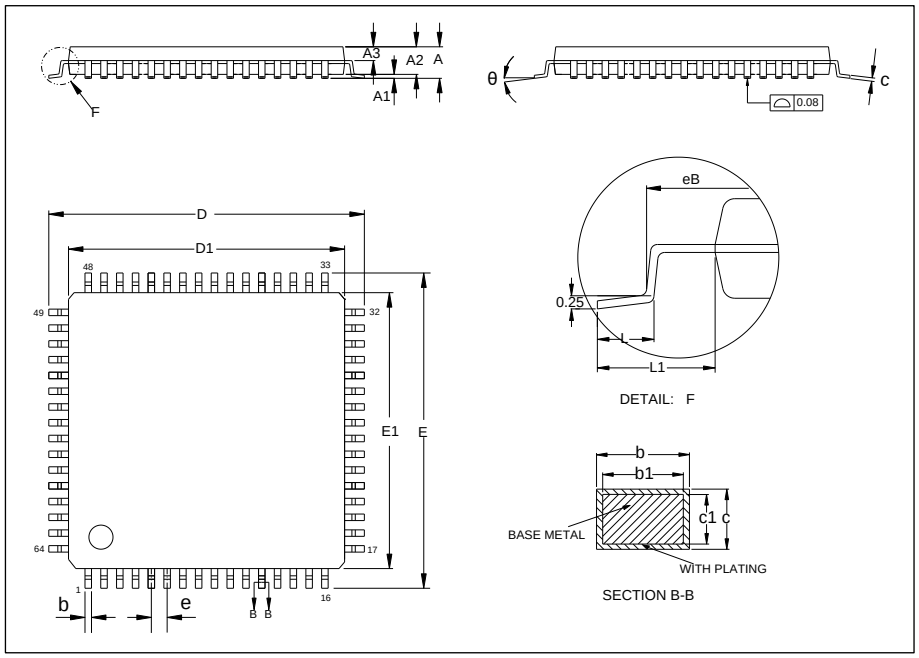
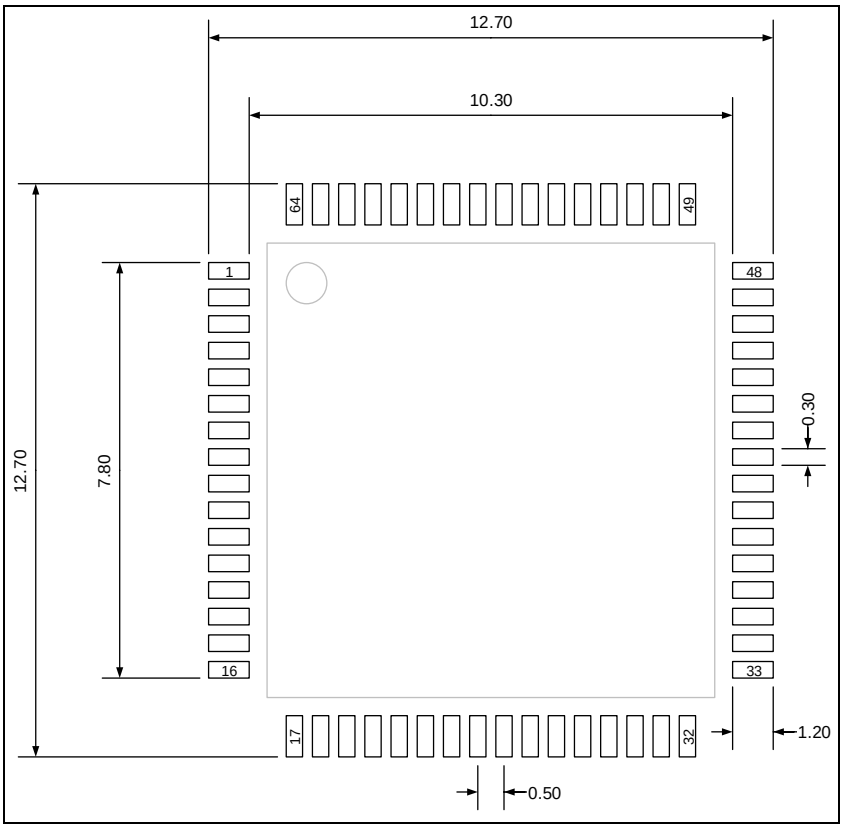


Table 5-1. LQFP64 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	—	0.50	—
eB	11.25	—	11.45
L	0.45	—	0.75
L1	—	1.00	—
θ	0°	—	7°

(Original dimensions are in millimeters)

Figure 5-2. LQFP64 recommended footprint



(Original dimensions are in millimeters)

5.2 QFN64 package outline dimensions

Figure 5-3. QFN64 package outline

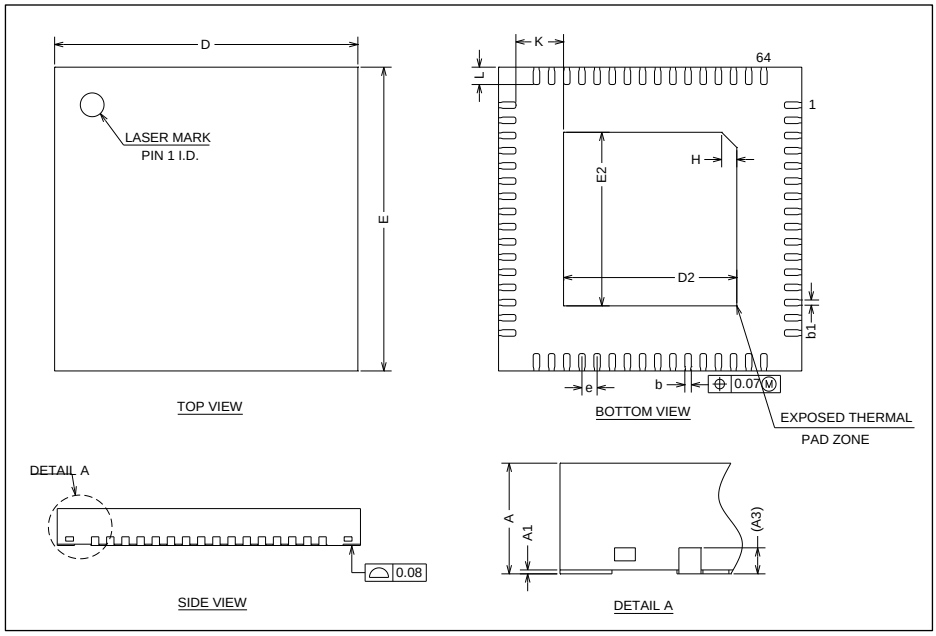
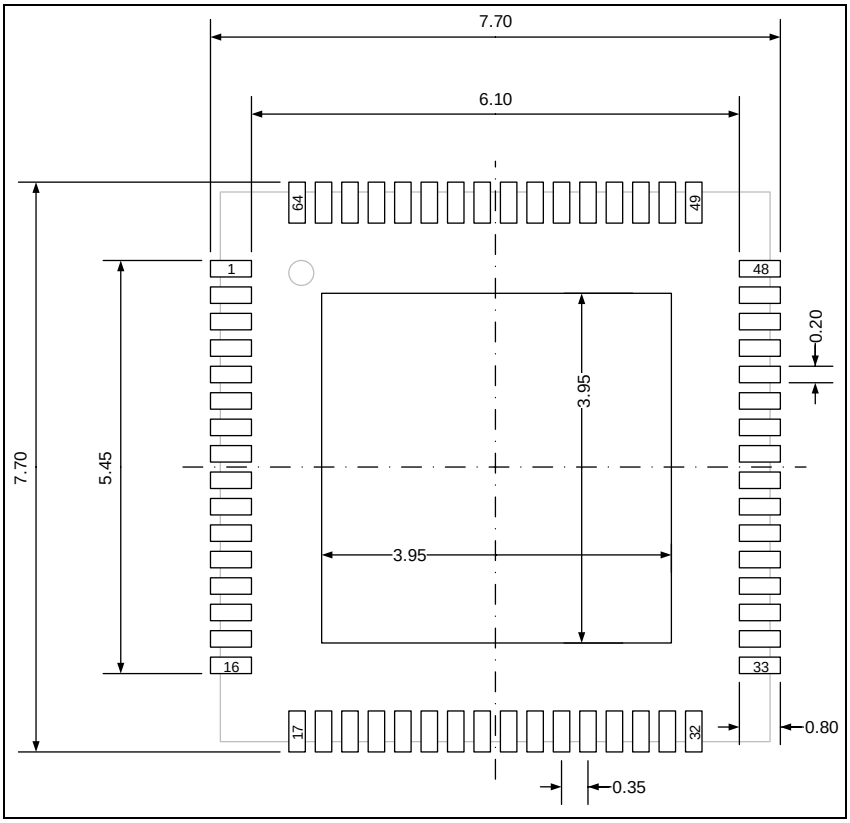


Table 5-2.QFN64 package dimensions

Symbol	Min	Typ	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	—	0.20	—
b	0.05	0.15	0.20
b1	—	0.12	—
D	6.90	7.00	7.10
D2	3.90	4.00	4.10
E	6.90	7.00	7.10
E2	3.90	4.00	4.10
e	—	0.35	—
H	0.30	0.35	0.40
K	—	1.10	—
L	0.30	0.40	0.50

(Original dimensions are in millimeters)

Figure 5-4. QFN64 recommended footprint



(Original dimensions are in millimeters)

5.3 LQFP48 package outline dimensions

Figure 5-5. LQFP48 package outline

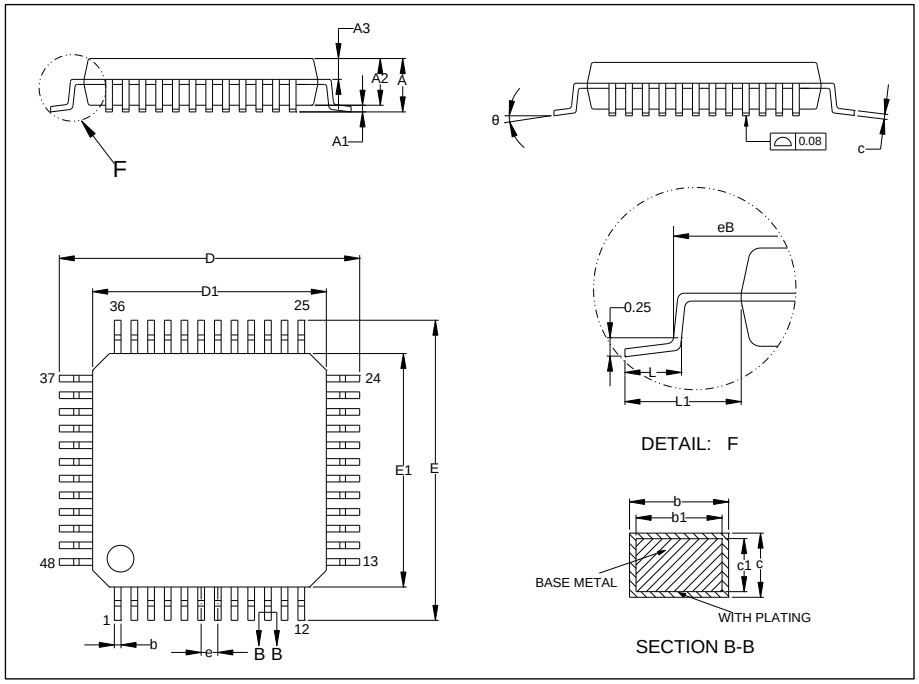
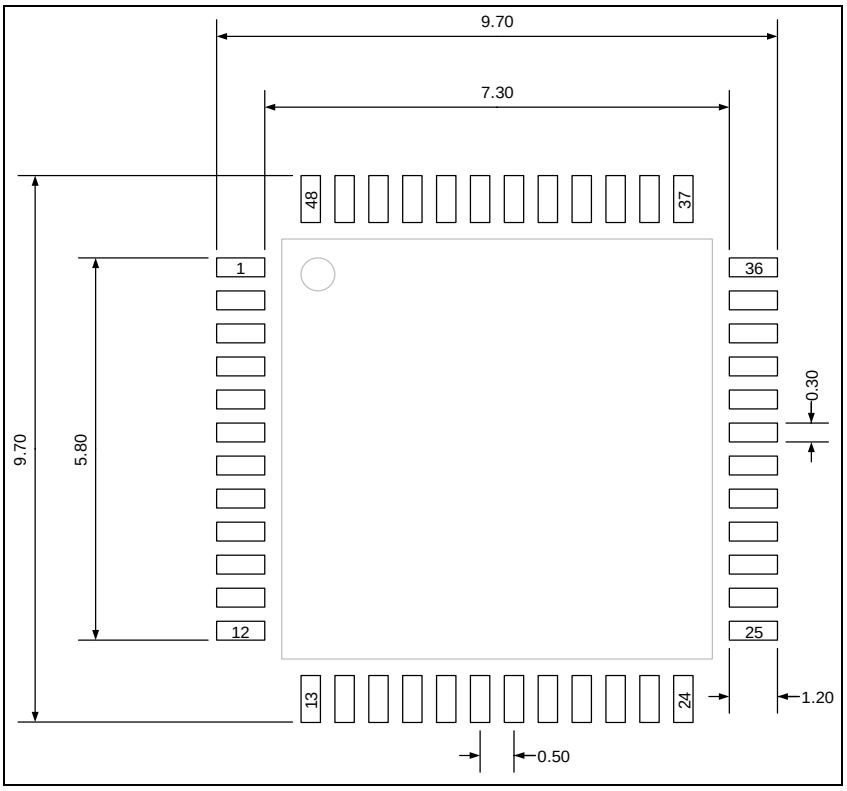


Table 5-3. LQFP48 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	—	0.50	—
eB	8.10	—	8.25
L	0.45	—	0.75
L1	—	1.00	—
θ	0°	—	7°

(Original dimensions are in millimeters)

Figure 5-6. LQFP48 recommended footprint



(Original dimensions are in millimeters)

5.4 QFN48 package outline dimensions

Figure 5-7. QFN48 package outline

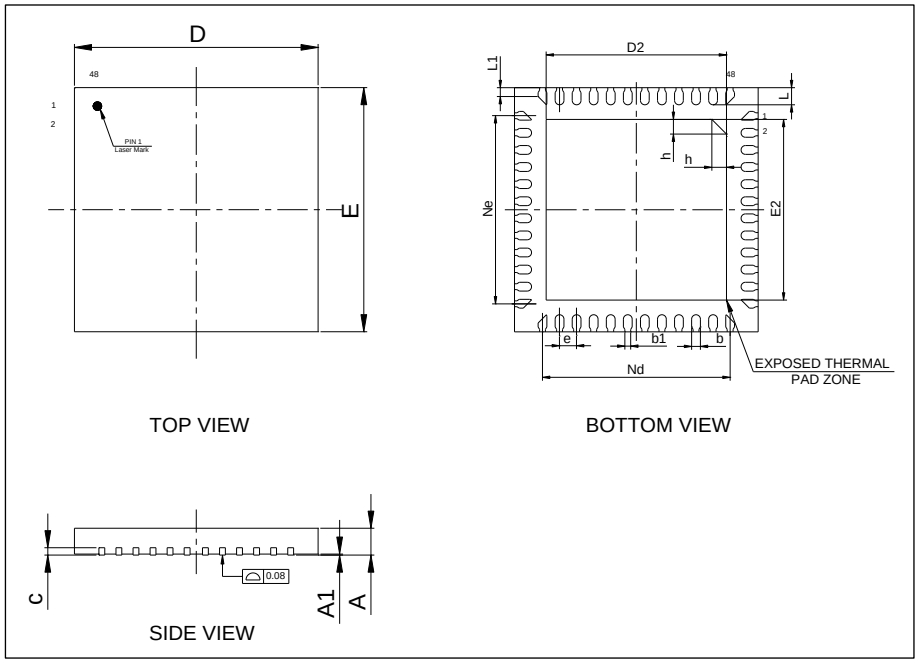
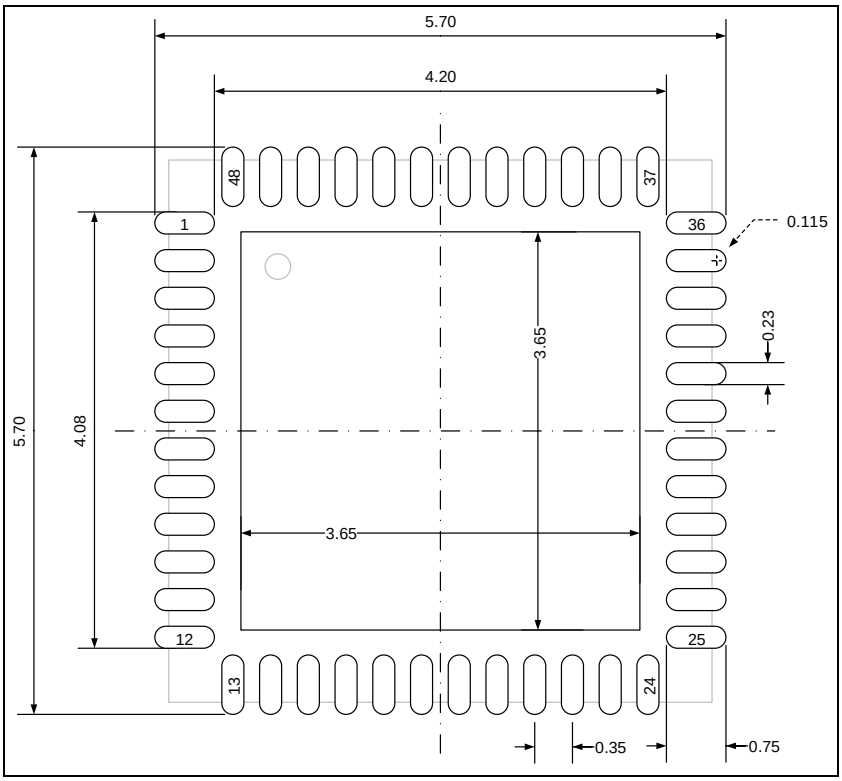


Table 5-4. QFN48 package dimensions

Symbol	Min	Typ	Max
A	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.13	0.18	0.23
b1	—	0.12	—
c	0.10	0.15	0.20
D	4.90	5.00	5.10
D2	3.60	3.70	3.80
E	4.90	5.00	5.10
E2	3.60	3.70	3.80
e	—	0.35	—
h	0.25	0.30	0.35
L	0.30	0.35	0.40
L1	0.13	0.18	0.23
Nd	—	3.85	—
Ne	—	3.85	—

(Original dimensions are in millimeters)

Figure 5-8. QFN48 recommended footprint



(Original dimensions are in millimeters)

5.5 LQFP32 package outline dimensions

Figure 5-9. LQFP32 package outline

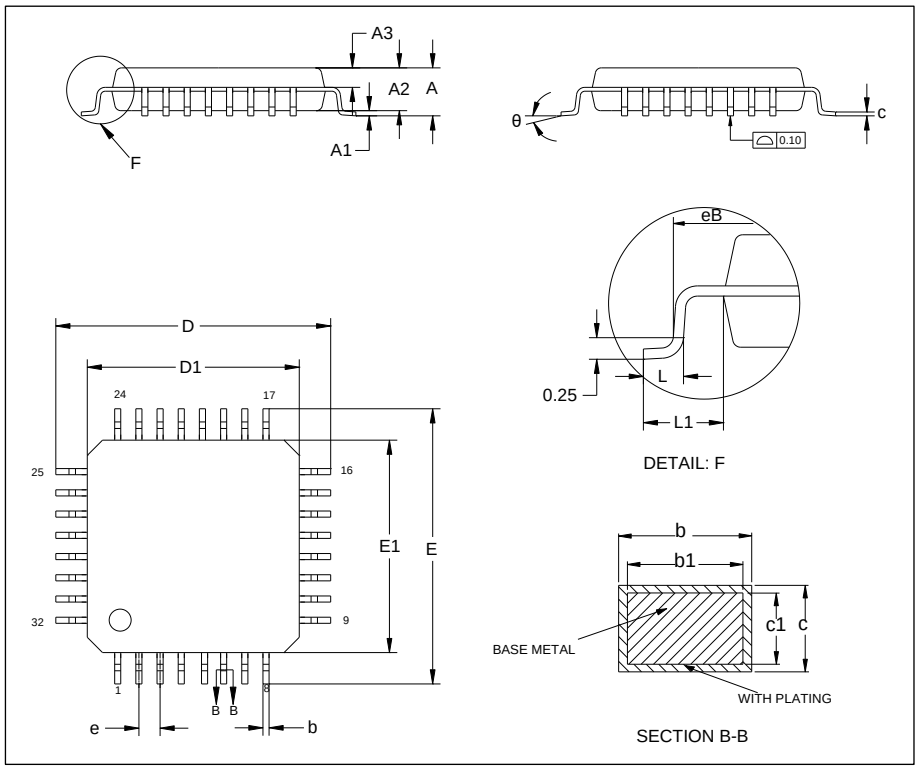
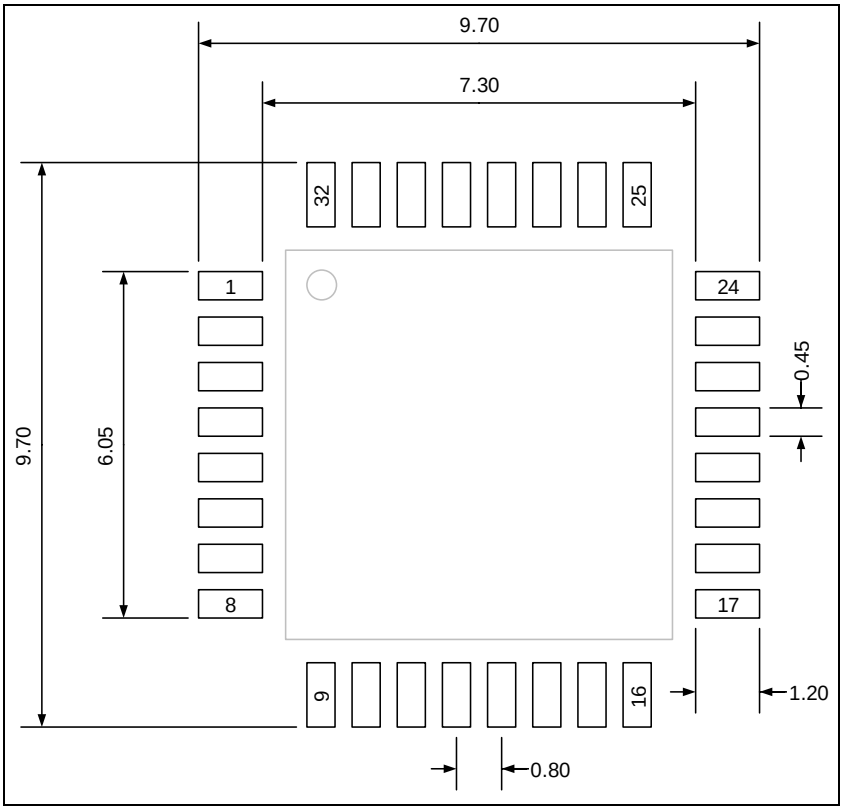


Table 5-5. LQFP32 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.33	—	0.41
b1	0.32	0.35	0.38
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	—	0.80	—
eB	8.10	—	8.25
L	0.45	—	0.75
L1	—	1.00	—
θ	0°	—	7°

(Original dimensions are in millimeters)

Figure 5-10. LQFP32 recommended footprint



(Original dimensions are in millimeters)

5.6 QFN32/QFN32 VREFP package outline dimensions

Figure 5-11. QFN32/QFN32 VREFP package outline

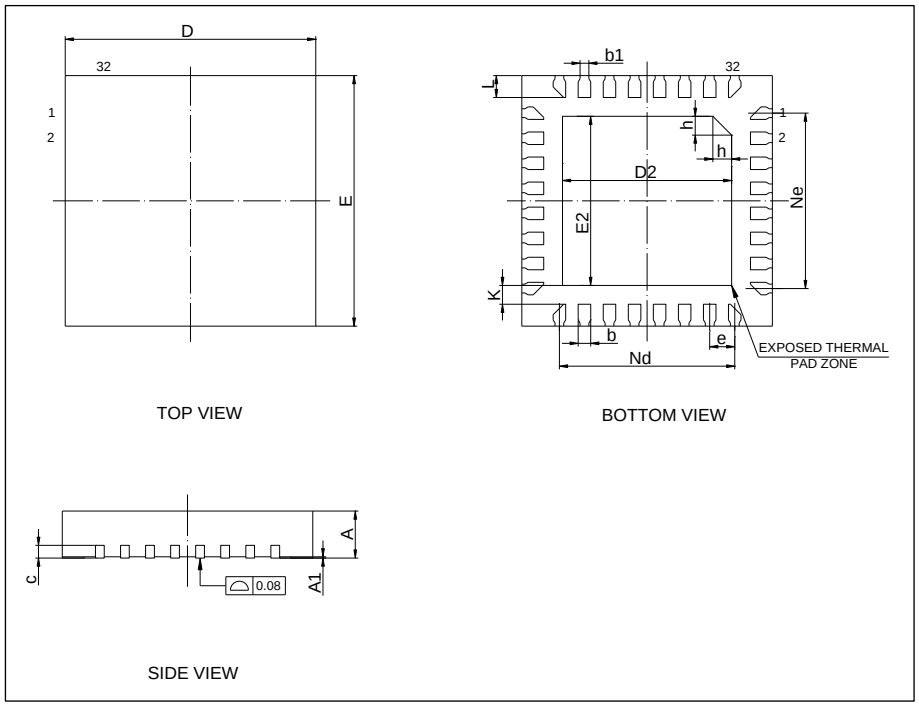
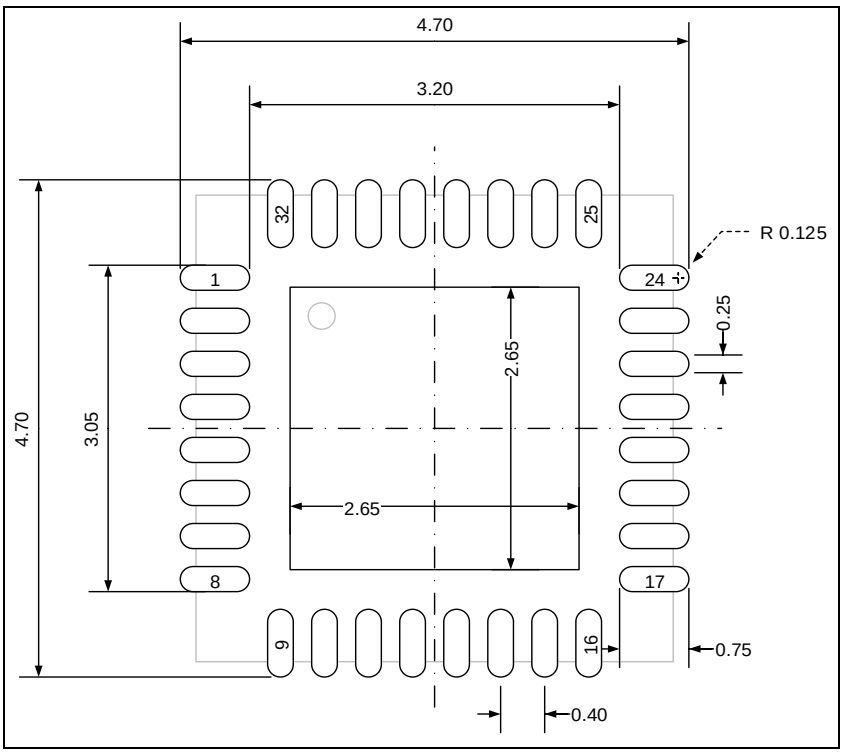


Table 5-6. QFN32/QFN32 VREFP package dimensions

Symbol	Min	Typ	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1	—	0.14	—
c	—	0.20	—
D	3.90	4.00	4.10
D2	2.60	2.70	2.80
E	3.90	4.00	4.10
E2	2.60	2.70	2.80
e	—	0.40	—
h	0.25	0.30	0.35
K	—	0.30	—
L	0.30	0.35	0.40
Nd	—	2.80	—
Ne	—	2.80	—

(Original dimensions are in millimeters)

Figure 5-12. QFN32/QFN32 VREFP recommended footprint



(Original dimensions are in millimeters)

5.7 WLCSP25 package outline dimensions

Figure 5-13. WLCSP25 package outline

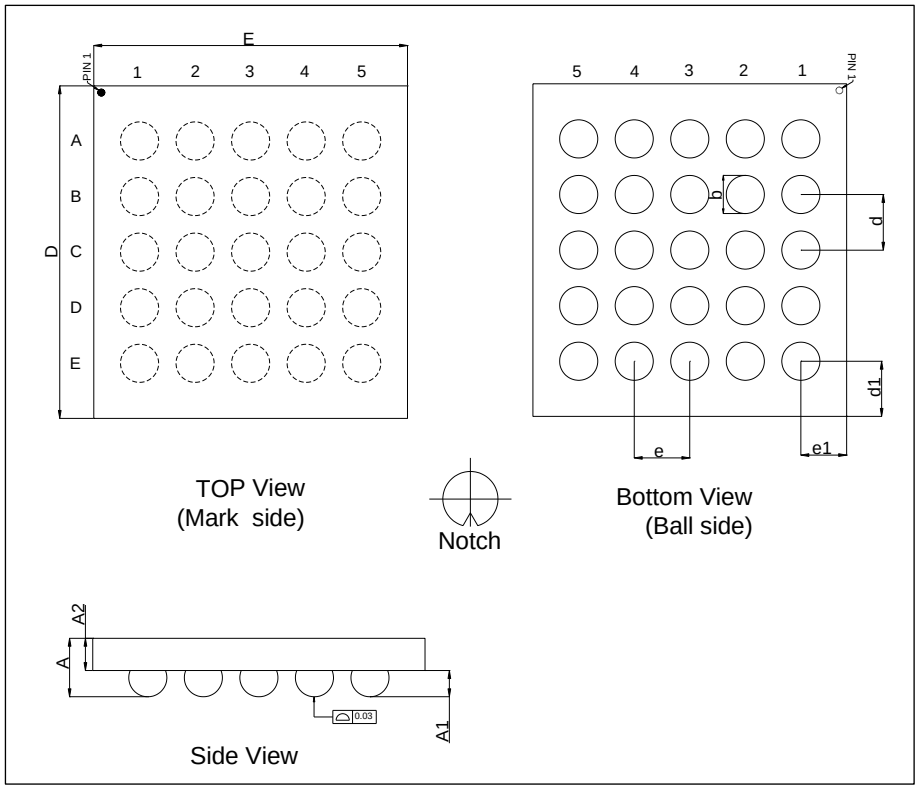
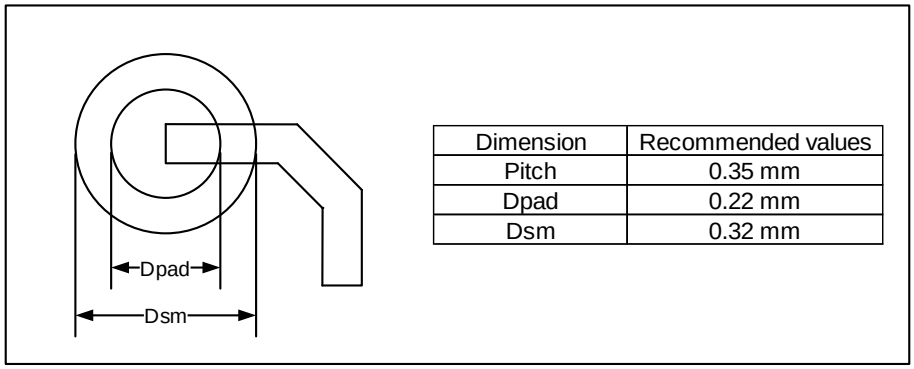


Table 5-7. WLCSP25 package dimensions

Symbol	Min	Typ	Max
A	0.440	0.470	0.500
A1	0.153	0.170	0.187
A2	0.287	0.300	0.313
b	0.216	0.240	0.264
D	2.077	2.092	2.107
E	1.960	1.975	1.990
d		0.350	
d1		0.346	
e	—	0.350	—
e1	—	0.287	—

(Original dimensions are in millimeters)

Figure 5-14. WLCSP25 recommended footprint



Dimension	Recommended values
Pitch	0.35 mm
Dpad	0.22 mm
Dsm	0.32 mm

(Original dimensions are in millimeters)

5.8 Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter "θ". For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

θ_{JA}: Thermal resistance, junction-to-ambient.

θ_{JB}: Thermal resistance, junction-to-board.

θ_{JC}: Thermal resistance, junction-to-case.

Ψ_{JB}: Thermal characterization parameter, junction-to-board.

Ψ_{JT}: Thermal characterization parameter, junction-to-top center.

$$\theta_{JA}=(T_J-T_A)/P_D \quad (5\text{-}1)$$

$$\theta_{JB}=(T_J-T_B)/P_D \quad (5\text{-}2)$$

$$\theta_{JC}=(T_J-T_C)/P_D \quad (5\text{-}3)$$

Where, T_J = Junction temperature.

T_A = Ambient temperature

T_B = Board temperature

T_C = Case temperature which is monitoring on package surface

P_D = Total power dissipation

θ_{JA} represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower θ_{JA} can be considerate as better overall thermal performance. θ_{JA} is generally used to estimate junction temperature.

θ_{JB} is used to measure the heat flow resistance between the chip surface and the PCB board.

θ_{JC} represents the thermal resistance between the chip surface and the package top case. θ_{JC} is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

Table 5-8. Package thermal characteristics(1)

Symbol	Condition	Package	Value	Unit
θ_{JA}	Natural convection, 2S2P PCB	LQFP64	54.57	°C/W
		QFN64	38.32	
		LQFP48	69.64	
		QFN48	42.58	
		LQFP32	55.26	
		QFN32	42.57	
		WLCSP25	70.14	
θ_{JB}	Cold plate, 2S2P PCB	LQFP64	35.08	°C/W

Symbol	Condition	Package	Value	Unit
		QFN64	17.23	
		LQFP48	43.16	
		QFN48	12.22	
		LQFP32	26.24	
		QFN32	19.21	
		WLCSP25	18.25	
θ_{JC}	Cold plate, 2S2P PCB	LQFP64	18.11	°C/W
		QFN64	13.28	
		LQFP48	25.36	
		QFN48	16.76	
		LQFP32	25.23	
		QFN32	19.10	
		WLCSP25	0.58	
Ψ_{JB}	Natural convection, 2S2P PCB	LQFP64	35.41	°C/W
		QFN64	17.48	
		LQFP48	47.75	
		QFN48	12.81	
		LQFP32	32.03	
		QFN32	19.18	
		WLCSP25	19.66	
Ψ_{JT}	Natural convection, 2S2P PCB	LQFP64	1.10	°C/W
		QFN64	2.90	
		LQFP48	2.45	
		QFN48	0.69	
		LQFP32	2.06	
		QFN32	0.62	
		WLCSP25	0.70	

(1) Thermal characteristics are based on simulation, and meet JEDEC specification.

6 Ordering information

Table 6-1. Part ordering code for GD32L235xx devices

Ordering code	Flash (KB)	Package	Package type	Temperature operating range
GD32L235RBT6	128	LQFP64	Green	Industrial -40°C to +85°C
GD32L235RBT7	128	LQFP64	Green	Industrial -40°C to +105°C
GD32L235R8T6	64	LQFP64	Green	Industrial -40°C to +85°C
GD32L235RBO6	128	QFN64	Green	Industrial -40°C to +85°C
GD32L235R8O6	64	QFN64	Green	Industrial -40°C to +85°C
GD32L235CBT6	128	LQFP48	Green	Industrial -40°C to +85°C
GD32L235CBT7	128	LQFP48	Green	Industrial -40°C to +105°C
GD32L235C8T6	64	LQFP48	Green	Industrial -40°C to +85°C
GD32L235CBO6	128	QFN48	Green	Industrial -40°C to +85°C
GD32L235C8O6	64	QFN48	Green	Industrial -40°C to +85°C
GD32L235KBT6	128	LQFP32	Green	Industrial -40°C to +85°C
GD32L235K8T6	64	LQFP32	Green	Industrial -40°C to +85°C
GD32L235KBQ6	128	QFN32	Green	Industrial -40°C to +85°C
GD32L235KBQ7	128	QFN32	Green	Industrial -40°C to +105°C
GD32L235K8Q6	64	QFN32	Green	Industrial -40°C to +85°C
GD32L235K8Q7	64	QFN32	Green	Industrial -40°C to +105°C
GD32L235KBQ6P	128	QFN32	Green	Industrial -40°C to +85°C
GD32L235K8Q6P	64	QFN32	Green	Industrial -40°C to +85°C
GD32L235EBY6	128	WLCSP25	Green	Industrial -40°C to +85°C

Ordering code	Flash (KB)	Package	Package type	Temperature operating range
GD32L235E8Y6	64	WLCSP25	Green	Industrial -40°C to +85°C

7 Revision history

Table 7-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Mar. 29, 2024
1.1	Update the pin number order of GD32L235KxxxP in ***Figure 2 8. GD32L235KxxxP QFN32 VREFP pinouts*** and ***Table 2-10. GD32L235KxxxP QFN32 VREFP pin definitions***.	Apr. 8, 2024
1.2	1. Add GD32L235CBT7 information in ***Table 2-1 \ Table 4-2 \ Table 4-23 \ Table 4-24 \ Table 4-25 \ Table 4-27.*** 2. Add coplanarity information for all POD diagram. 3.Update PA8 pin definition.	June. 13, 2024
1.3	1. Add GD32L235K8Q7 information in ***Table 2-1 \ 3.27 Package and operation temperature \ 6 Ordering information \ 4.1 Absolute maximum ratings .*** 2. Add the comment of VREFP of ***Table 4 33. ADC characteristics***. 3.Add Min and Max parameters of ***Table 4-31. Output voltage characteristics for all I/Os except PC13, PC14, PC15.***	Nov. 8, 2024
1.4	1. Add GD32L235RBT7 information in ***Table 2-1 \ 3.27 Package and operation temperature \ 6 Ordering information.*** 2. Change “DAC_OUT” to “DAC0_OUT0” in ***2.6. Pin definitions***. 3. Remove the maximum rate in the description of SPI ***in 3.19. Serial peripheral interface (SPI)*** (refer to ***Table 4 45. Standard SPI characteristics*** if needed). 4. Modify the description of the maximum rate for USART\UART in ***3.16. Universal synchronous/asynchronous receiver transmitter (USART/UART)***. 5. Modify the description of the maximum rate for LPUART in ***3.17. Universal asynchronous receiver transmitter (LPUART)***. 6. Add $Drift_{IRC16M}$, $Drift_{IRC48M}$, and f_{IRC32K} data under the conditions of VDD = VDDA = 3.3 V, TA = -40 °C ~ +105 °C in ***Table 4 23. High speed internal clock (IRC16M) characteristics \ Table 4 24. High speed internal clock (IRC48M) characteristics \ Table 4 25. Low speed internal clock (IRC32K) characteristics***.	Jan.2, 2025
1.5	1. Modify USART pin function description from USARTx_RTS to USARTx_RTS/USARTx_DE and modify TIMER pin function description from TIMER1_CH0_ETI to TIMER1_CH0,	Feb.8, 2025

Revision No.	Description	Date
	TIMER1_ETI in ***Pin definitions***. 2. Add GD32L235KBQ7 information in ***Table 2-1 \ 6 Ordering information.***	
2.0	1. Modify VDD maximum value from VSS+3.63V to VSS+4.0V, modify VDDA maximum value from VSS+3.63V to VSS+4.0V, modify VBAT maximum value from VSS+3.63V to VSS+4.0V, modify VIN 5T maximum value from VDD+3.63V to VDD+4.0V, modify VIN N5T maximum value from 3.63V to 4.0V in ***Table 4 2. Absolute maximum ratings***. 2. Update the Typ and Max values of the power consumption data to "by characterization" data of ***Table 4 8. Power consumption in Run mode*** \ ***Table 4 9. Power consumption in Run mode with different codes*** \ ***Table 4 10. Power consumption in Sleep mode*** \ ***Table 4 11. Power consumption in Deep-sleep mode*** \ ***Table 4 12. Power consumption in Standby mode***. Update the data to "by sample" data at 105℃ of ***Table 4 13. Power consumption in BKP_ONLY mode***. 3. Fill in the I_{LEAK} parameter with min = -2μA and max = 2μA in ***Table 4 30. I/O static characteristics***.	Apr.3, 2025
2.1	1. Modify Flash accesses from 0~3 to 0~2 wait states in ***1. General description***. 2. Update the POD and pinouts of WLCSP25 package by rotating it 90 degrees to the right in ***5.7 WLCSP25 package outline dimensions*** and ***Figure 2 9. GD32L235Ex WLCSP25 pinouts***.	Aug.8, 2025
2.2	1. Modify the number of GPIOs for WLCSP25: 23 to 22 in ***Table 2 1. GD32L235xx devices features and peripheral list***. 2. Modify the 1.1V domain to the Vcore domain in ***3.5. Power saving modes***. 3. Modify the description of the ADC input voltage in ***3.12. Analog to digital converter (ADC)***. 4. Add Vcore parameter and add a footnote of V_{BAT} "(3) When both VDD and VBAT are powered simultaneously, it is required that VBAT ≤ VDD + 0.3 V. " in ***Table 4 3. DC operating conditions***.	Jan.19, 2026

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