GigaDevice Semiconductor Inc.

GD32G553xx
Arm® Cortex®-M33 32-bit MCU

Datasheet

Revision 2.0

(Mar. 2026)

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1. General description

The GD32G553xx device belongs to the high-performance line of GD32 MCU family. It is a new 32-bit general-purpose microcontroller based on the Arm® Cortex®-M33 core. The Cortex®-M33 processor is a 32-bit processor that possesses low interrupt latency and low-cost debug. The characteristics of integrated and advanced make the Cortex®-M33 processor suitable for market products that require microcontrollers with high performance and low power consumption. The Cortex®-M33 processor is based on the Armv8 architecture and supports a powerful and scalable instruction set including general data processing I/O control tasks, advanced data processing bit field manipulations and DSP.

For GD32G553xxx7, the GD32G553xx device incorporates the Arm® Cortex®-M33 32-bit processor core operating at 216 MHz frequency with Flash security protection to prevent illegal code/data access. For GD32G553xxx3, the GD32G553xx device incorporates the Arm® Cortex®-M33 32-bit processor core operating at 170 MHz frequency with Flash security protection to prevent illegal code/data access. It provides up to 512 KB on-chip Flash memory, 80KB SRAM0, 16KB SRAM1 and 32KB TCMSRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer up to four 12-bit ADCs, eight 12-bit DAC, up to five general 16-bit timers, three 16-bit PWM advanced timers, two 32-bit general timers, and two 16-bit basic timers, a low power timer (LPTIMER), a high-resolution timer (HRTIMER), as well as standard and advanced communication interfaces: up to three SPIs, a QSPI, four I2Cs, three USARTs and two UARTs, three CANs. Additional peripherals as an EXMC interface, up to eight comparators (CMP), a cryptographic acceleration unit (CAU), CRC calculation unit (CRC), configurable logic array (CLA), true random number generator (TRNG), trigonometric math unit (TMU), VREF, high-performance digital filter (HPDF), filter arithmetic accelerator (FAC), filter fourier transform (FFT) and a trigger selection controller (TRIGSEL) are included.

For GD32G553xxx7, the device operates from a 1.71V to 3.6V power supply and available in –40 to +105 °C temperature range. For GD32G553xxx3, the device operates from a 1.71V to 3.6V power supply and available in –40 to +125 °C temperature range. Three power saving modes provide the flexibility for maximum optimization of power consumption, an especially important consideration in low power applications.

The above features make GD32G553xx devices suitable for a wide range of interconnection and advanced applications, especially in areas such as industrial control, consumer and handheld equipment, embedded modules, human machine interface, security and alarm systems, graphic display, audio player, automotive navigation, drone, IoT and so on.

2. Device overview

2.1. Device information

Table 2-1. GD32G553xx devices features and peripheral list

Part Number		GD32G553												
		QET7	QET3(1)	VET7	VET3(1)	MEY7TR	MET7	MET3(1)	RET7	RET3(1)	CET7	CET3(1)	CEU7	CEU3(1)
FLASH (KB)		512	512	512	512	512	512	512	512	512	512	512	512	512
SRAM (KB)	SRAM0	80	80	80	80	80	80	80	80	80	80	80	80	80
	SRAM1	16	16	16	16	16	16	16	16	16	16	16	16	16
	TCMSRAM	32	32	32	32	32	32	32	32	32	32	32	32	32
	Total	128	128	128	128	128	128	128	128	128	128	128	128	128
Timers	General timer (16-bit)	5 (2-3,14-16)	5 (2-3,14-16)	5 (2-3,14-16)	5 (2-3,14-16)	5 (2-3,14-16)	5 (2-3,14-16)	5 (2-3,14-16)	5 (2-3,14-16)	5 (2-3,14-16)	5 (2-3,14-16)	5 (2-3,14-16)	5 (2-3,14-16)	5 (2-3,14-16)
	General timer (32-bit)	2 (1,4)	2 (1,4)	2 (1,4)	2 (1,4)	2 (1,4)	2 (1,4)	2 (1,4)	2 (1,4)	2 (1,4)	2 (1,4)	2 (1,4)	2 (1,4)	2 (1,4)
	Advanced timer(16-bit)	3 (0,7,19)	3 (0,7,19)	3 (0,7,19)	3 (0,7,19)	3 (0,7,19)	3 (0,7,19)	3 (0,7,19)	3 (0,7,19)	3 (0,7,19)	3 (0,7,19)	3 (0,7,19)	3 (0,7,19)	3 (0,7,19)
	Basic timer (16-bit)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)
	HRTIMER	1	1	1	1	1	1	1	1	1	1	1	1	1
	LPTIMER	1	1	1	1	1	1	1	1	1	1	1	1	1
	SysTick	1	1	1	1	1	1	1	1	1	1	1	1	1

Part Number		GD32G553												
		QET7	QET3(1)	VET7	VET3(1)	MEY7TR	MET7	MET3(1)	RET7	RET3(1)	CET7	CET3(1)	CEU7	CEU3(1)
	Watchdog	2	2	2	2	2	2	2	2	2	2	2	2	2
	RTC	1	1	1	1	1	1	1	1	1	1	1	1	1
Connectivity	USART	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)
	UART	2 (3,4)	2 (3,4)	2 (3,4)	2 (3,4)	2 (3,4)	2 (3,4)	2 (3,4)	2 (3,4)	2 (3,4)	2 (3,4)	2 (3,4)	2 (3,4)	2 (3,4)
	I2C	4 (0-3)	4 (0-3)	4 (0-3)	4 (0-3)	4 (0-3)	4 (0-3)	4 (0-3)	4 (0-3)	4 (0-3)	4 (0-3)	4 (0-3)	4 (0-3)	4 (0-3)
	SPI	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)
	QSPI	1	1	1	1	1	1	1	1	1	1	1	1	1
	CAN	3xFD	3xFD	3xFD	3xFD	3xFD	3xFD	3xFD	3xFD	3xFD	3xFD	3xFD	3xFD	3xFD
GPIO		107	107	86	86	67	66	66	52	52	38	38	42	42
EXMC		1	1	1	1	1	1	1	0	0	0	0	0	0
CAU		1	1	1	1	1	1	1	1	1	1	1	1	1
TRIGSEL		1	1	1	1	1	1	1	1	1	1	1	1	1
CRC		1	1	1	1	1	1	1	1	1	1	1	1	1
CLA		1	1	1	1	1	1	1	1	1	1	1	1	1
TRNG		1	1	1	1	1	1	1	1	1	1	1	1	1
TMU		1	1	1	1	1	1	1	1	1	1	1	1	1
VREF		1	1	1	1	1	1	1	1	1	1	1	1	1

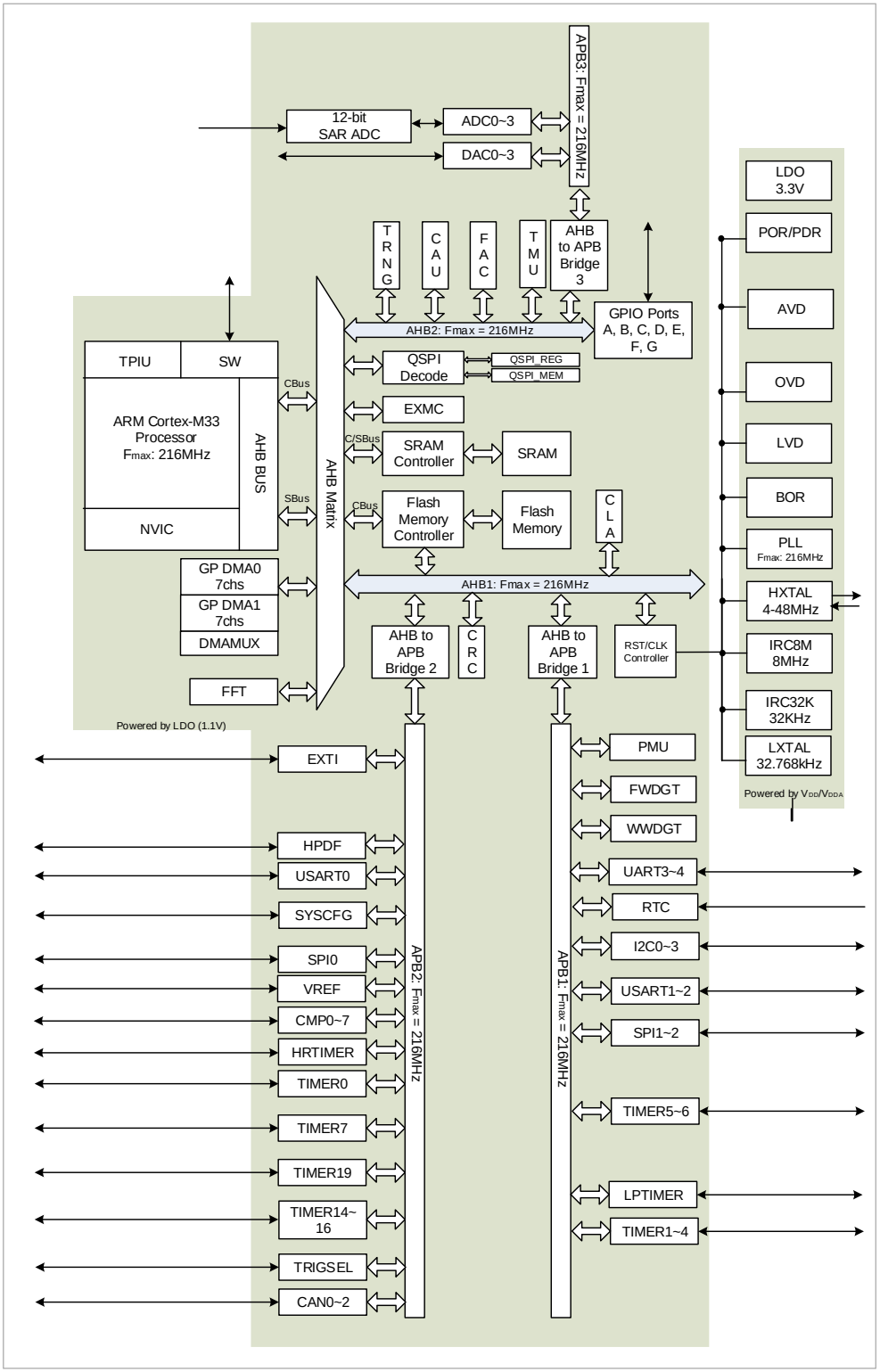
Part Number		GD32G553												
		QET7	QET3(1)	VET7	VET3(1)	MEY7TR	MET7	MET3(1)	RET7	RET3(1)	CET7	CET3(1)	CEU7	CEU3(1)
HPDF		1	1	1	1	1	1	1	1	1	1	1	1	1
FAC		1	1	1	1	1	1	1	1	1	1	1	1	1
FFT		1	1	1	1	1	1	1	1	1	1	1	1	1
12bit ADC	Units	4	4	4	4	4	4	4	4	4	4	4	4	4
	Channels	42	42	42	42	39	38	38	26	26	20	20	21	21
DAC		8	8	8	8	8	8	8	8	8	8	8	8	8
CMP		8	8	8	8	8	8	8	7	7	7	7	7	7
Package		LQFP128		LQFP100		WLCSP81	LQFP80		LQFP64		LQFP48		QFN48	

Note:

(1) For GD32G553xxx3 devices, the maximum frequency of the system clock is 170MHz.

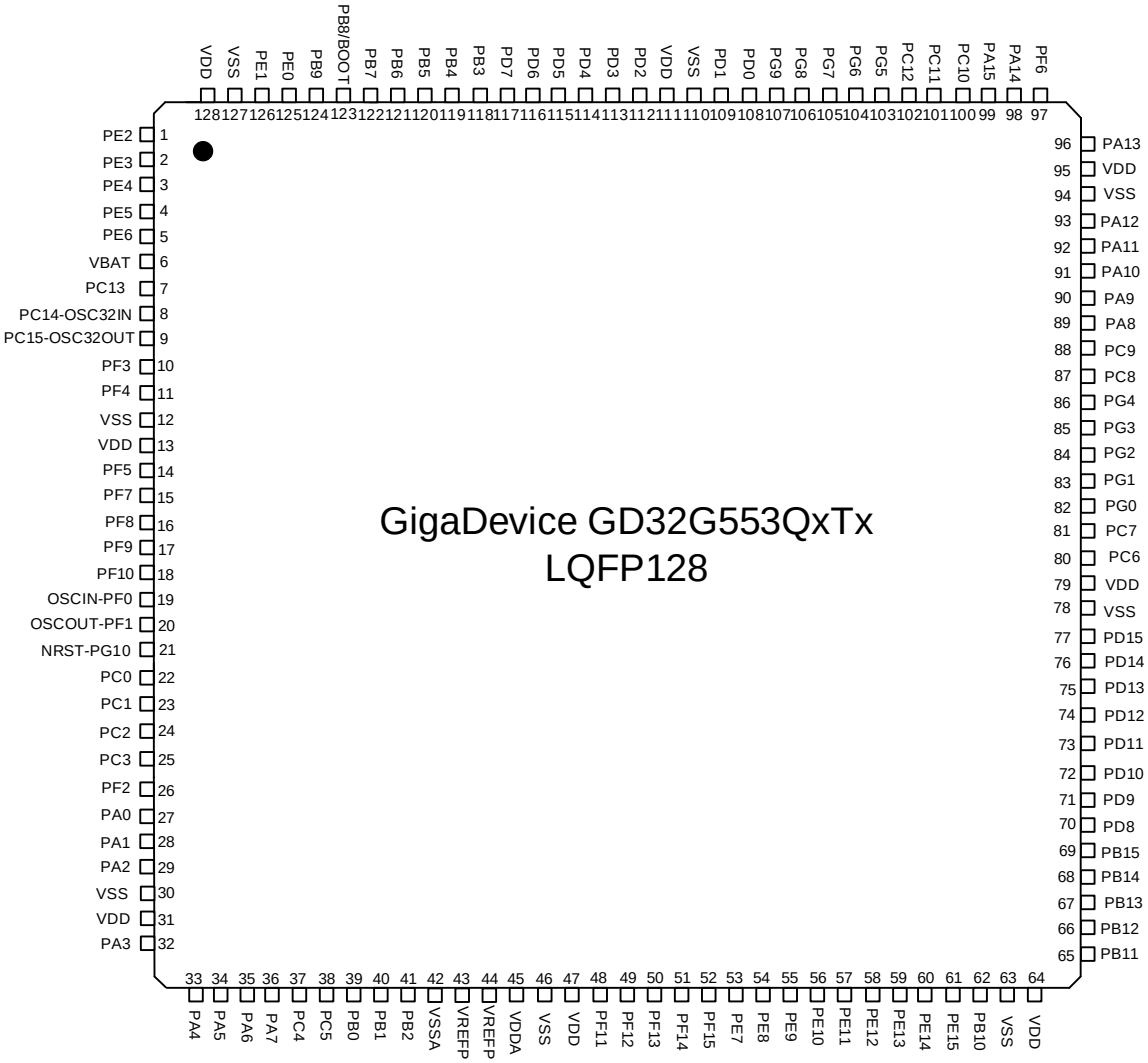
2.2. Block diagram

Figure 2-1. GD32G553xx block diagram



2.3. Pinouts and pin assignment

Figure 2-2. GD32G553QxTx LQFP128 pinouts(1)



(1) The above figure shows the package top view.

Figure 2-3. GD32G553VxTx LQFP100 pinouts(1)

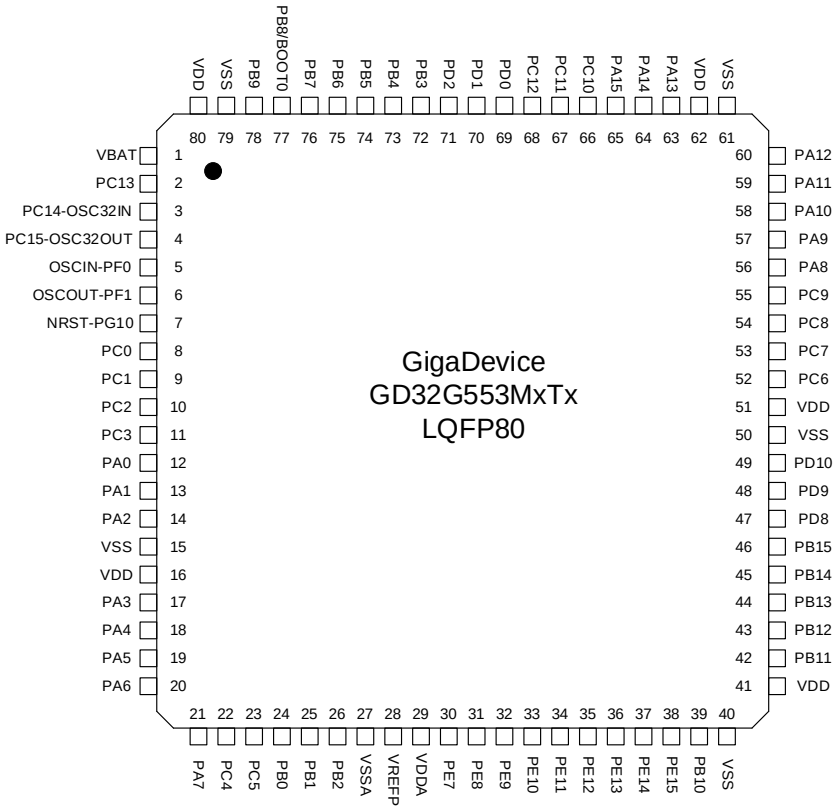
(1) The above figure shows the package top view.

Figure 2-4. GD32G553MxY7TR WLCSP81 pinouts(1)

	1	2	3	4	5	6	7	8	9
A	VDD	PA15	PC12	PD1	PB3	PB5	PB9	VSS	VDD
B	VSS	PA13	PC10	PD0	PD2	PB6	PB8 /BOOT0	PC13	VBAT
C	PA12	PA11	PA14	PC11	PC8	PB4	PB7	PC1	PC14-OSC32IN
D	PA8	PC9	PA10	PA9	PC7	PA4	PA0	NRST-PG10	PC15-OSC32OUT
E	VDD	PD11	PC6	PB15	PE12	PC4	PA1	PC0	OSCIN-PF0
F	VSS	PD10	PD9	PE15	PE9	PB0	PA5	PC2	OSCOUT-PF1
G	PD8	PB14	PB12	PE13	PE8	PB1	PA6	PA2	PC3
H	PB13	PB11	PB10	PE11	PE7	VSSA	PC5	PA3	VSS
J	VDD	VSS	PE14	PE10	VDDA	VREFP	PB2	PA7	VDD

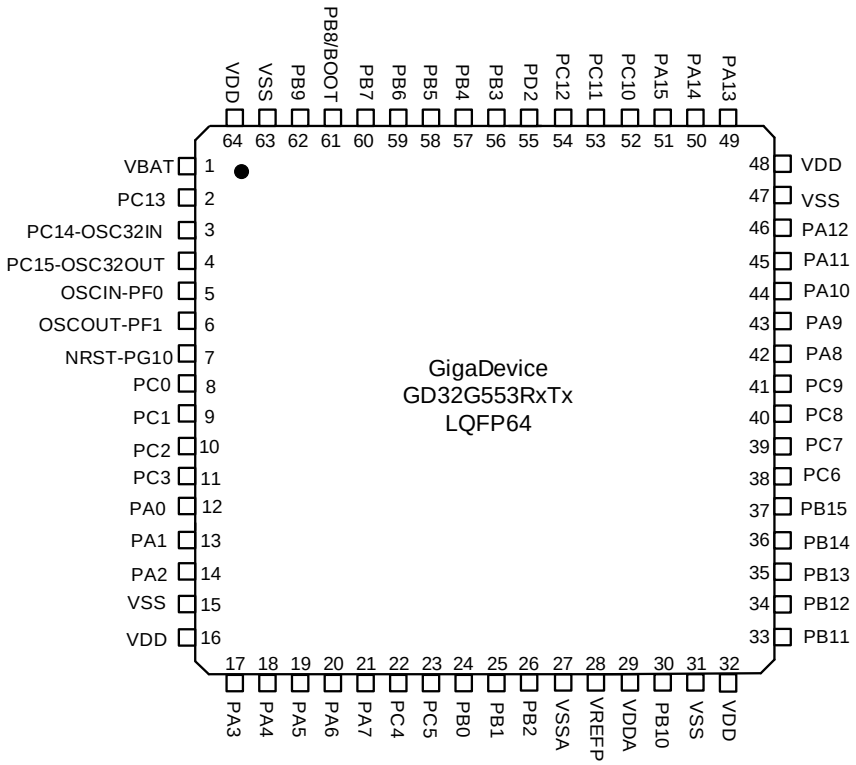
(1) The above figure shows the package top view.

Figure 2-5. GD32G553MxTx LQFP80 pinouts(1)



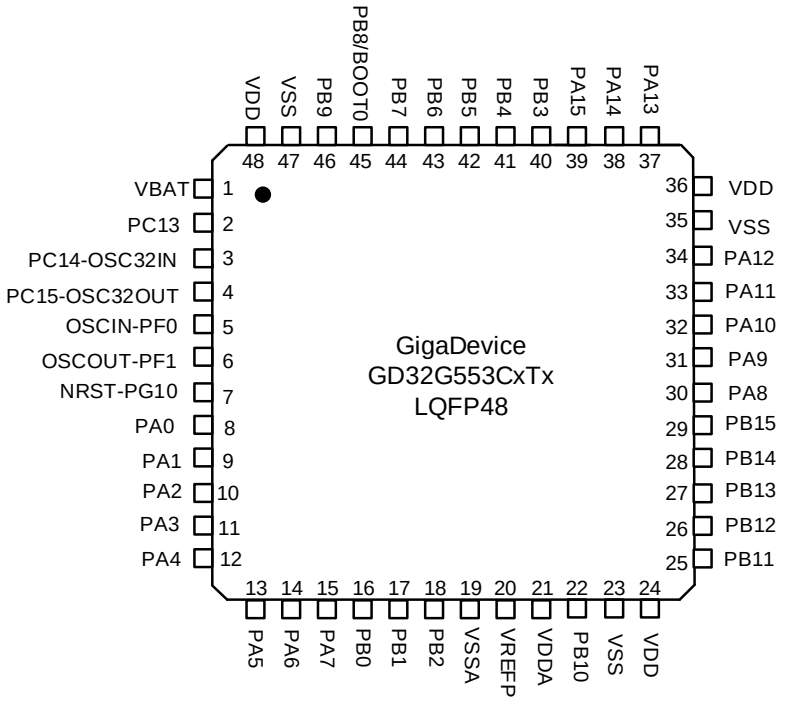
(1) The above figure shows the package top view.

Figure 2-6. GD32G553RxTx LQFP64 pinouts(1)



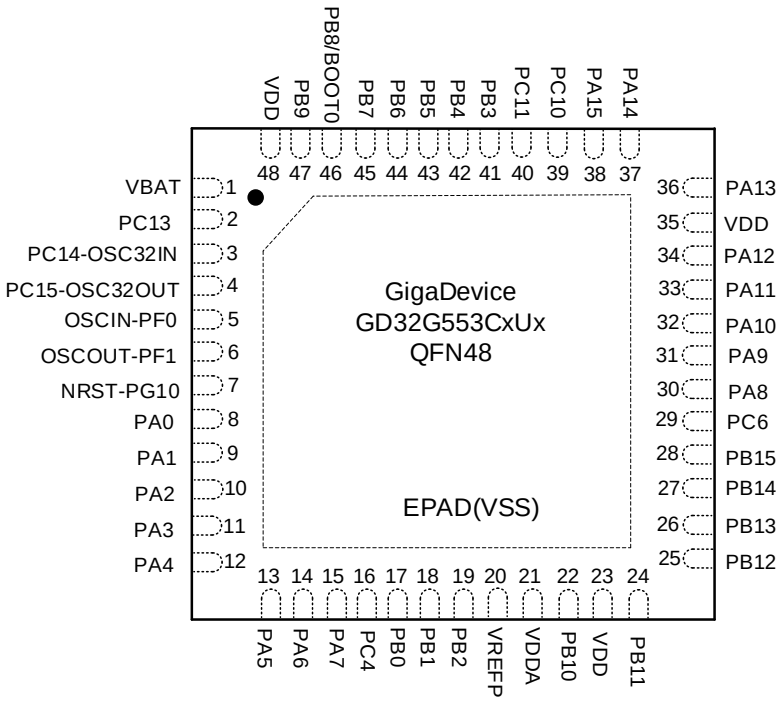
(1) The above figure shows the package top view.

Figure 2-7. GD32G553CxTx LQFP48 pinouts(1)



(1) The above figure shows the package top view.

Figure 2-8. GD32G553CxUx QFN48 pinouts(1)(2)



(1) The above figure shows the package top view.

(2) The EPAD is internally connected to VSS.

2.4. Memory map

Table 2-2. GD32G553xx memory map

Pre-defined Regions	Bus	Address	Peripherals
External RAM		0xD000 0000 - 0xDFFF FFFF	Reserved
		0xC000 0000 - 0xCFFF FFFF	Reserved
		0xA000 1400 - 0xBFFF FFFF	Reserved
		0xA000 1000 - 0xA000 13FF	QSPI- REG
		0xA000 0400 - 0xA000 0FFF	EXMC - SWREG
		0xA000 0000 - 0xA000 03FF	
		0x9000 0000 - 0x9FFF FFFF	QSPI- MEM
		0x8000 0000 - 0x8FFF FFFF	Reserved
		0x7000 0000 - 0x7FFF FFFF	Reserved
		0x6000 0000 - 0x6FFF FFFF	EXMC - NOR/PSRAM/SRAM
Peripheral	AHB1	0x5001 0000 - 0x5FFF FFFF	Reserved
		0x5000 4000 - 0x5000 FFFF	Reserved
		0x5000 3000 - 0x5000 3FFF	Reserved
		0x5000 2000 - 0x5000 2FFF	Reserved
	APB3	0x5000 1C00 - 0x5000 1FFF	DAC3
		0x5000 1800 - 0x5000 1BFF	DAC2
		0x5000 1400 - 0x5000 17FF	DAC1
		0x5000 1000 - 0x5000 13FF	DAC0
		0x5000 0C00 - 0x5000 0FFF	ADC3
		0x5000 0800 - 0x5000 0BFF	ADC2
		0x5000 0400 - 0x5000 07FF	ADC1
		0x5000 0000 - 0x5000 03FF	ADC0
	AHB2	0x4802 5000 - 0x4FFF FFFF	Reserved
		0x4802 4800 - 0x4802 4FFF	FAC
		0x4802 4400 - 0x4802 47FF	TMU
		0x4802 4000 - 0x4802 43FF	Reserved
		0x4802 3000 - 0x4802 3FFF	Reserved
		0x4802 2C00 - 0x4802 2FFF	Reserved
		0x4802 2800 - 0x4802 2BFF	CPDM
		0x4802 2400 - 0x4802 27FF	Reserved
		0x4802 1C00 - 0x4802 23FF	Reserved
		0x4802 1800 - 0x4802 1BFF	TRNG
		0x4802 1400 - 0x4802 17FF	Reserved
		0x4802 1000 - 0x4802 13FF	CAU
		0x4802 0400 - 0x4802 0FFF	Reserved
		0x4800 1C00 - 0x4802 03FF	Reserved

Pre-defined Regions	Bus	Address	Peripherals
		0x4800 1800 - 0x4800 1BFF	GPIOG
		0x4800 1400 - 0x4800 17FF	GPIOF
		0x4800 1000 - 0x4800 13FF	GPIOE
		0x4800 0C00 - 0x4800 0FFF	GPIOD
		0x4800 0800 - 0x4800 0BFF	GPIOC
		0x4800 0400 - 0x4800 07FF	GPIOB
		0x4800 0000 - 0x4800 03FF	GPIOA
	AHB1	0x4003 8400 - 0x47FF FFFF	Reserved
		0x4003 8000 - 0x4003 83FF	CLA
		0x4002 7800 - 0x4003 7FFF	Reserved
		0x4002 5000 - 0x4002 77FF	FFT
		0x4002 3400 - 0x4002 4FFF	Reserved
		0x4002 3000 - 0x4002 33FF	CRC
		0x4002 2400 - 0x4002 2FFF	Reserved
		0x4002 2000 - 0x4002 23FF	FMC
		0x4002 1C00 - 0x4002 1FFF	Reserved
		0x4002 1800 - 0x4002 1BFF	Reserved
		0x4002 1400 - 0x4002 17FF	Reserved
		0x4002 1000 - 0x4002 13FF	RCU
		0x4002 0C00 - 0x4002 0FFF	Reserved
		0x4002 0800 - 0x4002 0BFF	DMAMUX
		0x4002 0400 - 0x4002 07FF	DMA1
		0x4002 0000 - 0x4002 03FF	DMA0
	APB2	0x4001 D000 - 0x4001 FFFF	Reserved
		0x4001 C000 - 0x4001 CFFF	CAN2
		0x4001 B000 - 0x4001 BFFF	CAN1
		0x4001 A000 - 0x4001 AFFF	CAN0
		0x4001 8800 - 0x4001 9FFF	Reserved
		0x4001 8400 - 0x4001 87FF	TRIGSEL
		0x4001 8000 - 0x4001 83FF	Reserved
		0x4001 7C00 - 0x4001 7FFF	CMP
		0x4001 7800 - 0x4001 7BFF	VREF
		0x4001 7400 - 0x4001 77FF	Reserved
		0x4001 7000 - 0x4001 73FF	HPDF
		0x4001 6800 - 0x4001 6FFF	Reserved
		0x4001 5800 - 0x4001 67FF	HRTIMER
		0x4001 5400 - 0x4001 57FF	Reserved
		0x4001 5000 - 0x4001 53FF	TIMER19
		0x4001 4C00 - 0x4001 4FFF	Reserved
		0x4001 4800 - 0x4001 4BFF	TIMER16
		0x4001 4400 - 0x4001 47FF	TIMER15

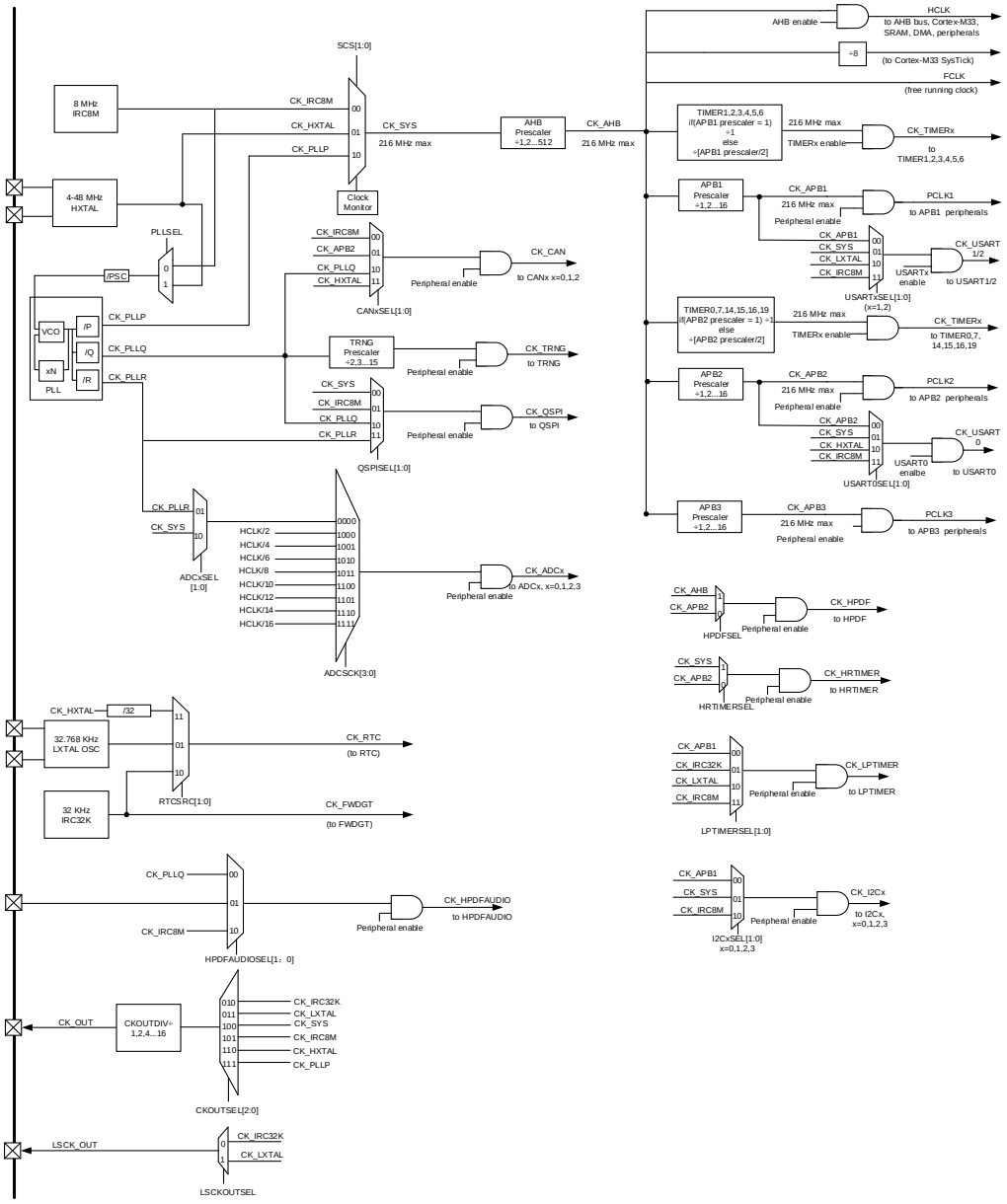
Pre-defined Regions	Bus	Address	Peripherals
		0x4001 4000 - 0x4001 43FF	TIMER14
		0x4001 3C00 - 0x4001 3FFF	Reserved
		0x4001 3800 - 0x4001 3BFF	USART0
		0x4001 3400 - 0x4001 37FF	TIMER7
		0x4001 3000 - 0x4001 33FF	SPI0
		0x4001 2C00 - 0x4001 2FFF	TIMER0
		0x4001 2800 - 0x4001 2BFF	Reserved
		0x4001 2400 - 0x4001 27FF	Reserved
		0x4001 2000 - 0x4001 23FF	Reserved
		0x4001 1C00 - 0x4001 1FFF	Reserved
		0x4001 1800 - 0x4001 1BFF	Reserved
		0x4001 1400 - 0x4001 17FF	Reserved
		0x4001 1000 - 0x4001 13FF	Reserved
		0x4001 0C00 - 0x4001 0FFF	Reserved
		0x4001 0800 - 0x4001 0BFF	Reserved
		0x4001 0400 - 0x4001 07FF	EXTI
		0x4001 0000 - 0x4001 03FF	SYSCFG
	APB1	0x4000 DC00 - 0x4000 FFFF	Reserved
		0x4000 D800 - 0x4000 DBFF	Reserved
		0x4000 D400 - 0x4000 D7FF	Reserved
		0x4000 D000 - 0x4000 D3FF	Reserved
		0x4000 CC00 - 0x4000 CFFF	Reserved
		0x4000 C800 - 0x4000 CBFF	Reserved
		0x4000 C400 - 0x4000 C7FF	Reserved
		0x4000 C000 - 0x4000 C3FF	I2C2
		0x4000 9800 - 0x4000 BFFF	Reserved
		0x4000 9400 - 0x4000 97FF	LPTIMER
		0x4000 8400 - 0x4000 93FF	Reserved
		0x4000 8000 - 0x4000 83FF	Reserved
		0x4000 7C00 - 0x4000 7FFF	Reserved
		0x4000 7800 - 0x4000 7BFF	Reserved
		0x4000 7400 - 0x4000 77FF	Reserved
		0x4000 7000 - 0x4000 73FF	PMU
		0x4000 6C00 - 0x4000 6FFF	Reserved
		0x4000 6800 - 0x4000 6BFF	Reserved
		0x4000 6400 - 0x4000 67FF	Reserved
		0x4000 6000 - 0x4000 63FF	Reserved
		0x4000 5C00 - 0x4000 5FFF	I2C3
		0x4000 5800 - 0x4000 5BFF	I2C1
		0x4000 5400 - 0x4000 57FF	I2C0
		0x4000 5000 - 0x4000 53FF	UART4

Pre-defined Regions	Bus	Address	Peripherals
		0x4000 4C00 - 0x4000 4FFF	UART3
		0x4000 4800 - 0x4000 4BFF	USART2
		0x4000 4400 - 0x4000 47FF	USART1
		0x4000 4000 - 0x4000 43FF	Reserved
		0x4000 3C00 - 0x4000 3FFF	SPI2
		0x4000 3800 - 0x4000 3BFF	SPI1
		0x4000 3400 - 0x4000 37FF	Reserved
		0x4000 3000 - 0x4000 33FF	FWDGT
		0x4000 2C00 - 0x4000 2FFF	WWDGT
		0x4000 2800 - 0x4000 2BFF	RTC
		0x4000 2400 - 0x4000 27FF	Reserved
		0x4000 2000 - 0x4000 23FF	Reserved
		0x4000 1C00 - 0x4000 1FFF	Reserved
		0x4000 1800 - 0x4000 1BFF	Reserved
		0x4000 1400 - 0x4000 17FF	TIMER6
		0x4000 1000 - 0x4000 13FF	TIMER5
		0x4000 0C00 - 0x4000 0FFF	TIMER4
		0x4000 0800 - 0x4000 0BFF	TIMER3
		0x4000 0400 - 0x4000 07FF	TIMER2
		0x4000 0000 - 0x4000 03FF	TIMER1
SRAM		0x2002 0000 - 0x3FFF FFFF	Reserved
		0x2001 C000 - 0x2001 FFFF	TCMSRAM aliased(32KB)
		0x2001 8000 - 0x2001 BFFF	
		0x2001 4000 - 0x2001 7FFF	SRAM1(16KB)
		0x2000 D000 - 0x2001 3FFF	SRAM0(80KB)
		0x2000 C000 - 0x2000 CFFF	
		0x2000 8000 - 0x2000 BFFF	
		0x2000 5000 - 0x2000 7FFF	
		0x2000 2000 - 0x2000 4FFF	
		0x2000 1000 - 0x2000 1FFF	
		0x2000 0000 - 0x2000 0FFF	
Code		0x1FFF FC10 - 0x1FFF FFFF	Reserved
		0x1FFF FC00 - 0x1FFF FC0F	Reserved
		0x1FFF F830 - 0x1FFF BFFF	Reserved
		0x1FFF F800 - 0x1FFF F82F	Option Bytes
		0x1FFF C000 - 0x1FFF F7FF	Reserved
		0x1FFF 8000 - 0x1FFF BFFF	System memory 1
		0x1FFF 7830 - 0x1FFF 7FFF	Reserved
		0x1FFF 7800 - 0x1FFF 782F	Option Bytes
		0x1FFF 7000 - 0x1FFF 77FF	OTP
		0x1FFF 3400 - 0x1FFF 6FFF	Reserved

Pre-defined Regions	Bus	Address	Peripherals
		0x1FFF 0000 - 0x1FFF 33FF	System memory 0
		0x1000 8000 - 0x1FFE FFFF	Reserved
		0x1000 0000 - 0x1000 7FFF	TCMSRAM
		0x0A00 8000 - 0x0FFF FFFF	Reserved
		0x0A00 6000 - 0x0A00 7FFF	Reserved
		0x0A00 4000 - 0x0A00 5FFF	Reserved
		0x0A00 0000 - 0x0A00 3FFF	Reserved
		0x08C0 1000 - 0x09FF FFFF	Reserved
		0x08C0 0000 - 0x08C0 0FFF	Reserved
		0x0881 0000 - 0x08BF FFFF	Reserved
		0x0880 0000 - 0x0880 FFFF	Reserved
		0x0808 0000 - 0x0871 FFFF	Reserved
		0x0806 0000 - 0x0807 FFFF	Main Flash memory
		0x0802 0000 - 0x0805 FFFF	
		0x0801 0000 - 0x0801 FFFF	
		0x0800 0000 - 0x0800 FFFF	
		0x0006 0000 - 0x07FF FFFF	Reserved
		0x0002 0000 - 0x0007 FFFF	Aliased to Flash or system memory
		0x0001 0000 - 0x0001 FFFF	
		0x0000 0000 - 0x0000 FFFF	

2.5. Clock tree

Figure 2-9. GD32G553xx clock tree



Legend:

HXTAL: High speed crystal oscillator

LXTAL: Low speed crystal oscillator

IRC8M: Internal 8M RC oscillators

IRC32K: Internal 32K RC oscillator

2.6. Pin definitions

2.6.1. GD32G553QxTx LQFP128 pin definitions

Table 2-3. GD32G553QxTx LQFP128 pin definitions

GD32G553QxTx LQFP128				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PE2	1	I/O	5VT	Default: PE2 Alternate: TIMER2_CH0, TIMER19_CH0, HRTIMER_ST7CH0, EXMC_A23, EVENTOUT
PE3	2	I/O	5VT	Default: PE3 Alternate: TIMER2_CH1, TIMER19_CH1, HRTIMER_ST7CH1, EXMC_A19, EVENTOUT
PE4	3	I/O	5VT	Default: PE4 Alternate: TIMER0_BRKIN1, TIMER2_CH2, HPDF_DATAIN3, TIMER19_MCH0, EXMC_A20, EVENTOUT
PE5	4	I/O	5VT	Default: PE5 Alternate: TIMER2_CH3, HPDF_CKIN3, TIMER19_MCH1, EXMC_A21, EVENTOUT
PE6	5	I/O	5VT	Default: PE6 Alternate: TIMER19_MCH2, EXMC_A22, EVENTOUT Additional: WKUP2, RTC_TAMP2
VBAT	6	P	-	Default: VBAT
PC13	7	I/O	5VT	Default: PC13 Alternate: TIMER0_BRKIN0, TIMER0_MCH0, TIMER7_MCH3, EVENTOUT Additional: WKUP1, RTC_TAMP0, RTC_TS, RTC_OUT0
PC14-OSC32IN	8	I/O	5VT	Default: PC14 Alternate: EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	9	I/O	5VT	Default: PC15 Alternate: EVENTOUT Additional: OSC32OUT
PF3	10	I/O	5VT	Default: PF3 Alternate: TIMER19_CH3, I2C2_SCL, EXMC_A3, EVENTOUT
PF4	11	I/O	5VT	Default: PF4 Alternate: CMP0_OUT, TIMER19_MCH0, I2C2_SDA, HPDF_DATAIN2, EXMC_A4, TRIGSEL_OUT1, EVENTOUT
VSS	12	P	-	Default: VSS
VDD	13	P	-	Default: VDD
PF5	14	I/O	5VT	Default: PF5

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: TIMER19_MCH1, HPDF_CKIN2, EXMC_A5, TRIGSEL_OUT5, EVENTOUT
PF7	15	I/O	5VT	Default: PF7 Alternate: TIMER19_BRKIN0, TIMER4_CH1, QSPI_IO2(6), EXMC_A1, EVENTOUT
PF8	16	I/O	5VT	Default: PF8 Alternate: TIMER19_BRKIN2, TIMER4_CH1, QSPI_IO0(6), EXMC_A24, EVENTOUT
PF9	17	I/O	5VT	Default: PF9 Alternate: TIMER19_BRKIN0, TIMER14_CH0, SPI1_SCK, TIMER4_CH3, QSPI_IO1(6), EXMC_A25, EVENTOUT
PF10	18	I/O	5VT	Default: PF10 Alternate: USART0_RTS, USART0_DE, TIMER19_BRKIN2, TIMER14_CH1, SPI1_SCK, QSPI_SCK(6), EXMC_A0, EVENTOUT
OSCIN-PF0	19	I/O	5VT	Default: OSCIN, PF0 Alternate: I2C1_SDA, SPI1_NSS, TIMER0_MCH2, EVENTOUT Additional: ADC0_IN9, OSCIN, CLAIN16
OSCOUT-PF1	20	I/O	5VT	Default: OSCOUT, PF1 Alternate: TIMER19_BRKIN1, SPI1_SCK, EVENTOUT Additional: ADC1_IN9, CMP2_IM, OSCOUT, CLAIN17
NRST-PG10	21	I/O	5VT	Default: NRST Alternate: CK_OUT, EVENTOUT Additional: PG10(7)
PC0	22	I/O	5VT	Default: PC0 Alternate: USART0_RX, LPTIMER_IN0, TIMER0_CH0, HPDF_CKIN0, HPDF_DATAIN4, TRIGSEL_IN8, EXMC_CLK, EVENTOUT Additional: ADC01_IN5, CMP2_IM
PC1	23	I/O		Default: PC1 Alternate: USART0_TX, LPTIMER_OUT, TIMER0_CH1, HPDF_CKIN4, HPDF_DATAIN0, QSPI_IO0(6), TRIGSEL_IN9, EXMC_NOE, EVENTOUT Additional: ADC01_IN6, CMP2_IP
PC2	24	I/O	5VT	Default: PC2 Alternate: HPDF_CKOUT, LPTIMER_IN1, TIMER0_CH2, CMP2_OUT, TIMER19_CH1, HPDF_CKIN1, QSPI_IO1(6), TRIGSEL_IN2, EXMC_NWE, EVENTOUT Additional: ADC01_IN7, CMP7_IP
PC3	25	I/O		Default: PC3 Alternate: LPTIMER_ETI0, TIMER0_CH3, TIMER0_BRKIN2, HPDF_DATAIN1, QSPI_IO2(6),

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				HRTIMER_FLT6, EXMC_NWAIT, EVENTOUT Additional: ADC01_IN8
PF2	26	I/O	5VT	Default: PF2 Alternate: TIMER19_CH2, I2C1_SMBA, EXMC_A2, EVENTOUT
PA0	27	I/O		Default: PA0 Alternate: TIMER1_CH0, TIMER4_CH0, UART3_TX, USART1_CTS, CMP0_OUT, TIMER7_BRKIN0, TIMER7_ETI, HRTIMER_ST6CH0, TRIGSEL_IN0, TIMER1_ETI, EXMC_A13, EVENTOUT Additional: ADC01_IN0, RTC_TAMP1, CMP0_IM, CMP2_IP, WKUP0, CLAIN18
PA1	28	I/O		Default: PA1 Alternate: RTC_REFIN, TIMER1_CH1, TIMER4_CH1, UART3_RX, USART1_RTS, USART1_DE, TIMER14_MCH0, HRTIMER_ST6CH1, TRIGSEL_IN1, EXMC_A14, EVENTOUT Additional: ADC01_IN1, CMP0_IP, CLAIN19
PA2	29	I/O	5VT	Default: PA2 Alternate: TIMER1_CH2, TIMER4_CH2, CLA0OUT, USART1_TX, CMP1_OUT, TIMER14_CH0, QSPI_CSN(3)(6), HRTIMER_ST7CH0, TRIGSEL_IN7, CK_HPDFAUDIO, EXMC_A15, EVENTOUT Additional: ADC0_IN2, CMP1_IM, WKUP3, LSCK_OUT
VSS	30	P	-	Default: VSS
VDD	31	P	-	Default: VDD
PA3	32	I/O		Default: PA3 Alternate: TIMER1_CH3, TIMER4_CH3, USART1_RX, TIMER14_CH1, QSPI_SCK(3), HRTIMER_ST7CH1, TRIGSEL_IN4, EXMC_A16, EVENTOUT Additional: ADC0_IN3, CMP1_IP
PA4	33	I/O		Default: PA4 Alternate: TIMER2_CH1, SPI0_NSS, SPI2_NSS, USART1_CK, HRTIMER_ST2CH0, EXMC_A17, EVENTOUT Additional: ADC1_IN15, DAC0_OUT0, CMP0_IM
PA5	34	I/O		Default: PA5 Alternate: TIMER1_CH0, TIMER1_ETI, SPI0_SCK, USART2_TX, HRTIMER_ST2CH1, EXMC_A18, EVENTOUT Additional: ADC1_IN12, DAC0_OUT1, CMP1_IM
PA6	35	I/O		Default: PA6 Alternate: TIMER15_CH0, TIMER2_CH0, TIMER7_BRKIN0, SPI0_MISO, USART2_RX, TIMER0_BRKIN0, CMP0_OUT, QSPI_IO3(3),

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				HRTIMER_ST3CH0, CK_HPDFAUDIO, EXMC_A19, EVENTOUT Additional: ADC1_IN2, DAC1_OUT0
PA7	36	I/O		Default: PA7 Alternate: TIMER16_CH0, TIMER2_CH1, CLA1OUT, TIMER7_MCH0, SPI0_MOSI, TIMER0_MCH0, CMP1_OUT, QSPI_IO2(3), HRTIMER_ST3CH1, TRIGSEL_IN5, UART4_TX, EXMC_A20, EVENTOUT Additional: ADC1_IN3, CMP1_IP, DAC1_OUT1
PC4	37	I/O	5VT	Default: PC4 Alternate: TIMER0_ETI, I2C1_SCL, USART0_TX, HPDF_CKIN2, QSPI_IO3(3), HRTIMER_FLT7, EXMC_NE0, EVENTOUT Additional: ADC1_IN4
PC5	38	I/O		Default: PC5 Alternate: TIMER14_BRKIN0, TIMER0_MCH3, USART0_RX, HPDF_DATAIN2, HRTIMER_EXEV9, EXMC_NE1, EVENTOUT Additional: ADC1_IN10, WKUP4
PB0	39	I/O		Default: PB0 Alternate: TIMER2_CH2, CLA1OUT, TIMER7_MCH1, HPDF_CKOUT, TIMER0_MCH1, HRTIMER_ST4CH0, QSPI_IO1(3), TRIGSEL_OUT3, HRTIMER_FLT4, EXMC_A1, EVENTOUT Additional: ADC2_IN11, ADC0_IN12, CMP3_IP, CLAIN8
PB1	40	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER7_MCH2, HPDF_DATAIN1, TIMER0_MCH2, TIMER19_MCH0, CMP3_OUT, HRTIMER_ST4CH1, QSPI_IO0(3), TRIGSEL_OUT4, HRTIMER_SCOUT, EXMC_A2, EVENTOUT Additional: ADC2_IN0, ADC0_IN11, CMP0_IP, CLAIN9
PB2	41	I/O		Default: PB2 Alternate: RTC_OUT1, LPTIMER_OUT, TIMER4_CH0, TIMER19_CH0, I2C2_SMBA, HPDF_CKIN1, HRTIMER_ST5CH0, QSPI_IO1(3), HRTIMER_SCIN, EXMC_A3, EVENTOUT Additional: ADC1_IN11, CMP3_IM, CLAIN10
VSSA	42	P	-	Default: VSSA
VREFP	43	P	-	Default: VREFP
VREFP	44	P	-	Default: VREFP
VDDA	45	P	-	Default: VDDA
VSS	46	P	-	Default: VSS
VDD	47	P	-	Default: VDD

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PF11	48	I/O	5VT	Default: PF11 Alternate: TIMER19_ETI, EXMC_NE3, EVENTOUT
PF12	49	I/O	5VT	Default: PF12 Alternate: TIMER19_CH0, EXMC_A6, EVENTOUT
PF13	50	I/O	5VT	Default: PF13 Alternate: TIMER19_CH1, HPDF_DATAIN6, I2C3_SMBA, EXMC_A7, EVENTOUT
PF14	51	I/O	5VT	Default: PF14 Alternate: TIMER19_CH2, HPDF_CKIN6, I2C3_SCL, EXMC_A8, EVENTOUT
PF15	52	I/O	5VT	Default: PF15 Alternate: TIMER19_CH3, I2C3_SDA, EXMC_A9, EVENTOUT
PE7	53	I/O		Default: PE7 Alternate: TIMER0_ETI, HPDF_DATAIN2, EXMC_D4, EVENTOUT Additional: ADC2_IN3, CMP3_IP
PE8	54	I/O	5VT	Default: PE8 Alternate: TIMER4_CH2, TIMER0_MCH0, HPDF_CKIN2, EXMC_D5, EVENTOUT Additional: ADC23_IN5, CMP3_IM
PE9	55	I/O	5VT	Default: PE9 Alternate: TIMER4_CH3, TIMER0_CH0, HPDF_CKOUT, SPI0_IO2, EXMC_D6, EVENTOUT Additional: ADC2_IN1, CMP7_IP
PE10	56	I/O	5VT	Default: PE10 Alternate: TIMER0_MCH1, HPDF_DATAIN4, SPI0_IO3, QSPI_SCK(4), EXMC_D7, EVENTOUT Additional: ADC2_IN12, ADC3_IN13
PE11	57	I/O	5VT	Default: PE11 Alternate: TIMER0_CH1, HPDF_CKIN4, QSPI_CSN(4), EXMC_D8, EVENTOUT Additional: ADC2_IN13, ADC3_IN14
PE12	58	I/O	5VT	Default: PE12 Alternate: TIMER0_MCH2, HPDF_DATAIN5, QSPI_IO0(4), EXMC_D9, EVENTOUT Additional: ADC2_IN14, ADC3_IN15
PE13	59	I/O	5VT	Default: PE13 Alternate: TIMER0_CH2, HPDF_CKIN5, QSPI_IO1(4), EXMC_D10, EVENTOUT Additional: ADC2_IN2
PE14	60	I/O	5VT	Default: PE14 Alternate: TIMER0_CH3, TIMER0_BRKIN2, QSPI_IO2(4), EXMC_D11, EVENTOUT Additional: ADC3_IN0

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PE15	61	I/O	5VT	Default: PE15 Alternate: TIMER0_BRKIN0, TIMER0_MCH3, USART2_RX, QSPI_IO3(4), EXMC_D12, EVENTOUT Additional: ADC3_IN1
PB10	62	I/O		Default: PB10 Alternate: TIMER1_CH2, HPDF_DATAIN0, HPDF_DATAIN7, USART2_TX, QSPI_SCK(4), TIMER0_BRKIN0, HRTIMER_FLT2, TRIGSEL_OUT2, EXMC_A7, EVENTOUT Additional: CMP4_IM
VSS	63	P	-	Default: VSS
VDD	64	P	-	Default: VDD
PB11	65	I/O		Default: PB11 Alternate: TIMER1_CH3, HPDF_DATAIN3, HPDF_CKIN7, USART2_RX, QSPI_CSN(4), HRTIMER_FLT3, EXMC_A8, EVENTOUT Additional: ADC01_IN13, CMP5_IP
PB12	66	I/O		Default: PB12 Alternate: TIMER4_ETI, I2C1_SMBA, SPI1_NSS, TIMER0_BRKIN0, USART2_CK, CAN1_RX, HPDF_DATAIN1, HRTIMER_ST2CH0, EXMC_A9, EVENTOUT Additional: ADC3_IN2, ADC0_IN10, CMP6_IM
PB13	67	I/O		Default: PB13 Alternate: SPI1_SCK, TIMER0_MCH0, USART2_CTS, CAN1_TX, HPDF_CKIN1, HRTIMER_ST2CH1, EXMC_A10, EVENTOUT Additional: ADC2_IN4, CMP4_IP
PB14	68	I/O		Default: PB14 Alternate: TIMER14_CH0, SPI1_MISO, TIMER0_MCH1, USART2_RTS, USART2_DE, CMP3_OUT, HPDF_DATAIN2, HRTIMER_ST3CH0, TRIGSEL_OUT1, EXMC_A11, EVENTOUT Additional: ADC3_IN3, ADC0_IN4, CMP6_IP
PB15	69	I/O		Default: PB15 Alternate: RTC_REFIN, TIMER14_CH1, TIMER14_MCH0, CMP2_OUT, TIMER0_MCH2, SPI1_MOSI, HPDF_CKIN2, HRTIMER_ST3CH1, TRIGSEL_OUT5, EXMC_A12, EVENTOUT Additional: ADC3_IN4, ADC1_IN14, CMP5_IM
PD8	70	I/O		Default: PD8 Alternate: HPDF_CKIN3, USART2_TX, EXMC_D13, EVENTOUT Additional: ADC3_IN11, CMP7_IM
PD9	71	I/O		Default: PD9

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: HPDF_DATAIN3, USART2_RX, EXMC_D14, EVENTOUT Additional: ADC3_IN12, CMP7_IM
PD10	72	I/O	5VT	Default: PD10 Alternate: HPDF_CKOUT, USART2_CK, EXMC_D15, EVENTOUT Additional: ADC23_IN6, CMP5_IM
PD11	73	I/O		Default: PD11 Alternate: TIMER4_ETI, I2C3_SMBA, USART2_CTS, EXMC_A16, EVENTOUT Additional: ADC23_IN7, CMP5_IP
PD12	74	I/O		Default: PD12 Alternate: TIMER3_CH0, USART2_RTS, USART2_DE, EXMC_A17, EVENTOUT Additional: ADC23_IN8, CMP4_IP
PD13	75	I/O	5VT	Default: PD13 Alternate: TIMER3_CH1, EXMC_A18, EVENTOUT Additional: ADC23_IN9, CMP4_IM
PD14	76	I/O		Default: PD14 Alternate: TIMER3_CH2, SPI0_IO2, EXMC_D0, EVENTOUT Additional: ADC23_IN10, CMP6_IP
PD15	77	I/O	5VT	Default: PD15 Alternate: TIMER3_CH3, SPI0_IO3, SPI1_NSS, EXMC_D1, EVENTOUT Additional: CMP6_IM
VSS	78	P	-	Default: VSS
VDD	79	P	-	Default: VDD
PC6	80	I/O	5VT	Default: PC6 Alternate: HPDF_CKIN3, TIMER0_BRKIN1, CMP5_OUT, TIMER2_CH0, HRTIMER_EXEV9, TIMER7_CH0, I2C3_SCL, HRTIMER_ST5CH0, EXMC_NE2, EVENTOUT
PC7	81	I/O	5VT	Default: PC7 Alternate: HPDF_DATAIN3, TIMER2_CH1, HRTIMER_FLT4, TIMER7_CH1, CMP4_OUT, I2C3_SDA, HRTIMER_ ST5CH1, EXMC_NE3, EVENTOUT
PG0	82	I/O	5VT	Default: PG0 Alternate: TIMER19_MCH0, EXMC_A10, EVENTOUT
PG1	83	I/O	5VT	Default: PG1 Alternate: TIMER19_MCH1, EXMC_A11, EVENTOUT
PG2	84	I/O	5VT	Default: PG2 Alternate: TIMER0_BRKIN1, TIMER19_MCH2, SPI0_SCK, EXMC_A12, EVENTOUT

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PG3	85	I/O	5VT	Default: PG3 Alternate: TIMER19_BRKIN0, I2C3_SCL, SPI0_MISO, TIMER19_MCH3, EXMC_A13, EVENTOUT
PG4	86	I/O	5VT	Default: PG4 Alternate: TIMER7_BRKIN1, TIMER19_BRKIN2, I2C3_SDA, SPI0_MOSI, EXMC_A14, EVENTOUT
PC8	87	I/O	5VT	Default: PC8 Alternate: TIMER2_CH2, HRTIMER_ST4CH0, TIMER7_CH2, TIMER19_CH2, CMP6_OUT, I2C2_SCL, EXMC_NBL0, EVENTOUT
PC9	88	I/O	5VT	Default: PC9 Alternate: TIMER2_CH3, HRTIMER_ST4CH1, TIMER7_CH3, TIMER7_BRKIN2, I2C2_SDA, EXMC_NBL1, EVENTOUT
PA8	89	I/O	5VT	Default: PA8 Alternate: CK_OUT, I2C2_SCL, I2C1_SDA, TIMER0_CH0, USART0_CK, CMP6_OUT, TIMER3_ETI, CAN2_RX, SPI1_NSS, HRTIMER_ST0CH0, UART4_RX, EXMC_A21, EVENTOUT Additional: ADC3_IN16, NMI, CLAIN11
PA9	90	I/O	5VT	Default: PA9 Alternate: I2C2_SMBA, I2C1_SCL, TIMER0_CH1, USART0_TX, CMP4_OUT, TIMER14_BRKIN0, TIMER1_CH2, SPI1_SCK, HRTIMER_ST0CH1, TRIGSEL_IN13, EXMC_A22, EVENTOUT Additional: ADC3_IN17, CLAIN12
PA10	91	I/O	5VT	Default: PA10 Alternate: TIMER16_BRKIN0, CLA2OUT, I2C1_SMBA, SPI1_MISO, TIMER0_CH2, USART0_RX, CMP5_OUT, TIMER1_CH3, TIMER7_BRKIN0, HRTIMER_ST1CH0, TRIGSEL_IN12, EXMC_A23, EVENTOUT Additional: CLAIN13, LVD_IN
PA11	92	I/O	5VT	Default: PA11 Alternate: CLA3OUT, SPI1_MOSI, TIMER0_MCH0, USART0_CTS, CMP0_OUT, CAN0_RX, TIMER3_CH0, TIMER0_CH3, TIMER0_BRKIN2, HRTIMER_ST1CH1, TRIGSEL_IN13, EXMC_A24, EVENTOUT Additional: CLAIN14
PA12	93	I/O	5VT	Default: PA12 Alternate: TIMER15_CH0, TIMER0_MCH1, USART0_RTS, USART0_DE, CMP1_OUT, CAN0_TX, TIMER3_CH1, TIMER0_ETI, HRTIMER_FLT0, TRIGSEL_IN12, EXMC_A25, EVENTOUT Additional: CLAIN15

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
VSS	94	P	-	Default: VSS
VDD	95	P	-	Default: VDD
PA13	96	I/O	5VT	Default: JTMS, SWDIO, PA13 Alternate: TIMER15_MCH0, TIMER0_BRKIN1, I2C3_SCL, I2C0_SCL, IFRP_OUT, TIMER7_BRKIN1, USART2_CTS, CMP7_OUT, TIMER3_CH2, TRIGSEL_IN10, EXMC_A5, EVENTOUT
PF6	97	I/O	5VT	Default: PF6 Alternate: TIMER4_ETI, TIMER3_CH3, I2C1_SCL, TIMER4_CH0, USART2_RTS, USART2_DE, QSPI_IO3(6), EVENTOUT
PA14	98	I/O	5VT	Default: JTCK, SWCLK, PA14 Alternate: LPTIMER_OUT, I2C3_SMBA, I2C0_SDA, TIMER7_CH1, TIMER0_BRKIN0, USART1_TX, CMP7_OUT, TRIGSEL_IN11, EVENTOUT
PA15	99	I/O	5VT	Default: JTDI, PA15 Alternate: TIMER1_CH0, TIMER7_CH0, CLA3OUT, I2C0_SCL, SPI0_NSS, SPI2_NSS, USART1_RX, UART3_RTS, UART3_DE, TIMER0_BRKIN0, CAN2_TX, TRIGSEL_OUT0, HRTIMER_FLT1, TIMER1_ETI, EVENTOUT Additional: CLAIN0
PC10	100	I/O	5VT	Default: PC10 Alternate: HPDF_CKIN5, TIMER7_MCH0, UART3_TX, SPI2_SCK, USART2_TX, HRTIMER_FLT5, EXMC_D0, EVENTOUT
PC11	101	I/O	5VT	Default: PC11 Alternate: HPDF_DATAIN5, HRTIMER_EXEV1, TIMER7_MCH1, UART3_RX, SPI2_MISO, USART2_RX, I2C2_SDA, EXMC_D1,EVENTOUT
PC12	102	I/O	5VT	Default: PC12 Alternate: TIMER4_CH1, HRTIMER_EXEV0, TIMER7_MCH2, UART4_TX, SPI2_MOSI, USART2_CK, EXMC_A0, EVENTOUT
PG5	103	I/O	5VT	Default: PG5 Alternate: TIMER19_ETI, SPI0_NSS, EXMC_A15, EVENTOUT
PG6	104	I/O	5VT	Default: PG6 Alternate: TIMER19_BRKIN0, I2C2_SMBA, EVENTOUT
PG7	105	I/O	5VT	Default: PG7 Alternate: TIMER19_BRKIN1, I2C2_SCL, EVENTOUT
PG8	106	I/O	5VT	Default: PG8 Alternate: I2C2_SDA, EXMC_NE2, EVENTOUT
PG9	107	I/O	5VT	Default: PG9

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: TIMER7_BRKIN1, SPI2_SCK, USART0_TX, EXMC_NE1, TIMER14_MCH0, EVENTOUT
PD0	108	I/O	5VT	Default: PD0 Alternate: HPDF_CKIN6, TIMER7_MCH3, CAN0_RX, EXMC_D2, TRIGSEL_IN3, EVENTOUT
PD1	109	I/O	5VT	Default: PD1 Alternate: HPDF_DATAIN6, TIMER7_CH3, TIMER7_BRKIN2, CAN0_TX, EXMC_D3, TRIGSEL_IN6, QSPI_DQS(5), EVENTOUT
VSS	110	P	-	Default: VSS
VDD	111	P	-	Default: VDD
PD2	112	I/O	5VT	Default: PD2 Alternate: TIMER2_ETI, TIMER7_BRKIN0, UART4_RX, QSPI_SCK(5), EVENTOUT
PD3	113	I/O	5VT	Default: PD3 Alternate: TIMER1_CH0, TIMER1_ETI, HPDF_CKOUT, USART1_CTS, QSPI_CSN(5), EXMC_CLK, EVENTOUT
PD4	114	I/O	5VT	Default: PD4 Alternate: TIMER1_CH1, USART1_RTS, USART1_DE, QSPI_IO0(5), EXMC_NOE, EVENTOUT
PD5	115	I/O	5VT	Default: PD5 Alternate: USART1_TX, QSPI_IO1, EXMC_NWE, EVENTOUT
PD6	116	I/O	5VT	Default: PD6 Alternate: TIMER1_CH3, HPDF_CKIN4, HPDF_DATAIN1, USART1_RX, QSPI_IO2(5), EXMC_NWAIT, EVENTOUT
PD7	117	I/O	5VT	Default: PD7 Alternate: TIMER1_CH2, HPDF_DATAIN4, HPDF_CKIN1, USART1_CK, QSPI_IO3(5), EXMC_NE0, EVENTOUT
PB3	118	I/O	5VT	Default: JTDO, PB3 Alternate: TIMER1_CH1, TIMER3_ETI, CLA0OUT, TIMER7_MCH0, SPI0_SCK, SPI2_SCK, USART1_TX, HRTIMER_ST5CH1, TIMER2_ETI, CAN2_RX, HRTIMER_SCOUT, HRTIMER_EXEV8, TRIGSEL_OUT7, EVENTOUT Additional: CLAIN1
PB4	119	I/O	5VT	Default: NJTRST, PB4 Alternate: TIMER15_CH0, TIMER2_CH0, CLA1OUT, TIMER7_MCH1, SPI0_MISO, SPI2_MISO, USART1_RX, UART4_RTS, UART4_DE, TIMER16_BRKIN0, CAN2_TX, HRTIMER_EXEV6, TRIGSEL_OUT6, EVENTOUT Additional: CLAIN2

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PB5	120	I/O	5VT	Default: PB5 Alternate: HPDF_CKIN0, TIMER15_BRKIN0, TIMER2_CH1, TIMER7_MCH2, I2C0_SMBA, SPI0_MOSI, SPI2_MOSI, USART1_CK, I2C2_SDA, CAN1_RX, TIMER16_CH0, LPTIMER_IN0, CLA2OUT, HRTIMER_EXEV5, UART4_CTS, EVENTOUT Additional: CLAIN3
PB6	121	I/O	5VT	Default: PB6 Alternate: HPDF_DATAIN5, TIMER15_MCH0, TIMER3_CH0, I2C0_SCL, TIMER7_CH0, TIMER7_ETI, USART0_TX, CMP3_OUT, CAN1_TX, TIMER7_BRKIN2, LPTIMER_ETI0, HRTIMER_SCIN, HRTIMER_EXEV3, EXMC_A4, EVENTOUT Additional: CLAIN4
PB7	122	I/O	5VT	Default: PB7 Alternate: HPDF_CKIN5, TIMER16_MCH0, TIMER3_CH1, I2C3_SDA, I2C0_SDA, TIMER7_BRKIN0, USART0_RX, CMP2_OUT, TIMER2_CH3, LPTIMER_IN1, EXMC_NL/EXMC_NADV, HRTIMER_EXEV2, UART3_CTS, QSPI_DQS(3)(4)(6), HRTIMER_ST5CH1, EVENTOUT Additional: CLAIN5
PB8/BOOT0	123	I/O	5VT	Default: BOOT0, PB8 Alternate: TIMER15_CH0, TIMER3_CH2, HPDF_CKIN7, I2C0_SCL, CLA3OUT, USART2_RX, CMP0_OUT, CAN0_RX, TIMER7_CH1, TIMER0_BRKIN0, HRTIMER_EXEV7, EVENTOUT Additional: CLAIN6
PB9	124	I/O	5VT	Default: PB9 Alternate: TIMER16_CH0, TIMER3_CH3, HPDF_DATAIN7, I2C0_SDA, IFRP_OUT, USART2_TX, CMP1_OUT, CAN0_TX, TIMER7_CH2, TIMER0_MCH2, HRTIMER_EXEV4, EXMC_A6, EVENTOUT Additional: CLAIN7
PE0	125	I/O	5VT	Default: PE0 Alternate: TIMER3_ETI, TIMER19_MCH3, TIMER15_CH0, TIMER19_ETI, USART0_TX, HRTIMER_ST6CH0, EXMC_NBL0, EVENTOUT
PE1	126	I/O	5VT	Default: PE1 Alternate: TIMER16_CH0, TIMER19_CH3, USART0_RX, HRTIMER_ST6CH1, EXMC_NBL1, EVENTOUT
VSS	127	P	-	Default: VSS

GD32G553QxTx LQFP128				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
VDD	128	P	-	Default: VDD

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) These QSPI pin functions are highly recommended to be used together, and the supported maximum communication clock is 120MHz for this group. Otherwise the QSPI maximum clock frequency cannot be guaranteed.

(4) These QSPI pin functions are highly recommended to be used together, and the supported maximum communication clock is 120MHz for this group. Otherwise the QSPI maximum clock frequency cannot be guaranteed.

(5) These QSPI pin functions are highly recommended to be used together, and the supported maximum communication clock is 200MHz for this group. Otherwise the QSPI maximum clock frequency cannot be guaranteed.

(6) These QSPI pin functions are highly recommended to be used together, and the supported maximum communication clock is 120MHz for this group. Otherwise the QSPI maximum clock frequency cannot be guaranteed.

(7) Refer to the description of the NRST_MDSEL bit field of OB_USER option byte in the GD32G5x3 User Manual to configure the NRST-PG10 pin as a PG10 general GPIO function.

2.6.2. GD32G553VxTx LQFP100 pin definitions

Table 2-4. GD32G553VxTx LQFP100 pin definitions

GD32G553VxTx LQFP100				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PE2	1	I/O	5VT	Default: PE2 Alternate: TIMER2_CH0, TIMER19_CH0, HRTIMER_ST7CH0, EXMC_A23, EVENTOUT
PE3	2	I/O	5VT	Default: PE3 Alternate: TIMER2_CH1, TIMER19_CH1, HRTIMER_ST7CH1, EXMC_A19, EVENTOUT
PE4	3	I/O	5VT	Default: PE4 Alternate: TIMER0_BRKIN1, TIMER2_CH2, HPDF_DATAIN3, TIMER19_MCH0, EXMC_A20, EVENTOUT
PE5	4	I/O	5VT	Default: PE5 Alternate: TIMER2_CH3, HPDF_CKIN3, TIMER19_MCH1, EXMC_A21, EVENTOUT
PE6	5	I/O	5VT	Default: PE6 Alternate: TIMER19_MCH2, EXMC_A22, EVENTOUT Additional: WKUP2, RTC_TAMP2
VBAT	6	P	-	Default: VBAT
PC13	7	I/O	5VT	Default: PC13 Alternate: TIMER0_BRKIN0, TIMER0_MCH0, TIMER7_MCH3, EVENTOUT Additional: WKUP1, RTC_TAMP0, RTC_TS, RTC_OUT0
PC14-OSC32IN	8	I/O	5VT	Default: PC14 Alternate: EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	9	I/O	5VT	Default: PC15 Alternate: EVENTOUT Additional: OSC32OUT
PF9	10	I/O	5VT	Default: PF9 Alternate: TIMER19_BRKIN0, TIMER14_CH0, SPI1_SCK, TIMER4_CH3, QSPI_IO1(6), EXMC_A25, EVENTOUT
PF10	11	I/O	5VT	Default: PF10 Alternate: USART0_RTS, USART0_DE, TIMER19_BRKIN2, TIMER14_CH1, SPI1_SCK, QSPI_SCK(6), EXMC_A0, EVENTOUT
OSCIN-PF0	12	I/O	5VT	Default: OSCIN, PF0 Alternate: I2C1_SDA, SPI1_NSS, TIMER0_MCH2, EVENTOUT Additional: ADC0_IN9, OSCIN, CLAIN16
OSCOUT-PF1	13	I/O	5VT	Default: OSCOUT, PF1 Alternate: TIMER19_BRKIN1, SPI1_SCK, EVENTOUT

GD32G553VxTx LQFP100				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Additional: ADC1_IN9, CMP2_IM, OSCOUT, CLAIN17
NRST-PG10	14	I/O	5VT	Default: NRST Alternate: CK_OUT, EVENTOUT Additional: PG10(7)
PC0	15	I/O	5VT	Default: PC0 Alternate: USART0_RX, LPTIMER_IN0, TIMER0_CH0, HPDF_CKIN0, HPDF_DATAIN4, TRIGSEL_IN8, EXMC_CLK, EVENTOUT Additional: ADC01_IN5, CMP2_IM
PC1	16	I/O		Default: PC1 Alternate: USART0_TX, LPTIMER_OUT, TIMER0_CH1, HPDF_CKIN4, HPDF_DATAIN0, QSPI_IO0(6), TRIGSEL_IN9, EXMC_NOE, EVENTOUT Additional: ADC01_IN6, CMP2_IP
PC2	17	I/O	5VT	Default: PC2 Alternate: HPDF_CKOUT, LPTIMER_IN1, TIMER0_CH2, CMP2_OUT, TIMER19_CH1, HPDF_CKIN1, QSPI_IO1(6), TRIGSEL_IN2, EXMC_NWE, EVENTOUT Additional: ADC01_IN7, CMP7_IP
PC3	18	I/O		Default: PC3 Alternate: LPTIMER_ETI0, TIMER0_CH3, TIMER0_BRKIN2, HPDF_DATAIN1, QSPI_IO2(6), HRTIMER_FLT6, EXMC_NWAIT, EVENTOUT Additional: ADC01_IN8
PF2	19	I/O	5VT	Default: PF2 Alternate: TIMER19_CH2, I2C1_SMBA, EXMC_A2, EVENTOUT
PA0	20	I/O		Default: PA0 Alternate: TIMER1_CH0, TIMER4_CH0, UART3_TX, USART1_CTS, CMP0_OUT, TIMER7_BRKIN0, TIMER7_ETI, HRTIMER_ST6CH0, TRIGSEL_IN0, TIMER1_ETI, EXMC_A13, EVENTOUT Additional: ADC01_IN0, RTC_TAMP1, CMP0_IM, CMP2_IP, WKUP0, CLAIN18
PA1	21	I/O		Default: PA1 Alternate: RTC_REFIN, TIMER1_CH1, TIMER4_CH1, UART3_RX, USART1_RTS, USART1_DE, TIMER14_MCH0, HRTIMER_ST6CH1, TRIGSEL_IN1, EXMC_A14, EVENTOUT Additional: ADC01_IN1, CMP0_IP, CLAIN19
PA2	22	I/O	5VT	Default: PA2 Alternate: TIMER1_CH2, TIMER4_CH2, CLA0OUT, USART1_TX, CMP1_OUT, TIMER14_CH0, QSPI_CSN(3)(6), HRTIMER_ST7CH0, TRIGSEL_IN7, CK_HPDFAUDIO, EXMC_A15, EVENTOUT

GD32G553VxTx LQFP100				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Additional: ADC0_IN2, CMP1_IM, WKUP3, LSCK_OUT
VSS	23	P	-	Default: VSS
VDD	24	P	-	Default: VDD
PA3	25	I/O		Default: PA3 Alternate: TIMER1_CH3, TIMER4_CH3, USART1_RX, TIMER14_CH1, QSPI_SCK(3), HRTIMER_ST7CH1, TRIGSEL_IN4, EXMC_A16, EVENTOUT Additional: ADC0_IN3, CMP1_IP
PA4	26	I/O		Default: PA4 Alternate: TIMER2_CH1, SPI0_NSS, SPI2_NSS, USART1_CK, HRTIMER_ST2CH0, EXMC_A17, EVENTOUT Additional: ADC1_IN15, DAC0_OUT0, CMP0_IM
PA5	27	I/O		Default: PA5 Alternate: TIMER1_CH0, TIMER1_ETI, SPI0_SCK, USART2_TX, HRTIMER_ST2CH1, EXMC_A18, EVENTOUT Additional: ADC1_IN12, DAC0_OUT1, CMP1_IM
PA6	28	I/O		Default: PA6 Alternate: TIMER15_CH0, TIMER2_CH0, TIMER7_BRKIN0, SPI0_MISO, USART2_RX, TIMER0_BRKIN0, CMP0_OUT, QSPI_IO3(3), HRTIMER_ST3CH0, CK_HPDFAUDIO, EXMC_A19, EVENTOUT Additional: ADC1_IN2, DAC1_OUT0
PA7	29	I/O		Default: PA7 Alternate: TIMER16_CH0, TIMER2_CH1, CLA1OUT, TIMER7_MCH0, SPI0_MOSI, TIMER0_MCH0, CMP1_OUT, QSPI_IO2(3), HRTIMER_ST3CH1, TRIGSEL_IN5, UART4_TX, EXMC_A20, EVENTOUT Additional: ADC1_IN3, CMP1_IP, DAC1_OUT1
PC4	30	I/O	5VT	Default: PC4 Alternate: TIMER0_ETI, I2C1_SCL, USART0_TX, HPDF_CKIN2, QSPI_IO3(3), HRTIMER_FLT7, EXMC_NE0, EVENTOUT Additional: ADC1_IN4
PC5	31	I/O		Default: PC5 Alternate: TIMER14_BRKIN0, TIMER0_MCH3, USART0_RX, HPDF_DATAIN2, HRTIMER_EXEV9, EXMC_NE1, EVENTOUT Additional: ADC1_IN10, WKUP4
PB0	32	I/O		Default: PB0 Alternate: TIMER2_CH2, CLA1OUT, TIMER7_MCH1, HPDF_CKOUT, TIMER0_MCH1, HRTIMER_ST4CH0, QSPI_IO1(3), TRIGSEL_OUT3, HRTIMER_FLT4,

GD32G553VxTx LQFP100				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				EXMC_A1, EVENTOUT Additional: ADC2_IN11, ADC0_IN12, CMP3_IP, CLAIN8
PB1	33	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER7_MCH2, HPDF_DATAIN1, TIMER0_MCH2, TIMER19_MCH0, CMP3_OUT, HRTIMER_ST4CH1, QSPI_IO0(3), TRIGSEL_OUT4, HRTIMER_SCOUT, EXMC_A2, EVENTOUT Additional: ADC2_IN0, ADC0_IN11, CMP0_IP, CLAIN9
PB2	34	I/O		Default: PB2 Alternate: RTC_OUT1, LPTIMER_OUT, TIMER4_CH0, TIMER19_CH0, I2C2_SMBA, HPDF_CKIN1, HRTIMER_ST5CH0, QSPI_IO1(3), HRTIMER_SCIN, EXMC_A3, EVENTOUT Additional: ADC1_IN11, CMP3_IM, CLAIN10
VSSA	35	P	-	Default: VSSA
VREFP	36	P	-	Default: VREFP
VDDA	37	P	-	Default: VDDA
PE7	38	I/O		Default: PE7 Alternate: TIMER0_ETI, HPDF_DATAIN2, EXMC_D4, EVENTOUT Additional: ADC2_IN3, CMP3_IP
PE8	39	I/O	5VT	Default: PE8 Alternate: TIMER4_CH2, TIMER0_MCH0, HPDF_CKIN2, EXMC_D5, EVENTOUT Additional: ADC23_IN5, CMP3_IM
PE9	40	I/O	5VT	Default: PE9 Alternate: TIMER4_CH3, TIMER0_CH0, HPDF_CKOUT, SPI0_IO2, EXMC_D6, EVENTOUT Additional: ADC2_IN1, CMP7_IP
PE10	41	I/O	5VT	Default: PE10 Alternate: TIMER0_MCH1, HPDF_DATAIN4, SPI0_IO3, QSPI_SCK(4), EXMC_D7, EVENTOUT Additional: ADC2_IN12, ADC3_IN13
PE11	42	I/O	5VT	Default: PE11 Alternate: TIMER0_CH1, HPDF_CKIN4, QSPI_CSN(4), EXMC_D8, EVENTOUT Additional: ADC2_IN13, ADC3_IN14
PE12	43	I/O	5VT	Default: PE12 Alternate: TIMER0_MCH2, HPDF_DATAIN5, QSPI_IO0(4), EXMC_D9, EVENTOUT Additional: ADC2_IN14, ADC3_IN15
PE13	44	I/O	5VT	Default: PE13 Alternate: TIMER0_CH2, HPDF_CKIN5, QSPI_IO1(4),

GD32G553VxTx LQFP100				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				EXMC_D10, EVENTOUT Additional: ADC2_IN2
PE14	45	I/O	5VT	Default: PE14 Alternate: TIMER0_CH3, TIMER0_BRKIN2, QSPI_IO2(4), EXMC_D11, EVENTOUT Additional: ADC3_IN0
PE15	46	I/O	5VT	Default: PE15 Alternate: TIMER0_BRKIN0, TIMER0_MCH3, USART2_RX, QSPI_IO3(4), EXMC_D12, EVENTOUT Additional: ADC3_IN1
PB10	47	I/O		Default: PB10 Alternate: TIMER1_CH2, HPDF_DATAIN0, HPDF_DATAIN7, USART2_TX, QSPI_SCK(4), TIMER0_BRKIN0, HRTIMER_FLT2, TRIGSEL_OUT2, EXMC_A7, EVENTOUT Additional: CMP4_IM
VSS	48	P	-	Default: VSS
VDD	49	P	-	Default: VDD
PB11	50	I/O		Default: PB11 Alternate: TIMER1_CH3, HPDF_DATAIN3, HPDF_CKIN7, USART2_RX, QSPI_CSN(4), HRTIMER_FLT3, EXMC_A8, EVENTOUT Additional: ADC01_IN13, CMP5_IP
PB12	51	I/O		Default: PB12 Alternate: TIMER4_ETI, I2C1_SMBA, SPI1_NSS, TIMER0_BRKIN0, USART2_CK, CAN1_RX, HPDF_DATAIN1, HRTIMER_ST2CH0, EXMC_A9, EVENTOUT Additional: ADC3_IN2, ADC0_IN10, CMP6_IM
PB13	52	I/O		Default: PB13 Alternate: SPI1_SCK, TIMER0_MCH0, USART2_CTS, CAN1_TX, HPDF_CKIN1, HRTIMER_ST2CH1, EXMC_A10, EVENTOUT Additional: ADC2_IN4, CMP4_IP
PB14	53	I/O		Default: PB14 Alternate: TIMER14_CH0, SPI1_MISO, TIMER0_MCH1, USART2_RTS, USART2_DE, CMP3_OUT, HPDF_DATAIN2, HRTIMER_ST3CH0, TRIGSEL_OUT1, EXMC_A11, EVENTOUT Additional: ADC3_IN3, ADC0_IN4, CMP6_IP
PB15	54	I/O		Default: PB15 Alternate: RTC_REFIN, TIMER14_CH1, TIMER14_MCH0, CMP2_OUT, TIMER0_MCH2, SPI1_MOSI, HPDF_CKIN2, HRTIMER_ST3CH1, TRIGSEL_OUT5, EXMC_A12, EVENTOUT

GD32G553VxTx LQFP100				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Additional: ADC3_IN4, ADC1_IN14, CMP5_IM
PD8	55	I/O		Default: PD8 Alternate: HPDF_CKIN3, USART2_TX, EXMC_D13, EVENTOUT Additional: ADC3_IN11, CMP7_IM
PD9	56	I/O		Default: PD9 Alternate: HPDF_DATAIN3, USART2_RX, EXMC_D14, EVENTOUT Additional: ADC3_IN12, CMP7_IM
PD10	57	I/O	5VT	Default: PD10 Alternate: HPDF_CKOUT, USART2_CK, EXMC_D15, EVENTOUT Additional: ADC23_IN6, CMP5_IM
PD11	58	I/O		Default: PD11 Alternate: TIMER4_ETI, I2C3_SMBA, USART2_CTS, EXMC_A16, EVENTOUT Additional: ADC23_IN7, CMP5_IP
PD12	59	I/O		Default: PD12 Alternate: TIMER3_CH0, USART2_RTS, USART2_DE, EXMC_A17, EVENTOUT Additional: ADC23_IN8, CMP4_IP
PD13	60	I/O	5VT	Default: PD13 Alternate: TIMER3_CH1, EXMC_A18, EVENTOUT Additional: ADC23_IN9, CMP4_IM
PD14	61	I/O		Default: PD14 Alternate: TIMER3_CH2, SPI0_IO2, EXMC_D0, EVENTOUT Additional: ADC23_IN10, CMP6_IP
PD15	62	I/O	5VT	Default: PD15 Alternate: TIMER3_CH3, SPI0_IO3, SPI1_NSS, EXMC_D1, EVENTOUT Additional: CMP6_IM
VSS	63	P	-	Default: VSS
VDD	64	P	-	Default: VDD
PC6	65	I/O	5VT	Default: PC6 Alternate: HPDF_CKIN3, TIMER0_BRKIN1, CMP5_OUT, TIMER2_CH0, HRTIMER_EXEV9, TIMER7_CH0, I2C3_SCL, HRTIMER_ST5CH0, EXMC_NE2, EVENTOUT
PC7	66	I/O	5VT	Default: PC7 Alternate: HPDF_DATAIN3, TIMER2_CH1, HRTIMER_FLT4, TIMER7_CH1, CMP4_OUT, I2C3_SDA, HRTIMER_ ST5CH1, EXMC_NE3, EVENTOUT
PC8	67	I/O	5VT	Default: PC8

GD32G553VxTx LQFP100				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: TIMER2_CH2, HRTIMER_ST4CH0, TIMER7_CH2, TIMER19_CH2, CMP6_OUT, I2C2_SCL, EXMC_NBL0, EVENTOUT
PC9	68	I/O	5VT	Default: PC9 Alternate: TIMER2_CH3, HRTIMER_ST4CH1, TIMER7_CH3, TIMER7_BRKIN2, I2C2_SDA, EXMC_NBL1, EVENTOUT
PA8	69	I/O	5VT	Default: PA8 Alternate: CK_OUT, I2C2_SCL, I2C1_SDA, TIMER0_CH0, USART0_CK, CMP6_OUT, TIMER3_ETI, CAN2_RX, SPI1_NSS, HRTIMER_ST0CH0, UART4_RX, EXMC_A21, EVENTOUT Additional: ADC3_IN16, NMI, CLAIN11
PA9	70	I/O	5VT	Default: PA9 Alternate: I2C2_SMBA, I2C1_SCL, TIMER0_CH1, USART0_TX, CMP4_OUT, TIMER14_BRKIN0, TIMER1_CH2, SPI1_SCK, HRTIMER_ST0CH1, TRIGSEL_IN13, EXMC_A22, EVENTOUT Additional: ADC3_IN17, CLAIN12
PA10	71	I/O	5VT	Default: PA10 Alternate: TIMER16_BRKIN0, CLA2OUT, I2C1_SMBA, SPI1_MISO, TIMER0_CH2, USART0_RX, CMP5_OUT, TIMER1_CH3, TIMER7_BRKIN0, HRTIMER_ST1CH0, TRIGSEL_IN12, EXMC_A23, EVENTOUT Additional: CLAIN13, LVD_IN
PA11	72	I/O	5VT	Default: PA11 Alternate: CLA3OUT, SPI1_MOSI, TIMER0_MCH0, USART0_CTS, CMP0_OUT, CAN0_RX, TIMER3_CH0, TIMER0_CH3, TIMER0_BRKIN2, HRTIMER_ST1CH1, TRIGSEL_IN13, EXMC_A24, EVENTOUT Additional: CLAIN14
PA12	73	I/O	5VT	Default: PA12 Alternate: TIMER15_CH0, TIMER0_MCH1, USART0_RTS, USART0_DE, CMP1_OUT, CAN0_TX, TIMER3_CH1, TIMER0_ETI, HRTIMER_FLT0, TRIGSEL_IN12, EXMC_A25, EVENTOUT Additional: CLAIN15
VSS	74	P	-	Default: VSS
VDD	75	P	-	Default: VDD
PA13	76	I/O	5VT	Default: JTMS, SWDIO, PA13 Alternate: TIMER15_MCH0, TIMER0_BRKIN1, I2C3_SCL, I2C0_SCL, IFRP_OUT, TIMER7_BRKIN1, USART2_CTS, CMP7_OUT, TIMER3_CH2, TRIGSEL_IN10, EXMC_A5, EVENTOUT

GD32G553VxTx LQFP100				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PA14	77	I/O	5VT	Default: JTCK, SWCLK, PA14 Alternate: LPTIMER_OUT, I2C3_SMBA, I2C0_SDA, TIMER7_CH1, TIMER0_BRKIN0, USART1_TX, CMP7_OUT, TRIGSEL_IN11, EVENTOUT
PA15	78	I/O	5VT	Default: JTDI, PA15 Alternate: TIMER1_CH0, TIMER7_CH0, CLA3OUT, I2C0_SCL, SPI0_NSS, SPI2_NSS, USART1_RX, UART3_RTS, UART3_DE, TIMER0_BRKIN0, CAN2_TX, TRIGSEL_OUT0, HRTIMER_FLT1, TIMER1_ETI, EVENTOUT Additional: CLAIN0
PC10	79	I/O	5VT	Default: PC10 Alternate: HPDF_CKIN5, TIMER7_MCH0, UART3_TX, SPI2_SCK, USART2_TX, HRTIMER_FLT5, EXMC_D0, EVENTOUT
PC11	80	I/O	5VT	Default: PC11 Alternate: HPDF_DATAIN5, HRTIMER_EXEV1, TIMER7_MCH1, UART3_RX, SPI2_MISO, USART2_RX, I2C2_SDA, EXMC_D1,EVENTOUT
PC12	81	I/O	5VT	Default: PC12 Alternate: TIMER4_CH1, HRTIMER_EXEV0, TIMER7_MCH2, UART4_TX, SPI2_MOSI, USART2_CK, EXMC_A0, EVENTOUT
PD0	82	I/O	5VT	Default: PD0 Alternate: HPDF_CKIN6, TIMER7_MCH3, CAN0_RX, EXMC_D2, TRIGSEL_IN3, EVENTOUT
PD1	83	I/O	5VT	Default: PD1 Alternate: HPDF_DATAIN6, TIMER7_CH3, TIMER7_BRKIN2, CAN0_TX, EXMC_D3, TRIGSEL_IN6, QSPI_DQS(5), EVENTOUT
PD2	84	I/O	5VT	Default: PD2 Alternate: TIMER2_ETI, TIMER7_BRKIN0, UART4_RX, QSPI_SCK(5), EVENTOUT
PD3	85	I/O	5VT	Default: PD3 Alternate: TIMER1_CH0, TIMER1_ETI, HPDF_CKOUT, USART1_CTS, QSPI_CSN(5), EXMC_CLK, EVENTOUT
PD4	86	I/O	5VT	Default: PD4 Alternate: TIMER1_CH1, USART1_RTS, USART1_DE, QSPI_IO0(5), EXMC_NOE, EVENTOUT
PD5	87	I/O	5VT	Default: PD5 Alternate: USART1_TX, QSPI_IO1, EXMC_NWE, EVENTOUT
PD6	88	I/O	5VT	Default: PD6 Alternate: TIMER1_CH3, HPDF_CKIN4, HPDF_DATAIN1, USART1_RX, QSPI_IO2(5),

GD32G553VxTx LQFP100				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				EXMC_NWAIT, EVENTOUT
PD7	89	I/O	5VT	Default: PD7 Alternate: TIMER1_CH2, HPDF_DATAIN4, HPDF_CKIN1, USART1_CK, QSPI_IO3(5), EXMC_NE0, EVENTOUT
PB3	90	I/O	5VT	Default: JTDO, PB3 Alternate: TIMER1_CH1, TIMER3_ETI, CLA0OUT, TIMER7_MCH0, SPI0_SCK, SPI2_SCK, USART1_TX, HRTIMER_ST5CH1, TIMER2_ETI, CAN2_RX, HRTIMER_SCOUT, HRTIMER_EXEV8, TRIGSEL_OUT7, EVENTOUT Additional: CLAIN1
PB4	91	I/O	5VT	Default: NJTRST, PB4 Alternate: TIMER15_CH0, TIMER2_CH0, CLA1OUT, TIMER7_MCH1, SPI0_MISO, SPI2_MISO, USART1_RX, UART4_RTS, UART4_DE, TIMER16_BRKIN0, CAN2_TX, HRTIMER_EXEV6, TRIGSEL_OUT6, EVENTOUT Additional: CLAIN2
PB5	92	I/O	5VT	Default: PB5 Alternate: HPDF_CKIN0, TIMER15_BRKIN0, TIMER2_CH1, TIMER7_MCH2, I2C0_SMBA, SPI0_MOSI, SPI2_MOSI, USART1_CK, I2C2_SDA, CAN1_RX, TIMER16_CH0, LPTIMER_IN0, CLA2OUT, HRTIMER_EXEV5, UART4_CTS, EVENTOUT Additional: CLAIN3
PB6	93	I/O	5VT	Default: PB6 Alternate: HPDF_DATAIN5, TIMER15_MCH0, TIMER3_CH0, I2C0_SCL, TIMER7_CH0, TIMER7_ETI, USART0_TX, CMP3_OUT, CAN1_TX, TIMER7_BRKIN2, LPTIMER_ETI0, HRTIMER_SCIN, HRTIMER_EXEV3, EXMC_A4, EVENTOUT Additional: CLAIN4
PB7	94	I/O	5VT	Default: PB7 Alternate: HPDF_CKIN5, TIMER16_MCH0, TIMER3_CH1, I2C3_SDA, I2C0_SDA, TIMER7_BRKIN0, USART0_RX, CMP2_OUT, TIMER2_CH3, LPTIMER_IN1, EXMC_NL/EXMC_NADV, HRTIMER_EXEV2, UART3_CTS, QSPI_DQS(3)(4)(6), HRTIMER_ST5CH1, EVENTOUT Additional: CLAIN5
PB8/BOOT0	95	I/O	5VT	Default: BOOT0, PB8 Alternate: TIMER15_CH0, TIMER3_CH2, HPDF_CKIN7, I2C0_SCL, CLA3OUT, USART2_RX,

GD32G553VxTx LQFP100				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				CMP0_OUT, CAN0_RX, TIMER7_CH1, TIMER0_BRKIN0, HRTIMER_EXEV7, EVENTOUT Additional: CLAIN6
PB9	96	I/O	5VT	Default: PB9 Alternate: TIMER16_CH0, TIMER3_CH3, HPDF_DATAIN7, I2C0_SDA, IFRP_OUT, USART2_TX, CMP1_OUT, CAN0_TX, TIMER7_CH2, TIMER0_MCH2, HRTIMER_EXEV4, EXMC_A6, EVENTOUT Additional: CLAIN7
PE0	97	I/O	5VT	Default: PE0 Alternate: TIMER3_ETI, TIMER19_MCH3, TIMER15_CH0, TIMER19_ETI, USART0_TX, HRTIMER_ST6CH0, EXMC_NBL0, EVENTOUT
PE1	98	I/O	5VT	Default: PE1 Alternate: TIMER16_CH0, TIMER19_CH3, USART0_RX, HRTIMER_ST6CH1, EXMC_NBL1, EVENTOUT
VSS	99	P	-	Default: VSS
VDD	100	P	-	Default: VDD

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) These QSPI pin functions are highly recommended to be used together, and the supported maximum communication clock is 120MHz for this group. Otherwise the QSPI maximum clock frequency cannot be guaranteed.

(4) These QSPI pin functions are highly recommended to be used together, and the supported maximum communication clock is 120MHz for this group. Otherwise the QSPI maximum clock frequency cannot be guaranteed.

(5) These QSPI pin functions are highly recommended to be used together, and the supported maximum communication clock is 200MHz for this group. Otherwise the QSPI maximum clock frequency cannot be guaranteed.

(6) These QSPI pin functions are highly recommended to be used together, and the supported maximum communication clock is 120MHz for this group. Otherwise the QSPI maximum clock frequency cannot be guaranteed.

(7) Refer to the description of the NRST_MDSEL bit field of OB_USER option byte in the GD32G5x3 User Manual to configure the NRST-PG10 pin as a PG10 general GPIO function.

2.6.3. GD32G553MxY7TR WLCSP81 pin definitions

Table 2-5. GD32G553MxY7TR WLCSP81 pin definitions

GD32G553MxY7TR WLCSP81				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
VDD	A1	P	-	Default: VDD
VSS	B1	P	-	Default: VSS
PA12	C1	I/O	5VT	Default: PA12 Alternate: TIMER15_CH0, TIMER0_MCH1, USART0_RTS, USART0_DE, CMP1_OUT, CAN0_TX, TIMER3_CH1, TIMER0_ETI, HRTIMER_FLT0, TRIGSEL_IN12, EXMC_A25, EVENTOUT Additional: CLAIN15
PA8	D1	I/O	5VT	Default: PA8 Alternate: CK_OUT, I2C2_SCL, I2C1_SDA, TIMER0_CH0, USART0_CK, CMP6_OUT, TIMER3_ETI, CAN2_RX, SPI1_NSS, HRTIMER_ST0CH0, UART4_RX, EXMC_A21, EVENTOUT Additional: ADC3_IN16, NMI, CLAIN11
VDD	E1	P	-	Default: VDD
VSS	F1	P	-	Default: VSS
PD8	G1	I/O		Default: PD8 Alternate: HPDF_CKIN3, USART2_TX, EXMC_D13, EVENTOUT Additional: ADC3_IN11, CMP7_IM
PB13	H1	I/O		Default: PB13 Alternate: SPI1_SCK, TIMER0_MCH0, USART2_CTS, CAN1_TX, HPDF_CKIN1, HRTIMER_ST2CH1, EXMC_A10, EVENTOUT Additional: ADC2_IN4, CMP4_IP
VDD	J1	P	-	Default: VDD
PA15	A2	I/O	5VT	Default: JTDI, PA15 Alternate: TIMER1_CH0, TIMER7_CH0, CLA3OUT, I2C0_SCL, SPI0_NSS, SPI2_NSS, USART1_RX, UART3_RTS, UART3_DE, TIMER0_BRKIN0, CAN2_TX, TRIGSEL_OUT0, HRTIMER_FLT1, TIMER1_ETI, EVENTOUT Additional: CLAIN0
PA13	B2	I/O	5VT	Default: JTMS, SWDIO, PA13 Alternate: TIMER15_MCH0, TIMER0_BRKIN1, I2C3_SCL, I2C0_SCL, IFRP_OUT, TIMER7_BRKIN1, USART2_CTS, CMP7_OUT, TIMER3_CH2, TRIGSEL_IN10, EXMC_A5, EVENTOUT
PA11	C2	I/O	5VT	Default: PA11 Alternate: CLA3OUT, SPI1_MOSI, TIMER0_MCH0, USART0_CTS, CMP0_OUT, CAN0_RX, TIMER3_CH0,

GD32G553MxY7TR WLCSP81				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				TIMER0_CH3, TIMER0_BRKIN2, HRTIMER_ST1CH1, TRIGSEL_IN13, EXMC_A24, EVENTOUT Additional: CLAIN14
PC9	D2	I/O	5VT	Default: PC9 Alternate: TIMER2_CH3, HRTIMER_ST4CH1, TIMER7_CH3, TIMER7_BRKIN2, I2C2_SDA, EXMC_NBL1, EVENTOUT
PD11	E2	I/O		Default: PD11 Alternate: TIMER4_ETI, I2C3_SMBA, USART2_CTS, EXMC_A16, EVENTOUT Additional: ADC23_IN7, CMP5_IP
PD10	F2	I/O	5VT	Default: PD10 Alternate: HPDF_CKOUT, USART2_CK, EXMC_D15, EVENTOUT Additional: ADC23_IN6, CMP5_IM
PB14	G2	I/O		Default: PB14 Alternate: TIMER14_CH0, SPI1_MISO, TIMER0_MCH1, USART2_RTS, USART2_DE, CMP3_OUT, HPDF_DATAIN2, HRTIMER_ST3CH0, TRIGSEL_OUT1, EXMC_A11, EVENTOUT Additional: ADC3_IN3, ADC0_IN4, CMP6_IP
PB11	H2	I/O		Default: PB11 Alternate: TIMER1_CH3, HPDF_DATAIN3, HPDF_CKIN7, USART2_RX, QSPI_CSN(4), HRTIMER_FLT3, EXMC_A8, EVENTOUT Additional: ADC01_IN13, CMP5_IP
VSS	J2	P	-	Default: VSS
PC12	A3	I/O	5VT	Default: PC12 Alternate: TIMER4_CH1, HRTIMER_EXEV0, TIMER7_MCH2, UART4_TX, SPI2_MOSI, USART2_CK, EXMC_A0, EVENTOUT
PC10	B3	I/O	5VT	Default: PC10 Alternate: HPDF_CKIN5, TIMER7_MCH0, UART3_TX, SPI2_SCK, USART2_TX, HRTIMER_FLT5, EXMC_D0, EVENTOUT
PA14	C3	I/O	5VT	Default: JTCK, SWCLK, PA14 Alternate: LPTIMER_OUT, I2C3_SMBA, I2C0_SDA, TIMER7_CH1, TIMER0_BRKIN0, USART1_TX, CMP7_OUT, TRIGSEL_IN11, EVENTOUT
PA10	D3	I/O	5VT	Default: PA10 Alternate: TIMER16_BRKIN0, CLA2OUT, I2C1_SMBA, SPI1_MISO, TIMER0_CH2, USART0_RX, CMP5_OUT, TIMER1_CH3, TIMER7_BRKIN0, HRTIMER_ST1CH0, TRIGSEL_IN12, EXMC_A23, EVENTOUT Additional: CLAIN13, LVD_IN

GD32G553MxY7TR WLCSP81				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PC6	E3	I/O	5VT	Default: PC6 Alternate: HPDF_CKIN3, TIMER0_BRKIN1, CMP5_OUT, TIMER2_CH0, HRTIMER_EXEV9, TIMER7_CH0, I2C3_SCL, HRTIMER_ST5CH0, EXMC_NE2, EVENTOUT
PD9	F3	I/O		Default: PD9 Alternate: HPDF_DATAIN3, USART2_RX, EXMC_D14, EVENTOUT Additional: ADC3_IN12, CMP7_IM
PB12	G3	I/O		Default: PB12 Alternate: TIMER4_ETI, I2C1_SMBA, SPI1_NSS, TIMER0_BRKIN0, USART2_CK, CAN1_RX, HPDF_DATAIN1, HRTIMER_ST2CH0, EXMC_A9, EVENTOUT Additional: ADC3_IN2, ADC0_IN10, CMP6_IM
PB10	H3	I/O		Default: PB10 Alternate: TIMER1_CH2, HPDF_DATAIN0, HPDF_DATAIN7, USART2_TX, QSPI_SCK(4), TIMER0_BRKIN0, HRTIMER_FLT2, TRIGSEL_OUT2, EXMC_A7, EVENTOUT Additional: CMP4_IM
PE14	J3	I/O	5VT	Default: PE14 Alternate: TIMER0_CH3, TIMER0_BRKIN2, QSPI_IO2(4), EXMC_D11, EVENTOUT Additional: ADC3_IN0
PD1	A4	I/O	5VT	Default: PD1 Alternate: HPDF_DATAIN6, TIMER7_CH3, TIMER7_BRKIN2, CAN0_TX, EXMC_D3, TRIGSEL_IN6, QSPI_DQS(5), EVENTOUT
PD0	B4	I/O	5VT	Default: PD0 Alternate: HPDF_CKIN6, TIMER7_MCH3, CAN0_RX, EXMC_D2, TRIGSEL_IN3, EVENTOUT
PC11	C4	I/O	5VT	Default: PC11 Alternate: HPDF_DATAIN5, HRTIMER_EXEV1, TIMER7_MCH1, UART3_RX, SPI2_MISO, USART2_RX, I2C2_SDA, EXMC_D1,EVENTOUT
PA9	D4	I/O	5VT	Default: PA9 Alternate: I2C2_SMBA, I2C1_SCL, TIMER0_CH1, USART0_TX, CMP4_OUT, TIMER14_BRKIN0, TIMER1_CH2, SPI1_SCK, HRTIMER_ST0CH1, TRIGSEL_IN13, EXMC_A22, EVENTOUT Additional: ADC3_IN17, CLAIN12
PB15	E4	I/O		Default: PB15 Alternate: RTC_REFIN, TIMER14_CH1, TIMER14_MCH0, CMP2_OUT, TIMER0_MCH2, SPI1_MOSI, HPDF_CKIN2, HRTIMER_ST3CH1,

GD32G553MxY7TR WLCSP81				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				TRIGSEL_OUT5, EXMC_A12, EVENTOUT Additional: ADC3_IN4, ADC1_IN14, CMP5_IM
PE15	F4	I/O	5VT	Default: PE15 Alternate: TIMER0_BRKIN0, TIMER0_MCH3, USART2_RX, QSPI_IO3(4), EXMC_D12, EVENTOUT Additional: ADC3_IN1
PE13	G4	I/O	5VT	Default: PE13 Alternate: TIMER0_CH2, HPDF_CKIN5, QSPI_IO1(4), EXMC_D10, EVENTOUT Additional: ADC2_IN2
PE11	H4	I/O	5VT	Default: PE11 Alternate: TIMER0_CH1, HPDF_CKIN4, QSPI_CSN(4), EXMC_D8, EVENTOUT Additional: ADC2_IN13, ADC3_IN14
PE10	J4	I/O	5VT	Default: PE10 Alternate: TIMER0_MCH1, HPDF_DATAIN4, SPI0_IO3, QSPI_SCK(4), EXMC_D7, EVENTOUT Additional: ADC2_IN12, ADC3_IN13
PB3	A5	I/O	5VT	Default: JTDO, PB3 Alternate: TIMER1_CH1, TIMER3_ETI, CLA0OUT, TIMER7_MCH0, SPI0_SCK, SPI2_SCK, USART1_TX, HRTIMER_ST5CH1, TIMER2_ETI, CAN2_RX, HRTIMER_SCOUT, HRTIMER_EXEV8, TRIGSEL_OUT7, EVENTOUT Additional: CLAIN1
PD2	B5	I/O	5VT	Default: PD2 Alternate: TIMER2_ETI, TIMER7_BRKIN0, UART4_RX, QSPI_SCK(5), EVENTOUT
PC8	C5	I/O	5VT	Default: PC8 Alternate: TIMER2_CH2, HRTIMER_ST4CH0, TIMER7_CH2, TIMER19_CH2, CMP6_OUT, I2C2_SCL, EXMC_NBL0, EVENTOUT
PC7	D5	I/O	5VT	Default: PC7 Alternate: HPDF_DATAIN3, TIMER2_CH1, HRTIMER_FLT4, TIMER7_CH1, CMP4_OUT, I2C3_SDA, HRTIMER_ ST5CH1, EXMC_NE3, EVENTOUT
PE12	E5	I/O	5VT	Default: PE12 Alternate: TIMER0_MCH2, HPDF_DATAIN5, QSPI_IO0(4), EXMC_D9, EVENTOUT Additional: ADC2_IN14, ADC3_IN15
PE9	F5	I/O	5VT	Default: PE9 Alternate: TIMER4_CH3, TIMER0_CH0, HPDF_CKOUT, SPI0_IO2, EXMC_D6, EVENTOUT Additional: ADC2_IN1, CMP7_IP

GD32G553MxY7TR WLCSP81				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PE8	G5	I/O	5VT	Default: PE8 Alternate: TIMER4_CH2, TIMER0_MCH0, HPDF_CKIN2, EXMC_D5, EVENTOUT Additional: ADC23_IN5, CMP3_IM
PE7	H5	I/O		Default: PE7 Alternate: TIMER0_ETI, HPDF_DATAIN2, EXMC_D4, EVENTOUT Additional: ADC2_IN3, CMP3_IP
VDDA	J5	P	-	Default: VDDA
PB5	A6	I/O	5VT	Default: PB5 Alternate: HPDF_CKIN0, TIMER15_BRKIN0, TIMER2_CH1, TIMER7_MCH2, I2C0_SMBA, SPI0_MOSI, SPI2_MOSI, USART1_CK, I2C2_SDA, CAN1_RX, TIMER16_CH0, LPTIMER_IN0, CLA2OUT, HRTIMER_EXEV5, UART4_CTS, EVENTOUT Additional: CLAIN3
PB6	B6	I/O	5VT	Default: PB6 Alternate: HPDF_DATAIN5, TIMER15_MCH0, TIMER3_CH0, I2C0_SCL, TIMER7_CH0, TIMER7_ETI, USART0_TX, CMP3_OUT, CAN1_TX, TIMER7_BRKIN2, LPTIMER_ETI0, HRTIMER_SCIN, HRTIMER_EXEV3, EXMC_A4, EVENTOUT Additional: CLAIN4
PB4	C6	I/O	5VT	Default: NJTRST, PB4 Alternate: TIMER15_CH0, TIMER2_CH0, CLA1OUT, TIMER7_MCH1, SPI0_MISO, SPI2_MISO, USART1_RX, UART4_RTS, UART4_DE, TIMER16_BRKIN0, CAN2_TX, HRTIMER_EXEV6, TRIGSEL_OUT6, EVENTOUT Additional: CLAIN2
PA4	D6	I/O		Default: PA4 Alternate: TIMER2_CH1, SPI0_NSS, SPI2_NSS, USART1_CK, HRTIMER_ST2CH0, EXMC_A17, EVENTOUT Additional: ADC1_IN15, DAC0_OUT0, CMP0_IM
PC4	E6	I/O	5VT	Default: PC4 Alternate: TIMER0_ETI, I2C1_SCL, USART0_TX, HPDF_CKIN2, QSPI_IO3(3), HRTIMER_FLT7, EXMC_NE0, EVENTOUT Additional: ADC1_IN4
PB0	F6	I/O		Default: PB0 Alternate: TIMER2_CH2, CLA1OUT, TIMER7_MCH1, HPDF_CKOUT, TIMER0_MCH1, HRTIMER_ST4CH0, QSPI_IO1(3), TRIGSEL_OUT3, HRTIMER_FLT4, EXMC_A1, EVENTOUT Additional: ADC2_IN11, ADC0_IN12, CMP3_IP,

GD32G553MxY7TR WLCSP81				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				CLAIN8
PB1	G6	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER7_MCH2, HPDF_DATAIN1, TIMER0_MCH2, TIMER19_MCH0, CMP3_OUT, HRTIMER_ST4CH1, QSPI_IO0(3), TRIGSEL_OUT4, HRTIMER_SCOUT, EXMC_A2, EVENTOUT Additional: ADC2_IN0, ADC0_IN11, CMP0_IP, CLAIN9
VSSA	H6	P	-	Default: VSSA
VREFP	J6	P	-	Default: VREFP
PB9	A7	I/O	5VT	Default: PB9 Alternate: TIMER16_CH0, TIMER3_CH3, HPDF_DATAIN7, I2C0_SDA, IFRP_OUT, USART2_TX, CMP1_OUT, CAN0_TX, TIMER7_CH2, TIMER0_MCH2, HRTIMER_EXEV4, EXMC_A6, EVENTOUT Additional: CLAIN7
PB8/BOOT0	B7	I/O	5VT	Default: BOOT0, PB8 Alternate: TIMER15_CH0, TIMER3_CH2, HPDF_CKIN7, I2C0_SCL, CLA3OUT, USART2_RX, CMP0_OUT, CAN0_RX, TIMER7_CH1, TIMER0_BRKIN0, HRTIMER_EXEV7, EVENTOUT Additional: CLAIN6
PB7	C7	I/O	5VT	Default: PB7 Alternate: HPDF_CKIN5, TIMER16_MCH0, TIMER3_CH1, I2C3_SDA, I2C0_SDA, TIMER7_BRKIN0, USART0_RX, CMP2_OUT, TIMER2_CH3, LPTIMER_IN1, EXMC_NL/EXMC_NADV, HRTIMER_EXEV2, UART3_CTS, QSPI_DQS(3)(4)(6), HRTIMER_ST5CH1, EVENTOUT Additional: CLAIN5
PA0	D7	I/O		Default: PA0 Alternate: TIMER1_CH0, TIMER4_CH0, UART3_TX, USART1_CTS, CMP0_OUT, TIMER7_BRKIN0, TIMER7_ETI, HRTIMER_ST6CH0, TRIGSEL_IN0, TIMER1_ETI, EXMC_A13, EVENTOUT Additional: ADC01_IN0, RTC_TAMP1, CMP0_IM, CMP2_IP, WKUP0, CLAIN18
PA1	E7	I/O		Default: PA1 Alternate: RTC_REFIN, TIMER1_CH1, TIMER4_CH1, UART3_RX, USART1_RTS, USART1_DE, TIMER14_MCH0, HRTIMER_ST6CH1, TRIGSEL_IN1, EXMC_A14, EVENTOUT Additional: ADC01_IN1, CMP0_IP, CLAIN19

GD32G553MxY7TR WLCSP81				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PA5	F7	I/O		Default: PA5 Alternate: TIMER1_CH0, TIMER1_ETI, SPI0_SCK, USART2_TX, HRTIMER_ST2CH1, EXMC_A18, EVENTOUT Additional: ADC1_IN12, DAC0_OUT1, CMP1_IM
PA6	G7	I/O		Default: PA6 Alternate: TIMER15_CH0, TIMER2_CH0, TIMER7_BRKIN0, SPI0_MISO, USART2_RX, TIMER0_BRKIN0, CMP0_OUT, QSPI_IO3(3), HRTIMER_ST3CH0, CK_HPDFAUDIO, EXMC_A19, EVENTOUT Additional: ADC1_IN2, DAC1_OUT0
PC5	H7	I/O		Default: PC5 Alternate: TIMER14_BRKIN0, TIMER0_MCH3, USART0_RX, HPDF_DATAIN2, HRTIMER_EXEV9, EXMC_NE1, EVENTOUT Additional: ADC1_IN10, WKUP4
PB2	J7	I/O		Default: PB2 Alternate: RTC_OUT1, LPTIMER_OUT, TIMER4_CH0, TIMER19_CH0, I2C2_SMBA, HPDF_CKIN1, HRTIMER_ST5CH0, QSPI_IO1(3), HRTIMER_SCIN, EXMC_A3, EVENTOUT Additional: ADC1_IN11, CMP3_IM, CLAIN10
VSS	A8	P	-	Default: VSS
PC13	B8	I/O	5VT	Default: PC13 Alternate: TIMER0_BRKIN0, TIMER0_MCH0, TIMER7_MCH3, EVENTOUT Additional: WKUP1, RTC_TAMP0, RTC_TS, RTC_OUT0
PC1	C8	I/O		Default: PC1 Alternate: USART0_TX, LPTIMER_OUT, TIMER0_CH1, HPDF_CKIN4, HPDF_DATAIN0, QSPI_IO0(6), TRIGSEL_IN9, EXMC_NOE, EVENTOUT Additional: ADC01_IN6, CMP2_IP
NRST-PG10	D8	I/O	5VT	Default: NRST Alternate: CK_OUT, EVENTOUT Additional: PG10(7)
PC0	E8	I/O	5VT	Default: PC0 Alternate: USART0_RX, LPTIMER_IN0, TIMER0_CH0, HPDF_CKIN0, HPDF_DATAIN4, TRIGSEL_IN8, EXMC_CLK, EVENTOUT Additional: ADC01_IN5, CMP2_IM
PC2	F8	I/O	5VT	Default: PC2 Alternate: HPDF_CKOUT, LPTIMER_IN1, TIMER0_CH2, CMP2_OUT, TIMER19_CH1,

GD32G553MxY7TR WLCSP81				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				HPDF_CKIN1, QSPI_IO1(6), TRIGSEL_IN2, EXMC_NWE, EVENTOUT Additional: ADC01_IN7, CMP7_IP
PA2	G8	I/O	5VT	Default: PA2 Alternate: TIMER1_CH2, TIMER4_CH2, CLA0OUT, USART1_TX, CMP1_OUT, TIMER14_CH0, QSPI_CSN(3)(6), HRTIMER_ST7CH0, TRIGSEL_IN7, CK_HPDFAUDIO, EXMC_A15, EVENTOUT Additional: ADC0_IN2, CMP1_IM, WKUP3, LSCK_OUT
PA3	H8	I/O		Default: PA3 Alternate: TIMER1_CH3, TIMER4_CH3, USART1_RX, TIMER14_CH1, QSPI_SCK(3), HRTIMER_ST7CH1, TRIGSEL_IN4, EXMC_A16, EVENTOUT Additional: ADC0_IN3, CMP1_IP
PA7	J8	I/O		Default: PA7 Alternate: TIMER16_CH0, TIMER2_CH1, CLA1OUT, TIMER7_MCH0, SPI0_MOSI, TIMER0_MCH0, CMP1_OUT, QSPI_IO2(3), HRTIMER_ST3CH1, TRIGSEL_IN5, UART4_TX, EXMC_A20, EVENTOUT Additional: ADC1_IN3, CMP1_IP, DAC1_OUT1
VDD	A9	P	-	Default: VDD
VBAT	B9	P	-	Default: VBAT
PC14-OSC32IN	C9	I/O	5VT	Default: PC14 Alternate: EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	D9	I/O	5VT	Default: PC15 Alternate: EVENTOUT Additional: OSC32OUT
OSCIN-PF0	E9	I/O	5VT	Default: OSCIN, PF0 Alternate: I2C1_SDA, SPI1_NSS, TIMER0_MCH2, EVENTOUT Additional: ADC0_IN9, OSCIN, CLAIN16
OSCOUT-PF1	F9	I/O	5VT	Default: OSCOUT, PF1 Alternate: TIMER19_BRKIN1, SPI1_SCK, EVENTOUT Additional: ADC1_IN9, CMP2_IM, OSCOUT, CLAIN17
PC3	G9	I/O		Default: PC3 Alternate: LPTIMER_ETI0, TIMER0_CH3, TIMER0_BRKIN2, HPDF_DATAIN1, QSPI_IO2(6), HRTIMER_FLT6, EXMC_NWAIT, EVENTOUT Additional: ADC01_IN8
VSS	H9	P	-	Default: VSS
VDD	J9	P	-	Default: VDD

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) These QSPI pin functions are highly recommended to be used together, and the supported maximum communication clock is 120MHz for this group. Otherwise the QSPI maximum clock frequency cannot be guaranteed.

(4) These QSPI pin functions are highly recommended to be used together, and the supported maximum communication clock is 120MHz for this group. Otherwise the QSPI maximum clock frequency cannot be guaranteed.

(5) These QSPI pin functions are highly recommended to be used together, and the supported maximum communication clock is 200MHz for this group. Otherwise the QSPI maximum clock frequency cannot be guaranteed.

(6) These QSPI pin functions are highly recommended to be used together, and the supported maximum communication clock is 120MHz for this group. Otherwise the QSPI maximum clock frequency cannot be guaranteed.

(7) Refer to the description of the NRST_MDSEL bit field of OB_USER option byte in the GD32G5x3 User Manual to configure the NRST-PG10 pin as a PG10 general GPIO function.

2.6.4. GD32G553MxTx LQFP80 pin definitions

Table 2-6. GD32G553MxTx LQFP80 pin definitions

GD32G553MxTx LQFP80				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
VBAT	1	P	-	Default: VBAT
PC13	2	I/O	5VT	Default: PC13 Alternate: TIMER0_BRKIN0, TIMER0_MCH0, TIMER7_MCH3, EVENTOUT Additional: WKUP1, RTC_TAMP0, RTC_TS, RTC_OUT0
PC14-OSC32IN	3	I/O	5VT	Default: PC14 Alternate: EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	4	I/O	5VT	Default: PC15 Alternate: EVENTOUT Additional: OSC32OUT
OSCIN-PF0	5	I/O	5VT	Default: OSCIN, PF0 Alternate: I2C1_SDA, SPI1_NSS, TIMER0_MCH2, EVENTOUT Additional: ADC0_IN9, OSCIN, CLAIN16
OSCOUT-PF1	6	I/O	5VT	Default: OSCOUT, PF1 Alternate: TIMER19_BRKIN1, SPI1_SCK, EVENTOUT Additional: ADC1_IN9, CMP2_IM, OSCOUT, CLAIN17
NRST-PG10	7	I/O	5VT	Default: NRST Alternate: CK_OUT, EVENTOUT Additional: PG10(7)
PC0	8	I/O	5VT	Default: PC0 Alternate: USART0_RX, LPTIMER_IN0, TIMER0_CH0, HPDF_CKIN0, HPDF_DATAIN4, TRIGSEL_IN8, EXMC_CLK, EVENTOUT Additional: ADC01_IN5, CMP2_IM
PC1	9	I/O		Default: PC1 Alternate: USART0_TX, LPTIMER_OUT, TIMER0_CH1, HPDF_CKIN4, HPDF_DATAIN0, QSPI_IO0(6), TRIGSEL_IN9, EXMC_NOE, EVENTOUT Additional: ADC01_IN6, CMP2_IP
PC2	10	I/O	5VT	Default: PC2 Alternate: HPDF_CKOUT, LPTIMER_IN1, TIMER0_CH2, CMP2_OUT, TIMER19_CH1, HPDF_CKIN1, QSPI_IO1(6), TRIGSEL_IN2, EXMC_NWE, EVENTOUT Additional: ADC01_IN7, CMP7_IP
PC3	11	I/O		Default: PC3 Alternate: LPTIMER_ETI0, TIMER0_CH3, TIMER0_BRKIN2, HPDF_DATAIN1, QSPI_IO2(6), HRTIMER_FLT6, EXMC_NWAIT, EVENTOUT

GD32G553MxTx LQFP80				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Additional: ADC01_IN8
PA0	12	I/O		Default: PA0 Alternate: TIMER1_CH0, TIMER4_CH0, UART3_TX, USART1_CTS, CMP0_OUT, TIMER7_BRKIN0, TIMER7_ETI, HRTIMER_ST6CH0, TRIGSEL_IN0, TIMER1_ETI, EXMC_A13, EVENTOUT Additional: ADC01_IN0, RTC_TAMP1, CMP0_IM, CMP2_IP, WKUP0, CLAIN18
PA1	13	I/O		Default: PA1 Alternate: RTC_REFIN, TIMER1_CH1, TIMER4_CH1, UART3_RX, USART1_RTS, USART1_DE, TIMER14_MCH0, HRTIMER_ST6CH1, TRIGSEL_IN1, EXMC_A14, EVENTOUT Additional: ADC01_IN1, CMP0_IP, CLAIN19
PA2	14	I/O	5VT	Default: PA2 Alternate: TIMER1_CH2, TIMER4_CH2, CLA0OUT, USART1_TX, CMP1_OUT, TIMER14_CH0, QSPI_CSN(3)(6), HRTIMER_ST7CH0, TRIGSEL_IN7, CK_HPDFAUDIO, EXMC_A15, EVENTOUT Additional: ADC0_IN2, CMP1_IM, WKUP3, LSCK_OUT
VSS	15	P	-	Default: VSS
VDD	16	P	-	Default: VDD
PA3	17	I/O		Default: PA3 Alternate: TIMER1_CH3, TIMER4_CH3, USART1_RX, TIMER14_CH1, QSPI_SCK(3), HRTIMER_ST7CH1, TRIGSEL_IN4, EXMC_A16, EVENTOUT Additional: ADC0_IN3, CMP1_IP
PA4	18	I/O		Default: PA4 Alternate: TIMER2_CH1, SPI0_NSS, SPI2_NSS, USART1_CK, HRTIMER_ST2CH0, EXMC_A17, EVENTOUT Additional: ADC1_IN15, DAC0_OUT0, CMP0_IM
PA5	19	I/O		Default: PA5 Alternate: TIMER1_CH0, TIMER1_ETI, SPI0_SCK, USART2_TX, HRTIMER_ST2CH1, EXMC_A18, EVENTOUT Additional: ADC1_IN12, DAC0_OUT1, CMP1_IM
PA6	20	I/O		Default: PA6 Alternate: TIMER15_CH0, TIMER2_CH0, TIMER7_BRKIN0, SPI0_MISO, USART2_RX, TIMER0_BRKIN0, CMP0_OUT, QSPI_IO3(3), HRTIMER_ST3CH0, CK_HPDFAUDIO, EXMC_A19, EVENTOUT Additional: ADC1_IN2, DAC1_OUT0
PA7	21	I/O		Default: PA7

GD32G553MxTx LQFP80				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: TIMER16_CH0, TIMER2_CH1, CLA1OUT, TIMER7_MCH0, SPI0_MOSI, TIMER0_MCH0, CMP1_OUT, QSPI_IO2(3), HRTIMER_ST3CH1, TRIGSEL_IN5, UART4_TX, EXMC_A20, EVENTOUT Additional: ADC1_IN3, CMP1_IP, DAC1_OUT1
PC4	22	I/O	5VT	Default: PC4 Alternate: TIMER0_ETI, I2C1_SCL, USART0_TX, HPDF_CKIN2, QSPI_IO3(3), HRTIMER_FLT7, EXMC_NE0, EVENTOUT Additional: ADC1_IN4
PC5	23	I/O		Default: PC5 Alternate: TIMER14_BRKIN0, TIMER0_MCH3, USART0_RX, HPDF_DATAIN2, HRTIMER_EXEV9, EXMC_NE1, EVENTOUT Additional: ADC1_IN10, WKUP4
PB0	24	I/O		Default: PB0 Alternate: TIMER2_CH2, CLA1OUT, TIMER7_MCH1, HPDF_CKOUT, TIMER0_MCH1, HRTIMER_ST4CH0, QSPI_IO1(3), TRIGSEL_OUT3, HRTIMER_FLT4, EXMC_A1, EVENTOUT Additional: ADC2_IN11, ADC0_IN12, CMP3_IP, CLAIN8
PB1	25	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER7_MCH2, HPDF_DATAIN1, TIMER0_MCH2, TIMER19_MCH0, CMP3_OUT, HRTIMER_ST4CH1, QSPI_IO0(3), TRIGSEL_OUT4, HRTIMER_SCOUT, EXMC_A2, EVENTOUT Additional: ADC2_IN0, ADC0_IN11, CMP0_IP, CLAIN9
PB2	26	I/O		Default: PB2 Alternate: RTC_OUT1, LPTIMER_OUT, TIMER4_CH0, TIMER19_CH0, I2C2_SMBA, HPDF_CKIN1, HRTIMER_ST5CH0, QSPI_IO1(3), HRTIMER_SCIN, EXMC_A3, EVENTOUT Additional: ADC1_IN11, CMP3_IM, CLAIN10
VSSA	27	P	-	Default: VSSA
VREFP	28	P	-	Default: VREFP
VDDA	29	P	-	Default: VDDA
PE7	30	I/O		Default: PE7 Alternate: TIMER0_ETI, HPDF_DATAIN2, EXMC_D4, EVENTOUT Additional: ADC2_IN3, CMP3_IP
PE8	31	I/O	5VT	Default: PE8 Alternate: TIMER4_CH2, TIMER0_MCH0, HPDF_CKIN2, EXMC_D5, EVENTOUT

GD32G553MxTx LQFP80				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Additional: ADC23_IN5, CMP3_IM
PE9	32	I/O	5VT	Default: PE9 Alternate: TIMER4_CH3, TIMER0_CH0, HPDF_CKOUT, SPI0_IO2, EXMC_D6, EVENTOUT Additional: ADC2_IN1, CMP7_IP
PE10	33	I/O	5VT	Default: PE10 Alternate: TIMER0_MCH1, HPDF_DATAIN4, SPI0_IO3, QSPI_SCK(4), EXMC_D7, EVENTOUT Additional: ADC2_IN12, ADC3_IN13
PE11	34	I/O	5VT	Default: PE11 Alternate: TIMER0_CH1, HPDF_CKIN4, QSPI_CSN(4), EXMC_D8, EVENTOUT Additional: ADC2_IN13, ADC3_IN14
PE12	35	I/O	5VT	Default: PE12 Alternate: TIMER0_MCH2, HPDF_DATAIN5, QSPI_IO0(4), EXMC_D9, EVENTOUT Additional: ADC2_IN14, ADC3_IN15
PE13	36	I/O	5VT	Default: PE13 Alternate: TIMER0_CH2, HPDF_CKIN5, QSPI_IO1(4), EXMC_D10, EVENTOUT Additional: ADC2_IN2
PE14	37	I/O	5VT	Default: PE14 Alternate: TIMER0_CH3, TIMER0_BRKIN2, QSPI_IO2(4), EXMC_D11, EVENTOUT Additional: ADC3_IN0
PE15	38	I/O	5VT	Default: PE15 Alternate: TIMER0_BRKIN0, TIMER0_MCH3, USART2_RX, QSPI_IO3(4), EXMC_D12, EVENTOUT Additional: ADC3_IN1
PB10	39	I/O		Default: PB10 Alternate: TIMER1_CH2, HPDF_DATAIN0, HPDF_DATAIN7, USART2_TX, QSPI_SCK(4), TIMER0_BRKIN0, HRTIMER_FLT2, TRIGSEL_OUT2, EXMC_A7, EVENTOUT Additional: CMP4_IM
VSS	40	P	-	Default: VSS
VDD	41	P	-	Default: VDD
PB11	42	I/O		Default: PB11 Alternate: TIMER1_CH3, HPDF_DATAIN3, HPDF_CKIN7, USART2_RX, QSPI_CSN(4), HRTIMER_FLT3, EXMC_A8, EVENTOUT Additional: ADC01_IN13, CMP5_IP
PB12	43	I/O		Default: PB12 Alternate: TIMER4_ETI, I2C1_SMBA, SPI1_NSS, TIMER0_BRKIN0, USART2_CK, CAN1_RX,

GD32G553MxTx LQFP80				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				HPDF_DATAIN1, HRTIMER_ST2CH0, EXMC_A9, EVENTOUT Additional: ADC3_IN2, ADC0_IN10, CMP6_IM
PB13	44	I/O		Default: PB13 Alternate: SPI1_SCK, TIMER0_MCH0, USART2_CTS, CAN1_TX, HPDF_CKIN1, HRTIMER_ST2CH1, EXMC_A10, EVENTOUT Additional: ADC2_IN4, CMP4_IP
PB14	45	I/O		Default: PB14 Alternate: TIMER14_CH0, SPI1_MISO, TIMER0_MCH1, USART2_RTS, USART2_DE, CMP3_OUT, HPDF_DATAIN2, HRTIMER_ST3CH0, TRIGSEL_OUT1, EXMC_A11, EVENTOUT Additional: ADC3_IN3, ADC0_IN4, CMP6_IP
PB15	46	I/O		Default: PB15 Alternate: RTC_REFIN, TIMER14_CH1, TIMER14_MCH0, CMP2_OUT, TIMER0_MCH2, SPI1_MOSI, HPDF_CKIN2, HRTIMER_ST3CH1, TRIGSEL_OUT5, EXMC_A12, EVENTOUT Additional: ADC3_IN4, ADC1_IN14, CMP5_IM
PD8	47	I/O		Default: PD8 Alternate: HPDF_CKIN3, USART2_TX, EXMC_D13, EVENTOUT Additional: ADC3_IN11, CMP7_IM
PD9	48	I/O		Default: PD9 Alternate: HPDF_DATAIN3, USART2_RX, EXMC_D14, EVENTOUT Additional: ADC3_IN12, CMP7_IM
PD10	49	I/O	5VT	Default: PD10 Alternate: HPDF_CKOUT, USART2_CK, EXMC_D15, EVENTOUT Additional: ADC23_IN6, CMP5_IM
VSS	50	P	-	Default: VSS
VDD	51	P	-	Default: VDD
PC6	52	I/O	5VT	Default: PC6 Alternate: HPDF_CKIN3, TIMER0_BRKIN1, CMP5_OUT, TIMER2_CH0, HRTIMER_EXEV9, TIMER7_CH0, I2C3_SCL, HRTIMER_ST5CH0, EXMC_NE2, EVENTOUT
PC7	53	I/O	5VT	Default: PC7 Alternate: HPDF_DATAIN3, TIMER2_CH1, HRTIMER_FLT4, TIMER7_CH1, CMP4_OUT, I2C3_SDA, HRTIMER_ ST5CH1, EXMC_NE3, EVENTOUT
PC8	54	I/O	5VT	Default: PC8

GD32G553MxTx LQFP80				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: TIMER2_CH2, HRTIMER_ST4CH0, TIMER7_CH2, TIMER19_CH2, CMP6_OUT, I2C2_SCL, EXMC_NBL0, EVENTOUT
PC9	55	I/O	5VT	Default: PC9 Alternate: TIMER2_CH3, HRTIMER_ST4CH1, TIMER7_CH3, TIMER7_BRKIN2, I2C2_SDA, EXMC_NBL1, EVENTOUT
PA8	56	I/O	5VT	Default: PA8 Alternate: CK_OUT, I2C2_SCL, I2C1_SDA, TIMER0_CH0, USART0_CK, CMP6_OUT, TIMER3_ETI, CAN2_RX, SPI1_NSS, HRTIMER_ST0CH0, UART4_RX, EXMC_A21, EVENTOUT Additional: ADC3_IN16, NMI, CLAIN11
PA9	57	I/O	5VT	Default: PA9 Alternate: I2C2_SMBA, I2C1_SCL, TIMER0_CH1, USART0_TX, CMP4_OUT, TIMER14_BRKIN0, TIMER1_CH2, SPI1_SCK, HRTIMER_ST0CH1, TRIGSEL_IN13, EXMC_A22, EVENTOUT Additional: ADC3_IN17, CLAIN12
PA10	58	I/O	5VT	Default: PA10 Alternate: TIMER16_BRKIN0, CLA2OUT, I2C1_SMBA, SPI1_MISO, TIMER0_CH2, USART0_RX, CMP5_OUT, TIMER1_CH3, TIMER7_BRKIN0, HRTIMER_ST1CH0, TRIGSEL_IN12, EXMC_A23, EVENTOUT Additional: CLAIN13, LVD_IN
PA11	59	I/O	5VT	Default: PA11 Alternate: CLA3OUT, SPI1_MOSI, TIMER0_MCH0, USART0_CTS, CMP0_OUT, CAN0_RX, TIMER3_CH0, TIMER0_CH3, TIMER0_BRKIN2, HRTIMER_ST1CH1, TRIGSEL_IN13, EXMC_A24, EVENTOUT Additional: CLAIN14
PA12	60	I/O	5VT	Default: PA12 Alternate: TIMER15_CH0, TIMER0_MCH1, USART0_RTS, USART0_DE, CMP1_OUT, CAN0_TX, TIMER3_CH1, TIMER0_ETI, HRTIMER_FLT0, TRIGSEL_IN12, EXMC_A25, EVENTOUT Additional: CLAIN15
VSS	61	P	-	Default: VSS
VDD	62	P	-	Default: VDD
PA13	63	I/O	5VT	Default: JTMS, SWDIO, PA13 Alternate: TIMER15_MCH0, TIMER0_BRKIN1, I2C3_SCL, I2C0_SCL, IFRP_OUT, TIMER7_BRKIN1, USART2_CTS, CMP7_OUT, TIMER3_CH2, TRIGSEL_IN10, EXMC_A5, EVENTOUT

GD32G553MxTx LQFP80				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PA14	64	I/O	5VT	Default: JTCK, SWCLK, PA14 Alternate: LPTIMER_OUT, I2C3_SMBA, I2C0_SDA, TIMER7_CH1, TIMER0_BRKIN0, USART1_TX, CMP7_OUT, TRIGSEL_IN11, EVENTOUT
PA15	65	I/O	5VT	Default: JTDI, PA15 Alternate: TIMER1_CH0, TIMER7_CH0, CLA3OUT, I2C0_SCL, SPI0_NSS, SPI2_NSS, USART1_RX, UART3_RTS, UART3_DE, TIMER0_BRKIN0, CAN2_TX, TRIGSEL_OUT0, HRTIMER_FLT1, TIMER1_ETI, EVENTOUT Additional: CLAIN0
PC10	66	I/O	5VT	Default: PC10 Alternate: HPDF_CKIN5, TIMER7_MCH0, UART3_TX, SPI2_SCK, USART2_TX, HRTIMER_FLT5, EXMC_D0, EVENTOUT
PC11	67	I/O	5VT	Default: PC11 Alternate: HPDF_DATAIN5, HRTIMER_EXEV1, TIMER7_MCH1, UART3_RX, SPI2_MISO, USART2_RX, I2C2_SDA, EXMC_D1,EVENTOUT
PC12	68	I/O	5VT	Default: PC12 Alternate: TIMER4_CH1, HRTIMER_EXEV0, TIMER7_MCH2, UART4_TX, SPI2_MOSI, USART2_CK, EXMC_A0, EVENTOUT
PD0	69	I/O	5VT	Default: PD0 Alternate: HPDF_CKIN6, TIMER7_MCH3, CAN0_RX, EXMC_D2, TRIGSEL_IN3, EVENTOUT
PD1	70	I/O	5VT	Default: PD1 Alternate: HPDF_DATAIN6, TIMER7_CH3, TIMER7_BRKIN2, CAN0_TX, EXMC_D3, TRIGSEL_IN6, QSPI_DQS(5), EVENTOUT
PD2	71	I/O	5VT	Default: PD2 Alternate: TIMER2_ETI, TIMER7_BRKIN0, UART4_RX, QSPI_SCK(5), EVENTOUT
PB3	72	I/O	5VT	Default: JTDO, PB3 Alternate: TIMER1_CH1, TIMER3_ETI, CLA0OUT, TIMER7_MCH0, SPI0_SCK, SPI2_SCK, USART1_TX, HRTIMER_ST5CH1, TIMER2_ETI, CAN2_RX, HRTIMER_SCOUT, HRTIMER_EXEV8, TRIGSEL_OUT7, EVENTOUT Additional: CLAIN1
PB4	73	I/O	5VT	Default: NJTRST, PB4 Alternate: TIMER15_CH0, TIMER2_CH0, CLA1OUT, TIMER7_MCH1, SPI0_MISO, SPI2_MISO, USART1_RX, UART4_RTS, UART4_DE, TIMER16_BRKIN0, CAN2_TX, HRTIMER_EXEV6, TRIGSEL_OUT6, EVENTOUT

GD32G553MxTx LQFP80				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Additional: CLAIN2
PB5	74	I/O	5VT	Default: PB5 Alternate: HPDF_CKIN0, TIMER15_BRKIN0, TIMER2_CH1, TIMER7_MCH2, I2C0_SMBA, SPI0_MOSI, SPI2_MOSI, USART1_CK, I2C2_SDA, CAN1_RX, TIMER16_CH0, LPTIMER_IN0, CLA2OUT, HRTIMER_EXEV5, UART4_CTS, EVENTOUT Additional: CLAIN3
PB6	75	I/O	5VT	Default: PB6 Alternate: HPDF_DATAIN5, TIMER15_MCH0, TIMER3_CH0, I2C0_SCL, TIMER7_CH0, TIMER7_ETI, USART0_TX, CMP3_OUT, CAN1_TX, TIMER7_BRKIN2, LPTIMER_ETI0, HRTIMER_SCIN, HRTIMER_EXEV3, EXMC_A4, EVENTOUT Additional: CLAIN4
PB7	76	I/O	5VT	Default: PB7 Alternate: HPDF_CKIN5, TIMER16_MCH0, TIMER3_CH1, I2C3_SDA, I2C0_SDA, TIMER7_BRKIN0, USART0_RX, CMP2_OUT, TIMER2_CH3, LPTIMER_IN1, EXMC_NL/EXMC_NADV, HRTIMER_EXEV2, UART3_CTS, QSPI_DQS(3)(4)(6), HRTIMER_ST5CH1, EVENTOUT Additional: CLAIN5
PB8/BOOT0	77	I/O	5VT	Default: BOOT0, PB8 Alternate: TIMER15_CH0, TIMER3_CH2, HPDF_CKIN7, I2C0_SCL, CLA3OUT, USART2_RX, CMP0_OUT, CAN0_RX, TIMER7_CH1, TIMER0_BRKIN0, HRTIMER_EXEV7, EVENTOUT Additional: CLAIN6
PB9	78	I/O	5VT	Default: PB9 Alternate: TIMER16_CH0, TIMER3_CH3, HPDF_DATAIN7, I2C0_SDA, IFRP_OUT, USART2_TX, CMP1_OUT, CAN0_TX, TIMER7_CH2, TIMER0_MCH2, HRTIMER_EXEV4, EXMC_A6, EVENTOUT Additional: CLAIN7
VSS	79	P	-	Default: VSS
VDD	80	P	-	Default: VDD

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) These QSPI pin functions are highly recommended to be used together, and the supported maximum communication clock is 120MHz for this group. Otherwise the QSPI maximum clock frequency cannot be guaranteed.

(4) These QSPI pin functions are highly recommended to be used together, and the supported maximum communication clock is 120MHz for this group. Otherwise the QSPI maximum clock frequency cannot be guaranteed.

(5) These QSPI pin functions are highly recommended to be used together, and the supported maximum communication clock is 200MHz for this group. Otherwise the QSPI maximum clock frequency cannot be guaranteed.

(6) These QSPI pin functions are highly recommended to be used together, and the supported maximum communication clock is 120MHz for this group. Otherwise the QSPI maximum clock frequency cannot be guaranteed.

(7) Refer to the description of the NRST_MDSEL bit field of OB_USER option byte in the GD32G5x3 User Manual to configure the NRST-PG10 pin as a PG10 general GPIO function.

2.6.5. GD32G553RxTx LQFP64 pin definitions

Table 2-7. GD32G553RxTx LQFP64 pin definitions

GD32G553RxTx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
VBAT	1	P	-	Default: VBAT
PC13	2	I/O	5VT	Default: PC13 Alternate: TIMER0_BRKIN0, TIMER0_MCH0, TIMER7_MCH3, EVENTOUT Additional: WKUP1, RTC_TAMP0, RTC_TS, RTC_OUT0
PC14-OSC32IN	3	I/O	5VT	Default: PC14 Alternate: EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	4	I/O	5VT	Default: PC15 Alternate: EVENTOUT Additional: OSC32OUT
OSCIN-PF0	5	I/O	5VT	Default: OSCIN, PF0 Alternate: I2C1_SDA, SPI1_NSS, TIMER0_MCH2, EVENTOUT Additional: ADC0_IN9, OSCIN, CLAIN16
OSCOUT-PF1	6	I/O	5VT	Default: OSCOUT, PF1 Alternate: TIMER19_BRKIN1, SPI1_SCK, EVENTOUT Additional: ADC1_IN9, CMP2_IM, OSCOUT, CLAIN17
NRST-PG10	7	I/O	5VT	Default: NRST Alternate: CK_OUT, EVENTOUT Additional: PG10(7)
PC0	8	I/O	5VT	Default: PC0 Alternate: USART0_RX, LPTIMER_IN0, TIMER0_CH0, HPDF_CKIN0, HPDF_DATAIN4, TRIGSEL_IN8, EVENTOUT Additional: ADC01_IN5, CMP2_IM
PC1	9	I/O		Default: PC1 Alternate: USART0_TX, LPTIMER_OUT, TIMER0_CH1, HPDF_CKIN4, HPDF_DATAIN0, QSPI_IO0(6), TRIGSEL_IN9, EVENTOUT Additional: ADC01_IN6, CMP2_IP
PC2	10	I/O	5VT	Default: PC2 Alternate: HPDF_CKOUT, LPTIMER_IN1, TIMER0_CH2, CMP2_OUT, TIMER19_CH1, HPDF_CKIN1, QSPI_IO1(6), TRIGSEL_IN2, EVENTOUT Additional: ADC01_IN7
PC3	11	I/O		Default: PC3 Alternate: LPTIMER_ETI0, TIMER0_CH3, TIMER0_BRKIN2, HPDF_DATAIN1, QSPI_IO2(6), HRTIMER_FLT6, EVENTOUT

GD32G553RxTx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Additional: ADC01_IN8
PA0	12	I/O		Default: PA0 Alternate: TIMER1_CH0, TIMER4_CH0, UART3_TX, USART1_CTS, CMP0_OUT, TIMER7_BRKIN0, TIMER7_ETI, HRTIMER_ST6CH0, TRIGSEL_IN0, TIMER1_ETI, EVENTOUT Additional: ADC01_IN0, RTC_TAMP1, CMP0_IM, CMP2_IP, WKUP0, CLAIN18
PA1	13	I/O		Default: PA1 Alternate: RTC_REFIN, TIMER1_CH1, TIMER4_CH1, UART3_RX, USART1_RTS, USART1_DE, TIMER14_MCH0, HRTIMER_ST6CH1, TRIGSEL_IN1, EVENTOUT Additional: ADC01_IN1, CMP0_IP, CLAIN19
PA2	14	I/O	5VT	Default: PA2 Alternate: TIMER1_CH2, TIMER4_CH2, CLA0OUT, USART1_TX, CMP1_OUT, TIMER14_CH0, QSPI_CSN(3)(6), HRTIMER_ST7CH0, TRIGSEL_IN7, CK_HPDFAUDIO, EVENTOUT Additional: ADC0_IN2, CMP1_IM, WKUP3, LSCK_OUT
VSS	15	P	-	Default: VSS
VDD	16	P	-	Default: VDD
PA3	17	I/O		Default: PA3 Alternate: TIMER1_CH3, TIMER4_CH3, USART1_RX, TIMER14_CH1, QSPI_SCK(3), HRTIMER_ST7CH1, TRIGSEL_IN4, EVENTOUT Additional: ADC0_IN3, CMP1_IP
PA4	18	I/O		Default: PA4 Alternate: TIMER2_CH1, SPI0_NSS, SPI2_NSS, USART1_CK, HRTIMER_ST2CH0, EVENTOUT Additional: ADC1_IN15, DAC0_OUT0, CMP0_IM
PA5	19	I/O		Default: PA5 Alternate: TIMER1_CH0, TIMER1_ETI, SPI0_SCK, USART2_TX, HRTIMER_ST2CH1, EVENTOUT Additional: ADC1_IN12, DAC0_OUT1, CMP1_IM
PA6	20	I/O		Default: PA6 Alternate: TIMER15_CH0, TIMER2_CH0, TIMER7_BRKIN0, SPI0_MISO, USART2_RX, TIMER0_BRKIN0, CMP0_OUT, QSPI_IO3(3), HRTIMER_ST3CH0, CK_HPDFAUDIO, EVENTOUT Additional: ADC1_IN2, DAC1_OUT0
PA7	21	I/O		Default: PA7 Alternate: TIMER16_CH0, TIMER2_CH1, CLA1OUT, TIMER7_MCH0, SPI0_MOSI, TIMER0_MCH0, CMP1_OUT, QSPI_IO2(3), HRTIMER_ST3CH1,

GD32G553RxTx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				TRIGSEL_IN5, UART4_TX, EVENTOUT Additional: ADC1_IN3, CMP1_IP, DAC1_OUT1
PC4	22	I/O	5VT	Default: PC4 Alternate: TIMER0_ETI, I2C1_SCL, USART0_TX, HPDF_CKIN2, QSPI_IO3(3), HRTIMER_FLT7, EVENTOUT Additional: ADC1_IN4
PC5	23	I/O		Default: PC5 Alternate: TIMER14_BRKIN0, TIMER0_MCH3, USART0_RX, HPDF_DATAIN2, HRTIMER_EXEV9, EVENTOUT Additional: ADC1_IN10, WKUP4
PB0	24	I/O		Default: PB0 Alternate: TIMER2_CH2, CLA1OUT, TIMER7_MCH1, HPDF_CKOUT, TIMER0_MCH1, HRTIMER_ST4CH0, QSPI_IO1(3), TRIGSEL_OUT3, HRTIMER_FLT4, EVENTOUT Additional: ADC2_IN11, ADC0_IN12, CMP3_IP, CLAIN8
PB1	25	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER7_MCH2, HPDF_DATAIN1, TIMER0_MCH2, TIMER19_MCH0, CMP3_OUT, HRTIMER_ST4CH1, QSPI_IO0(3), TRIGSEL_OUT4, HRTIMER_SCOUT, EVENTOUT Additional: ADC2_IN0, ADC0_IN11, CMP0_IP, CLAIN9
PB2	26	I/O		Default: PB2 Alternate: RTC_OUT1, LPTIMER_OUT, TIMER4_CH0, TIMER19_CH0, I2C2_SMBA, HPDF_CKIN1, HRTIMER_ST5CH0, QSPI_IO1(3), HRTIMER_SCIN, EVENTOUT Additional: ADC1_IN11, CMP3_IM, CLAIN10
VSSA	27	P	-	Default: VSSA
VREFP	28	P	-	Default: VREFP
VDDA	29	P	-	Default: VDDA
PB10	30	I/O		Default: PB10 Alternate: TIMER1_CH2, HPDF_DATAIN0, HPDF_DATAIN7, USART2_TX, QSPI_SCK(4), TIMER0_BRKIN0, HRTIMER_FLT2, TRIGSEL_OUT2, EVENTOUT Additional: CMP4_IM
VSS	31	P	-	Default: VSS
VDD	32	P	-	Default: VDD
PB11	33	I/O		Default: PB11 Alternate: TIMER1_CH3, HPDF_DATAIN3, HPDF_CKIN7, USART2_RX, QSPI_CSN(4),

GD32G553RxTx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				HRTIMER_FLT3, EVENTOUT Additional: ADC01_IN13, CMP5_IP
PB12	34	I/O		Default: PB12 Alternate: TIMER4_ETI, I2C1_SMBA, SPI1_NSS, TIMER0_BRKIN0, USART2_CK, CAN1_RX, HPDF_DATAIN1, HRTIMER_ST2CH0, EVENTOUT Additional: ADC3_IN2, ADC0_IN10, CMP6_IM
PB13	35	I/O		Default: PB13 Alternate: SPI1_SCK, TIMER0_MCH0, USART2_CTS, CAN1_TX, HPDF_CKIN1, HRTIMER_ST2CH1, EVENTOUT Additional: ADC2_IN4, CMP4_IP
PB14	36	I/O		Default: PB14 Alternate: TIMER14_CH0, SPI1_MISO, TIMER0_MCH1, USART2_RTS, USART2_DE, CMP3_OUT, HPDF_DATAIN2, HRTIMER_ST3CH0, TRIGSEL_OUT1, EVENTOUT Additional: ADC3_IN3, ADC0_IN4, CMP6_IP
PB15	37	I/O		Default: PB15 Alternate: RTC_REFIN, TIMER14_CH1, TIMER14_MCH0, CMP2_OUT, TIMER0_MCH2, SPI1_MOSI, HPDF_CKIN2, HRTIMER_ST3CH1, TRIGSEL_OUT5, EVENTOUT Additional: ADC3_IN4, ADC1_IN14, CMP5_IM
PC6	38	I/O	5VT	Default: PC6 Alternate: HPDF_CKIN3, TIMER0_BRKIN1, CMP5_OUT, TIMER2_CH0, HRTIMER_EXEV9, TIMER7_CH0, I2C3_SCL, HRTIMER_ST5CH0, EVENTOUT
PC7	39	I/O	5VT	Default: PC7 Alternate: HPDF_DATAIN3, TIMER2_CH1, HRTIMER_FLT4, TIMER7_CH1, CMP4_OUT, I2C3_SDA, HRTIMER_ ST5CH1, EVENTOUT
PC8	40	I/O	5VT	Default: PC8 Alternate: TIMER2_CH2, HRTIMER_ST4CH0, TIMER7_CH2, TIMER19_CH2, CMP6_OUT, I2C2_SCL, EVENTOUT
PC9	41	I/O	5VT	Default: PC9 Alternate: TIMER2_CH3, HRTIMER_ST4CH1, TIMER7_CH3, TIMER7_BRKIN2, I2C2_SDA, EVENTOUT
PA8	42	I/O	5VT	Default: PA8 Alternate: CK_OUT, I2C2_SCL, I2C1_SDA, TIMER0_CH0, USART0_CK, CMP6_OUT, TIMER3_ETI, CAN2_RX, SPI1_NSS, HRTIMER_ST0CH0, UART4_RX, EVENTOUT

GD32G553RxTx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Additional: ADC3_IN16, NMI, CLAIN11
PA9	43	I/O	5VT	Default: PA9 Alternate: I2C2_SMBA, I2C1_SCL, TIMER0_CH1, USART0_TX, CMP4_OUT, TIMER14_BRKIN0, TIMER1_CH2, SPI1_SCK, HRTIMER_ST0CH1, TRIGSEL_IN13, EVENTOUT Additional: ADC3_IN17, CLAIN12
PA10	44	I/O	5VT	Default: PA10 Alternate: TIMER16_BRKIN0, CLA2OUT, I2C1_SMBA, SPI1_MISO, TIMER0_CH2, USART0_RX, CMP5_OUT, TIMER1_CH3, TIMER7_BRKIN0, HRTIMER_ST1CH0, TRIGSEL_IN12, EVENTOUT Additional: CLAIN13, LVD_IN
PA11	45	I/O	5VT	Default: PA11 Alternate: CLA3OUT, SPI1_MOSI, TIMER0_MCH0, USART0_CTS, CMP0_OUT, CAN0_RX, TIMER3_CH0, TIMER0_CH3, TIMER0_BRKIN2, HRTIMER_ST1CH1, TRIGSEL_IN13, EVENTOUT Additional: CLAIN14
PA12	46	I/O	5VT	Default: PA12 Alternate: TIMER15_CH0, TIMER0_MCH1, USART0_RTS, USART0_DE, CMP1_OUT, CAN0_TX, TIMER3_CH1, TIMER0_ETI, HRTIMER_FLT0, TRIGSEL_IN12, EVENTOUT Additional: CLAIN15
VSS	47	P	-	Default: VSS
VDD	48	P	-	Default: VDD
PA13	49	I/O	5VT	Default: JTMS, SWDIO, PA13 Alternate: TIMER15_MCH0, TIMER0_BRKIN1, I2C3_SCL, I2C0_SCL, IFRP_OUT, TIMER7_BRKIN1, USART2_CTS, TIMER3_CH2, TRIGSEL_IN10, EVENTOUT
PA14	50	I/O	5VT	Default: JTCK, SWCLK, PA14 Alternate: LPTIMER_OUT, I2C3_SMBA, I2C0_SDA, TIMER7_CH1, TIMER0_BRKIN0, USART1_TX, TRIGSEL_IN11, EVENTOUT
PA15	51	I/O	5VT	Default: JTDI, PA15 Alternate: TIMER1_CH0, TIMER7_CH0, CLA3OUT, I2C0_SCL, SPI0_NSS, SPI2_NSS, USART1_RX, UART3_RTS, UART3_DE, TIMER0_BRKIN0, CAN2_TX, TRIGSEL_OUT0, HRTIMER_FLT1, TIMER1_ETI, EVENTOUT Additional: CLAIN0
PC10	52	I/O	5VT	Default: PC10 Alternate: HPDF_CKIN5, TIMER7_MCH0, UART3_TX,

GD32G553RxTx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				SPI2_SCK, USART2_TX, HRTIMER_FLT5, EVENTOUT
PC11	53	I/O	5VT	Default: PC11 Alternate: HPDF_DATAIN5, HRTIMER_EXEV1, TIMER7_MCH1, UART3_RX, SPI2_MISO, USART2_RX, I2C2_SDA, EVENTOUT
PC12	54	I/O	5VT	Default: PC12 Alternate: TIMER4_CH1, HRTIMER_EXEV0, TIMER7_MCH2, UART4_TX, SPI2_MOSI, USART2_CK, EVENTOUT
PD2	55	I/O	5VT	Default: PD2 Alternate: TIMER2_ETI, TIMER7_BRKIN0, UART4_RX, QSPI_SCK(5), EVENTOUT
PB3	56	I/O	5VT	Default: JTDO, PB3 Alternate: TIMER1_CH1, TIMER3_ETI, CLA0OUT, TIMER7_MCH0, SPI0_SCK, SPI2_SCK, USART1_TX, HRTIMER_ST5CH1, TIMER2_ETI, CAN2_RX, HRTIMER_SCOUT, HRTIMER_EXEV8, TRIGSEL_OUT7, EVENTOUT Additional: CLAIN1
PB4	57	I/O	5VT	Default: NJTRST, PB4 Alternate: TIMER15_CH0, TIMER2_CH0, CLA1OUT, TIMER7_MCH1, SPI0_MISO, SPI2_MISO, USART1_RX, UART4_RTS, UART4_DE, TIMER16_BRKIN0, CAN2_TX, HRTIMER_EXEV6, TRIGSEL_OUT6, EVENTOUT Additional: CLAIN2
PB5	58	I/O	5VT	Default: PB5 Alternate: HPDF_CKIN0, TIMER15_BRKIN0, TIMER2_CH1, TIMER7_MCH2, I2C0_SMBA, SPI0_MOSI, SPI2_MOSI, USART1_CK, I2C2_SDA, CAN1_RX, TIMER16_CH0, LPTIMER_IN0, CLA2OUT, HRTIMER_EXEV5, UART4_CTS, EVENTOUT Additional: CLAIN3
PB6	59	I/O	5VT	Default: PB6 Alternate: HPDF_DATAIN5, TIMER15_MCH0, TIMER3_CH0, I2C0_SCL, TIMER7_CH0, TIMER7_ETI, USART0_TX, CMP3_OUT, CAN1_TX, TIMER7_BRKIN2, LPTIMER_ETI0, HRTIMER_SCIN, HRTIMER_EXEV3, EVENTOUT Additional: CLAIN4
PB7	60	I/O	5VT	Default: PB7 Alternate: HPDF_CKIN5, TIMER16_MCH0, TIMER3_CH1, I2C3_SDA, I2C0_SDA, TIMER7_BRKIN0, USART0_RX, CMP2_OUT, TIMER2_CH3, LPTIMER_IN1, HRTIMER_EXEV2,

GD32G553RxTx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				UART3_CTS, QSPI_DQS(3)(4)(6), HRTIMER_ST5CH1, EVENTOUT Additional: CLAIN5
PB8/BOOT0	61	I/O	5VT	Default: BOOT0, PB8 Alternate: TIMER15_CH0, TIMER3_CH2, HPDF_CKIN7, I2C0_SCL, CLA3OUT, USART2_RX, CMP0_OUT, CAN0_RX, TIMER7_CH1, TIMER0_BRKIN0, HRTIMER_EXEV7, EVENTOUT Additional: CLAIN6
PB9	62	I/O	5VT	Default: PB9 Alternate: TIMER16_CH0, TIMER3_CH3, HPDF_DATAIN7, I2C0_SDA, IFRP_OUT, USART2_TX, CMP1_OUT, CAN0_TX, TIMER7_CH2, TIMER0_MCH2, HRTIMER_EXEV4, EVENTOUT Additional: CLAIN7
VSS	63	P	-	Default: VSS
VDD	64	P	-	Default: VDD

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) These QSPI pin functions are highly recommended to be used together, and the supported maximum communication clock is 120MHz for this group. Otherwise the QSPI maximum clock frequency cannot be guaranteed.

(4) These QSPI pin functions are highly recommended to be used together, and the supported maximum communication clock is 120MHz for this group. Otherwise the QSPI maximum clock frequency cannot be guaranteed.

(5) These QSPI pin functions are highly recommended to be used together, and the supported maximum communication clock is 200MHz for this group. Otherwise the QSPI maximum clock frequency cannot be guaranteed.

(6) These QSPI pin functions are highly recommended to be used together, and the supported maximum communication clock is 120MHz for this group. Otherwise the QSPI maximum clock frequency cannot be guaranteed.

(7) Refer to the description of the NRST_MDSEL bit field of OB_USER option byte in the GD32G5x3 User Manual to configure the NRST-PG10 pin as a PG10 general GPIO function.

2.6.6. GD32G553CxTx LQFP48 pin definitions

Table 2-8. GD32G553CxTx LQFP48 pin definitions

GD32G553CxTx LQFP48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
VBAT	1	P	-	Default: VBAT
PC13	2	I/O	5VT	Default: PC13 Alternate: TIMER0_BRKIN0, TIMER0_MCH0, TIMER7_MCH3, EVENTOUT Additional: WKUP1, RTC_TAMP0, RTC_TS, RTC_OUT0
PC14-OSC32IN	3	I/O	5VT	Default: PC14 Alternate: EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	4	I/O	5VT	Default: PC15 Alternate: EVENTOUT Additional: OSC32OUT
OSCIN-PF0	5	I/O	5VT	Default: OSCIN, PF0 Alternate: I2C1_SDA, SPI1_NSS, TIMER0_MCH2, EVENTOUT Additional: ADC0_IN9, OSCIN, CLAIN16
OSCOUT-PF1	6	I/O	5VT	Default: OSCOUT, PF1 Alternate: TIMER19_BRKIN1, SPI1_SCK, EVENTOUT Additional: ADC1_IN9, CMP2_IM, OSCOUT, CLAIN17
NRST-PG10	7	I/O	5VT	Default: NRST Alternate: CK_OUT, EVENTOUT Additional: PG10(7)
PA0	8	I/O		Default: PA0 Alternate: TIMER1_CH0, TIMER4_CH0, UART3_TX, USART1_CTS, CMP0_OUT, TIMER7_BRKIN0, TIMER7_ETI, HRTIMER_ST6CH0, TRIGSEL_IN0, TIMER1_ETI, EVENTOUT Additional: ADC01_IN0, RTC_TAMP1, CMP0_IM, CMP2_IP, WKUP0, CLAIN18
PA1	9	I/O		Default: PA1 Alternate: RTC_REFIN, TIMER1_CH1, TIMER4_CH1, UART3_RX, USART1_RTS, USART1_DE, TIMER14_MCH0, HRTIMER_ST6CH1, TRIGSEL_IN1, EVENTOUT Additional: ADC01_IN1, CMP0_IP, CLAIN19
PA2	10	I/O	5VT	Default: PA2 Alternate: TIMER1_CH2, TIMER4_CH2, CLA0OUT, USART1_TX, CMP1_OUT, TIMER14_CH0, QSPI_CSN(3)(6), HRTIMER_ST7CH0, TRIGSEL_IN7, CK_HPDFAUDIO, EVENTOUT Additional: ADC0_IN2, CMP1_IM, WKUP3, LSCK_OUT

GD32G553CxTx LQFP48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PA3	11	I/O		Default: PA3 Alternate: TIMER1_CH3, TIMER4_CH3, USART1_RX, TIMER14_CH1, QSPI_SCK(3), HRTIMER_ST7CH1, TRIGSEL_IN4, EVENTOUT Additional: ADC0_IN3, CMP1_IP
PA4	12	I/O		Default: PA4 Alternate: TIMER2_CH1, SPI0_NSS, SPI2_NSS, USART1_CK, HRTIMER_ST2CH0, EVENTOUT Additional: ADC1_IN15, DAC0_OUT0, CMP0_IM
PA5	13	I/O		Default: PA5 Alternate: TIMER1_CH0, TIMER1_ETI, SPI0_SCK, USART2_TX, HRTIMER_ST2CH1, EVENTOUT Additional: ADC1_IN12, DAC0_OUT1, CMP1_IM
PA6	14	I/O		Default: PA6 Alternate: TIMER15_CH0, TIMER2_CH0, TIMER7_BRKIN0, SPI0_MISO, USART2_RX, TIMER0_BRKIN0, CMP0_OUT, QSPI_IO3(3), HRTIMER_ST3CH0, CK_HPDFAUDIO, EVENTOUT Additional: ADC1_IN2, DAC1_OUT0
PA7	15	I/O		Default: PA7 Alternate: TIMER16_CH0, TIMER2_CH1, CLA1OUT, TIMER7_MCH0, SPI0_MOSI, TIMER0_MCH0, CMP1_OUT, QSPI_IO2(3), HRTIMER_ST3CH1, TRIGSEL_IN5, UART4_TX, EVENTOUT Additional: ADC1_IN3, CMP1_IP, DAC1_OUT1
PB0	16	I/O		Default: PB0 Alternate: TIMER2_CH2, CLA1OUT, TIMER7_MCH1, HPDF_CKOUT, TIMER0_MCH1, HRTIMER_ST4CH0, QSPI_IO1(3), TRIGSEL_OUT3, HRTIMER_FLT4, EVENTOUT Additional: ADC2_IN11, ADC0_IN12, CMP3_IP, CLAIN8
PB1	17	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER7_MCH2, HPDF_DATAIN1, TIMER0_MCH2, TIMER19_MCH0, CMP3_OUT, HRTIMER_ST4CH1, QSPI_IO0(3), TRIGSEL_OUT4, HRTIMER_SCOUT, EVENTOUT Additional: ADC2_IN0, ADC0_IN11, CMP0_IP, CLAIN9
PB2	18	I/O		Default: PB2 Alternate: RTC_OUT1, LPTIMER_OUT, TIMER4_CH0, TIMER19_CH0, I2C2_SMBA, HPDF_CKIN1, HRTIMER_ST5CH0, QSPI_IO1(3), HRTIMER_SCIN, EVENTOUT Additional: ADC1_IN11, CMP3_IM, CLAIN10
VSSA	19	P	-	Default: VSSA

GD32G553CxTx LQFP48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
VREFP	20	P	-	Default: VREFP
VDDA	21	P	-	Default: VDDA
PB10	22	I/O		Default: PB10 Alternate: TIMER1_CH2, HPDF_DATAIN0, HPDF_DATAIN7, USART2_TX, QSPI_SCK(4), TIMER0_BRKIN0, HRTIMER_FLT2, TRIGSEL_OUT2, EVENTOUT Additional: CMP4_IM
VSS	23	P	-	Default: VSS
VDD	24	P	-	Default: VDD
PB11	25	I/O		Default: PB11 Alternate: TIMER1_CH3, HPDF_DATAIN3, HPDF_CKIN7, USART2_RX, QSPI_CSN(4), HRTIMER_FLT3, EVENTOUT Additional: ADC01_IN13, CMP5_IP
PB12	26	I/O		Default: PB12 Alternate: TIMER4_ETI, I2C1_SMBA, SPI1_NSS, TIMER0_BRKIN0, USART2_CK, CAN1_RX, HPDF_DATAIN1, HRTIMER_ST2CH0, EVENTOUT Additional: ADC3_IN2, ADC0_IN10, CMP6_IM
PB13	27	I/O		Default: PB13 Alternate: SPI1_SCK, TIMER0_MCH0, USART2_CTS, CAN1_TX, HPDF_CKIN1, HRTIMER_ST2CH1, EVENTOUT Additional: ADC2_IN4, CMP4_IP
PB14	28	I/O		Default: PB14 Alternate: TIMER14_CH0, SPI1_MISO, TIMER0_MCH1, USART2_RTS, USART2_DE, CMP3_OUT, HPDF_DATAIN2, HRTIMER_ST3CH0, TRIGSEL_OUT1, EVENTOUT Additional: ADC3_IN3, ADC0_IN4, CMP6_IP
PB15	29	I/O		Default: PB15 Alternate: RTC_REFIN, TIMER14_CH1, TIMER14_MCH0, CMP2_OUT, TIMER0_MCH2, SPI1_MOSI, HPDF_CKIN2, HRTIMER_ST3CH1, TRIGSEL_OUT5, EVENTOUT Additional: ADC3_IN4, ADC1_IN14, CMP5_IM
PA8	30	I/O	5VT	Default: PA8 Alternate: CK_OUT, I2C2_SCL, I2C1_SDA, TIMER0_CH0, USART0_CK, CMP6_OUT, TIMER3_ETI, CAN2_RX, SPI1_NSS, HRTIMER_ST0CH0, UART4_RX, EVENTOUT Additional: ADC3_IN16, NMI, CLAIN11
PA9	31	I/O	5VT	Default: PA9 Alternate: I2C2_SMBA, I2C1_SCL, TIMER0_CH1,

GD32G553CxTx LQFP48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				USART0_TX, CMP4_OUT, TIMER14_BRKIN0, TIMER1_CH2, SPI1_SCK, HRTIMER_ST0CH1, TRIGSEL_IN13, EVENTOUT Additional: ADC3_IN17, CLAIN12
PA10	32	I/O	5VT	Default: PA10 Alternate: TIMER16_BRKIN0, CLA2OUT, I2C1_SMBA, SPI1_MISO, TIMER0_CH2, USART0_RX, CMP5_OUT, TIMER1_CH3, TIMER7_BRKIN0, HRTIMER_ST1CH0, TRIGSEL_IN12, EVENTOUT Additional: CLAIN13, LVD_IN
PA11	33	I/O	5VT	Default: PA11 Alternate: CLA3OUT, SPI1_MOSI, TIMER0_MCH0, USART0_CTS, CMP0_OUT, CAN0_RX, TIMER3_CH0, TIMER0_CH3, TIMER0_BRKIN2, HRTIMER_ST1CH1, TRIGSEL_IN13, EVENTOUT Additional: CLAIN14
PA12	34	I/O	5VT	Default: PA12 Alternate: TIMER15_CH0, TIMER0_MCH1, USART0_RTS, USART0_DE, CMP1_OUT, CAN0_TX, TIMER3_CH1, TIMER0_ETI, HRTIMER_FLT0, TRIGSEL_IN12, EVENTOUT Additional: CLAIN15
VSS	35	P	-	Default: VSS
VDD	36	P	-	Default: VDD
PA13	37	I/O	5VT	Default: JTMS, SWDIO, PA13 Alternate: TIMER15_MCH0, TIMER0_BRKIN1, I2C3_SCL, I2C0_SCL, IFRP_OUT, TIMER7_BRKIN1, USART2_CTS, TIMER3_CH2, TRIGSEL_IN10, EVENTOUT
PA14	38	I/O	5VT	Default: JTCK, SWCLK, PA14 Alternate: LPTIMER_OUT, I2C3_SMBA, I2C0_SDA, TIMER7_CH1, TIMER0_BRKIN0, USART1_TX, TRIGSEL_IN11, EVENTOUT
PA15	39	I/O	5VT	Default: JTDI, PA15 Alternate: TIMER1_CH0, TIMER7_CH0, CLA3OUT, I2C0_SCL, SPI0_NSS, SPI2_NSS, USART1_RX, UART3_RTS, UART3_DE, TIMER0_BRKIN0, CAN2_TX, TRIGSEL_OUT0, HRTIMER_FLT1, TIMER1_ETI, EVENTOUT Additional: CLAIN0
PB3	40	I/O	5VT	Default: JTDO, PB3 Alternate: TIMER1_CH1, TIMER3_ETI, CLA0OUT, TIMER7_MCH0, SPI0_SCK, SPI2_SCK, USART1_TX, HRTIMER_ST5CH1, TIMER2_ETI, CAN2_RX, HRTIMER_SCOUT, HRTIMER_EXEV8,

GD32G553CxTx LQFP48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				TRIGSEL_OUT7, EVENTOUT Additional: CLAIN1
PB4	41	I/O	5VT	Default: NJTRST, PB4 Alternate: TIMER15_CH0, TIMER2_CH0, CLA1OUT, TIMER7_MCH1, SPI0_MISO, SPI2_MISO, USART1_RX, UART4_RTS, UART4_DE, TIMER16_BRKIN0, CAN2_TX, HRTIMER_EXEV6, TRIGSEL_OUT6, EVENTOUT Additional: CLAIN2
PB5	42	I/O	5VT	Default: PB5 Alternate: HPDF_CKIN0, TIMER15_BRKIN0, TIMER2_CH1, TIMER7_MCH2, I2C0_SMBA, SPI0_MOSI, SPI2_MOSI, USART1_CK, I2C2_SDA, CAN1_RX, TIMER16_CH0, LPTIMER_IN0, CLA2OUT, HRTIMER_EXEV5, UART4_CTS, EVENTOUT Additional: CLAIN3
PB6	43	I/O	5VT	Default: PB6 Alternate: HPDF_DATAIN5, TIMER15_MCH0, TIMER3_CH0, I2C0_SCL, TIMER7_CH0, TIMER7_ETI, USART0_TX, CMP3_OUT, CAN1_TX, TIMER7_BRKIN2, LPTIMER_ETI0, HRTIMER_SCIN, HRTIMER_EXEV3, EVENTOUT Additional: CLAIN4
PB7	44	I/O	5VT	Default: PB7 Alternate: HPDF_CKIN5, TIMER16_MCH0, TIMER3_CH1, I2C3_SDA, I2C0_SDA, TIMER7_BRKIN0, USART0_RX, CMP2_OUT, TIMER2_CH3, LPTIMER_IN1, HRTIMER_EXEV2, UART3_CTS, QSPI_DQS(3)(4)(6), HRTIMER_ST5CH1, EVENTOUT Additional: CLAIN5
PB8/BOOT0	45	I/O	5VT	Default: BOOT0, PB8 Alternate: TIMER15_CH0, TIMER3_CH2, HPDF_CKIN7, I2C0_SCL, CLA3OUT, USART2_RX, CMP0_OUT, CAN0_RX, TIMER7_CH1, TIMER0_BRKIN0, HRTIMER_EXEV7, EVENTOUT Additional: CLAIN6
PB9	46	I/O	5VT	Default: PB9 Alternate: TIMER16_CH0, TIMER3_CH3, HPDF_DATAIN7, I2C0_SDA, IFRP_OUT, USART2_TX, CMP1_OUT, CAN0_TX, TIMER7_CH2, TIMER0_MCH2, HRTIMER_EXEV4, EVENTOUT Additional: CLAIN7
VSS	47	P	-	Default: VSS

GD32G553CxTx LQFP48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
VDD	48	P	-	Default: VDD

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) These QSPI pin functions are highly recommended to be used together, and the supported maximum communication clock is 120MHz for this group. Otherwise the QSPI maximum clock frequency cannot be guaranteed.

(4) These QSPI pin functions are highly recommended to be used together, and the supported maximum communication clock is 120MHz for this group. Otherwise the QSPI maximum clock frequency cannot be guaranteed.

(5) These QSPI pin functions are highly recommended to be used together, and the supported maximum communication clock is 200MHz for this group. Otherwise the QSPI maximum clock frequency cannot be guaranteed.

(6) These QSPI pin functions are highly recommended to be used together, and the supported maximum communication clock is 120MHz for this group. Otherwise the QSPI maximum clock frequency cannot be guaranteed.

(7) Refer to the description of the NRST_MDSEL bit field of OB_USER option byte in the GD32G5x3 User Manual to configure the NRST-PG10 pin as a PG10 general GPIO function.

2.6.7. GD32G553CxUx QFN48 pin definitions

Table 2-9. GD32G553CxUx QFN48 pin definitions

GD32G553CxUx QFN48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
VBAT	1	P	-	Default: VBAT
PC13	2	I/O	5VT	Default: PC13 Alternate: TIMER0_BRKIN0, TIMER0_MCH0, TIMER7_MCH3, EVENTOUT Additional: WKUP1, RTC_TAMP0, RTC_TS, RTC_OUT0
PC14-OSC32IN	3	I/O	5VT	Default: PC14 Alternate: EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	4	I/O	5VT	Default: PC15 Alternate: EVENTOUT Additional: OSC32OUT
OSCIN-PF0	5	I/O	5VT	Default: OSCIN, PF0 Alternate: I2C1_SDA, SPI1_NSS, TIMER0_MCH2, EVENTOUT Additional: ADC0_IN9, OSCIN, CLAIN16
OSCOUT-PF1	6	I/O	5VT	Default: OSCOUT, PF1 Alternate: TIMER19_BRKIN1, SPI1_SCK, EVENTOUT Additional: ADC1_IN9, CMP2_IM, OSCOUT, CLAIN17
NRST-PG10	7	I/O	5VT	Default: NRST Alternate: CK_OUT, EVENTOUT Additional: PG10(7)
PA0	8	I/O		Default: PA0 Alternate: TIMER1_CH0, TIMER4_CH0, UART3_TX, USART1_CTS, CMP0_OUT, TIMER7_BRKIN0, TIMER7_ETI, HRTIMER_ST6CH0, TRIGSEL_IN0, TIMER1_ETI, EVENTOUT Additional: ADC01_IN0, RTC_TAMP1, CMP0_IM, CMP2_IP, WKUP0, CLAIN18
PA1	9	I/O		Default: PA1 Alternate: RTC_REFIN, TIMER1_CH1, TIMER4_CH1, UART3_RX, USART1_RTS, USART1_DE, TIMER14_MCH0, HRTIMER_ST6CH1, TRIGSEL_IN1, EVENTOUT Additional: ADC01_IN1, CMP0_IP, CLAIN19
PA2	10	I/O	5VT	Default: PA2 Alternate: TIMER1_CH2, TIMER4_CH2, CLA0OUT, USART1_TX, CMP1_OUT, TIMER14_CH0, QSPI_CSN(3)(6), HRTIMER_ST7CH0, TRIGSEL_IN7, CK_HPDFAUDIO, EVENTOUT Additional: ADC0_IN2, CMP1_IM, WKUP3, LSCK_OUT

GD32G553CxUx QFN48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PA3	11	I/O		Default: PA3 Alternate: TIMER1_CH3, TIMER4_CH3, USART1_RX, TIMER14_CH1, QSPI_SCK(3), HRTIMER_ST7CH1, TRIGSEL_IN4, EVENTOUT Additional: ADC0_IN3, CMP1_IP
PA4	12	I/O		Default: PA4 Alternate: TIMER2_CH1, SPI0_NSS, SPI2_NSS, USART1_CK, HRTIMER_ST2CH0, EVENTOUT Additional: ADC1_IN15, DAC0_OUT0, CMP0_IM
PA5	13	I/O		Default: PA5 Alternate: TIMER1_CH0, TIMER1_ETI, SPI0_SCK, USART2_TX, HRTIMER_ST2CH1, EVENTOUT Additional: ADC1_IN12, DAC0_OUT1, CMP1_IM
PA6	14	I/O		Default: PA6 Alternate: TIMER15_CH0, TIMER2_CH0, TIMER7_BRKIN0, SPI0_MISO, USART2_RX, TIMER0_BRKIN0, CMP0_OUT, QSPI_IO3(3), HRTIMER_ST3CH0, CK_HPDFAUDIO, EVENTOUT Additional: ADC1_IN2, DAC1_OUT0
PA7	15	I/O		Default: PA7 Alternate: TIMER16_CH0, TIMER2_CH1, CLA1OUT, TIMER7_MCH0, SPI0_MOSI, TIMER0_MCH0, CMP1_OUT, QSPI_IO2(3), HRTIMER_ST3CH1, TRIGSEL_IN5, UART4_TX, EVENTOUT Additional: ADC1_IN3, CMP1_IP, DAC1_OUT1
PC4	16	I/O	5VT	Default: PC4 Alternate: TIMER0_ETI, I2C1_SCL, USART0_TX, HPDF_CKIN2, QSPI_IO3(3), HRTIMER_FLT7, EVENTOUT Additional: ADC1_IN4
PB0	17	I/O		Default: PB0 Alternate: TIMER2_CH2, CLA1OUT, TIMER7_MCH1, HPDF_CKOUT, TIMER0_MCH1, HRTIMER_ST4CH0, QSPI_IO1(3), TRIGSEL_OUT3, HRTIMER_FLT4, EVENTOUT Additional: ADC2_IN11, ADC0_IN12, CMP3_IP, CLAIN8
PB1	18	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER7_MCH2, HPDF_DATAIN1, TIMER0_MCH2, TIMER19_MCH0, CMP3_OUT, HRTIMER_ST4CH1, QSPI_IO0(3), TRIGSEL_OUT4, HRTIMER_SCOUT, EVENTOUT Additional: ADC2_IN0, ADC0_IN11, CMP0_IP, CLAIN9
PB2	19	I/O		Default: PB2 Alternate: RTC_OUT1, LPTIMER_OUT, TIMER4_CH0, TIMER19_CH0, I2C2_SMBA, HPDF_CKIN1,

GD32G553CxUx QFN48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				HRTIMER_ST5CH0, QSPI_IO1(3), HRTIMER_SCIN, EVENTOUT Additional: ADC1_IN11, CMP3_IM, CLAIN10
VREFP	20	P	-	Default: VREFP
VDDA	21	P	-	Default: VDDA
PB10	22	I/O		Default: PB10 Alternate: TIMER1_CH2, HPDF_DATAIN0, HPDF_DATAIN7, USART2_TX, QSPI_SCK(4), TIMER0_BRKIN0, HRTIMER_FLT2, TRIGSEL_OUT2, EVENTOUT Additional: CMP4_IM
VDD	23	P	-	Default: VDD
PB11	24	I/O		Default: PB11 Alternate: TIMER1_CH3, HPDF_DATAIN3, HPDF_CKIN7, USART2_RX, QSPI_CSN(4), HRTIMER_FLT3, EVENTOUT Additional: ADC01_IN13, CMP5_IP
PB12	25	I/O		Default: PB12 Alternate: TIMER4_ETI, I2C1_SMBA, SPI1_NSS, TIMER0_BRKIN0, USART2_CK, CAN1_RX, HPDF_DATAIN1, HRTIMER_ST2CH0, EVENTOUT Additional: ADC3_IN2, ADC0_IN10, CMP6_IM
PB13	26	I/O		Default: PB13 Alternate: SPI1_SCK, TIMER0_MCH0, USART2_CTS, CAN1_TX, HPDF_CKIN1, HRTIMER_ST2CH1, EVENTOUT Additional: ADC2_IN4, CMP4_IP
PB14	27	I/O		Default: PB14 Alternate: TIMER14_CH0, SPI1_MISO, TIMER0_MCH1, USART2_RTS, USART2_DE, CMP3_OUT, HPDF_DATAIN2, HRTIMER_ST3CH0, TRIGSEL_OUT1, EVENTOUT Additional: ADC3_IN3, ADC0_IN4, CMP6_IP
PB15	28	I/O		Default: PB15 Alternate: RTC_REFIN, TIMER14_CH1, TIMER14_MCH0, CMP2_OUT, TIMER0_MCH2, SPI1_MOSI, HPDF_CKIN2, HRTIMER_ST3CH1, TRIGSEL_OUT5, EVENTOUT Additional: ADC3_IN4, ADC1_IN14, CMP5_IM
PC6	29	I/O	5VT	Default: PC6 Alternate: HPDF_CKIN3, TIMER0_BRKIN1, CMP5_OUT, TIMER2_CH0, HRTIMER_EXEV9, TIMER7_CH0, I2C3_SCL, HRTIMER_ST5CH0, EVENTOUT
PA8	30	I/O	5VT	Default: PA8

GD32G553CxUx QFN48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: CK_OUT, I2C2_SCL, I2C1_SDA, TIMER0_CH0, USART0_CK, CMP6_OUT, TIMER3_ETI, CAN2_RX, SPI1_NSS, HRTIMER_ST0CH0, UART4_RX, EVENTOUT Additional: ADC3_IN16, NMI, CLAIN11
PA9	31	I/O	5VT	Default: PA9 Alternate: I2C2_SMBA, I2C1_SCL, TIMER0_CH1, USART0_TX, CMP4_OUT, TIMER14_BRKIN0, TIMER1_CH2, SPI1_SCK, HRTIMER_ST0CH1, TRIGSEL_IN13, EVENTOUT Additional: ADC3_IN17, CLAIN12
PA10	32	I/O	5VT	Default: PA10 Alternate: TIMER16_BRKIN0, CLA2OUT, I2C1_SMBA, SPI1_MISO, TIMER0_CH2, USART0_RX, CMP5_OUT, TIMER1_CH3, TIMER7_BRKIN0, HRTIMER_ST1CH0, TRIGSEL_IN12, EVENTOUT Additional: CLAIN13, LVD_IN
PA11	33	I/O	5VT	Default: PA11 Alternate: CLA3OUT, SPI1_MOSI, TIMER0_MCH0, USART0_CTS, CMP0_OUT, CAN0_RX, TIMER3_CH0, TIMER0_CH3, TIMER0_BRKIN2, HRTIMER_ST1CH1, TRIGSEL_IN13, EVENTOUT Additional: CLAIN14
PA12	34	I/O	5VT	Default: PA12 Alternate: TIMER15_CH0, TIMER0_MCH1, USART0_RTS, USART0_DE, CMP1_OUT, CAN0_TX, TIMER3_CH1, TIMER0_ETI, HRTIMER_FLT0, TRIGSEL_IN12, EVENTOUT Additional: CLAIN15
VDD	35	P	-	Default: VDD
PA13	36	I/O	5VT	Default: JTMS, SWDIO, PA13 Alternate: TIMER15_MCH0, TIMER0_BRKIN1, I2C3_SCL, I2C0_SCL, IFRP_OUT, TIMER7_BRKIN1, USART2_CTS, TIMER3_CH2, TRIGSEL_IN10, EVENTOUT
PA14	37	I/O	5VT	Default: JTCK, SWCLK, PA14 Alternate: LPTIMER_OUT, I2C3_SMBA, I2C0_SDA, TIMER7_CH1, TIMER0_BRKIN0, USART1_TX, TRIGSEL_IN11, EVENTOUT
PA15	38	I/O	5VT	Default: JTDI, PA15 Alternate: TIMER1_CH0, TIMER7_CH0, CLA3OUT, I2C0_SCL, SPI0_NSS, SPI2_NSS, USART1_RX, UART3_RTS, UART3_DE, TIMER0_BRKIN0, CAN2_TX, TRIGSEL_OUT0, HRTIMER_FLT1, TIMER1_ETI, EVENTOUT Additional: CLAIN0

GD32G553CxUx QFN48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PC10	39	I/O	5VT	Default: PC10 Alternate: HPDF_CKIN5, TIMER7_MCH0, UART3_TX, SPI2_SCK, USART2_TX, HRTIMER_FLT5, EVENTOUT
PC11	40	I/O	5VT	Default: PC11 Alternate: HPDF_DATAIN5, HRTIMER_EXEV1, TIMER7_MCH1, UART3_RX, SPI2_MISO, USART2_RX, I2C2_SDA, EVENTOUT
PB3	41	I/O	5VT	Default: JTDO, PB3 Alternate: TIMER1_CH1, TIMER3_ETI, CLA0OUT, TIMER7_MCH0, SPI0_SCK, SPI2_SCK, USART1_TX, HRTIMER_ST5CH1, TIMER2_ETI, CAN2_RX, HRTIMER_SCOUT, HRTIMER_EXEV8, TRIGSEL_OUT7, EVENTOUT Additional: CLAIN1
PB4	42	I/O	5VT	Default: NJTRST, PB4 Alternate: TIMER15_CH0, TIMER2_CH0, CLA1OUT, TIMER7_MCH1, SPI0_MISO, SPI2_MISO, USART1_RX, UART4_RTS, UART4_DE, TIMER16_BRKIN0, CAN2_TX, HRTIMER_EXEV6, TRIGSEL_OUT6, EVENTOUT Additional: CLAIN2
PB5	43	I/O	5VT	Default: PB5 Alternate: HPDF_CKIN0, TIMER15_BRKIN0, TIMER2_CH1, TIMER7_MCH2, I2C0_SMBA, SPI0_MOSI, SPI2_MOSI, USART1_CK, I2C2_SDA, CAN1_RX, TIMER16_CH0, LPTIMER_IN0, CLA2OUT, HRTIMER_EXEV5, UART4_CTS, EVENTOUT Additional: CLAIN3
PB6	44	I/O	5VT	Default: PB6 Alternate: HPDF_DATAIN5, TIMER15_MCH0, TIMER3_CH0, I2C0_SCL, TIMER7_CH0, TIMER7_ETI, USART0_TX, CMP3_OUT, CAN1_TX, TIMER7_BRKIN2, LPTIMER_ETI0, HRTIMER_SCIN, HRTIMER_EXEV3, EVENTOUT Additional: CLAIN4
PB7	45	I/O	5VT	Default: PB7 Alternate: HPDF_CKIN5, TIMER16_MCH0, TIMER3_CH1, I2C3_SDA, I2C0_SDA, TIMER7_BRKIN0, USART0_RX, CMP2_OUT, TIMER2_CH3, LPTIMER_IN1, HRTIMER_EXEV2, UART3_CTS, QSPI_DQS(3)(4)(6), HRTIMER_ST5CH1, EVENTOUT Additional: CLAIN5
PB8/BOOT0	46	I/O	5VT	Default: BOOT0, PB8

GD32G553CxUx QFN48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: TIMER15_CH0, TIMER3_CH2, HPDF_CKIN7, I2C0_SCL, CLA3OUT, USART2_RX, CMP0_OUT, CAN0_RX, TIMER7_CH1, TIMER0_BRKIN0, HRTIMER_EXEV7, EVENTOUT Additional: CLAIN6
PB9	47	I/O	5VT	Default: PB9 Alternate: TIMER16_CH0, TIMER3_CH3, HPDF_DATAIN7, I2C0_SDA, IFRP_OUT, USART2_TX, CMP1_OUT, CAN0_TX, TIMER7_CH2, TIMER0_MCH2, HRTIMER_EXEV4, EVENTOUT Additional: CLAIN7
VDD	48	P	-	Default: VDD

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) These QSPI pin functions are highly recommended to be used together, and the supported maximum communication clock is 120MHz for this group. Otherwise the QSPI maximum clock frequency cannot be guaranteed.

(4) These QSPI pin functions are highly recommended to be used together, and the supported maximum communication clock is 120MHz for this group. Otherwise the QSPI maximum clock frequency cannot be guaranteed.

(5) These QSPI pin functions are highly recommended to be used together, and the supported maximum communication clock is 200MHz for this group. Otherwise the QSPI maximum clock frequency cannot be guaranteed.

(6) These QSPI pin functions are highly recommended to be used together, and the supported maximum communication clock is 120MHz for this group. Otherwise the QSPI maximum clock frequency cannot be guaranteed.

(7) Refer to the description of the NRST_MDSEL bit field of OB_USER option byte in the GD32G5x3 User Manual to configure the NRST-PG10 pin as a PG10 general GPIO function.

2.6.8. GD32G553xx pin alternate functions

Table 2-10. Port A alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0		TIMER1_CH0	TIMER4_CH0				UART3_TX	USART1_CTS	CMP0_OUT	TIMER7_BRKIN0	TIMER7_ETI	EXMC_A13(1)	HRTIMER_ST6CH0	TRIGSEL_IN0	TIMER1_ETI	EVENTOUT
PA1	RTC_REFIN	TIMER1_CH1	TIMER4_CH1				UART3_RX	USART1_RTS/USART1_DE		TIMER14_MCH0		EXMC_A14(1)	HRTIMER_ST6CH1	TRIGSEL_IN1		EVENTOUT
PA2		TIMER1_CH2	TIMER4_CH2	CLA0OUT				USART1_TX	CMP1_OUT	TIMER14_CH0	QSPI_CSN(5)(8)	EXMC_A15(1)	HRTIMER_ST7CH0	TRIGSEL_IN7	CK_HPDFAUDIO	EVENTOUT
PA3		TIMER1_CH3	TIMER4_CH3					USART1_RX		TIMER14_CH1	QSPI_SCK(5)	EXMC_A16(1)	HRTIMER_ST7CH1	TRIGSEL_IN4		EVENTOUT
PA4			TIMER2_CH1			SPI0_NSS	SPI2_NSS	USART1_CK				EXMC_A17(1)	HRTIMER_ST2CH0			EVENTOUT
PA5		TIMER1_CH0	TIMER1_ETI			SPI0_SCK		USART2_TX				EXMC_A18(1)	HRTIMER_ST2CH1			EVENTOUT
PA6		TIMER15_CH0	TIMER2_CH0		TIMER7_BRKIN0	SPI0_MISO	TIMER0_BRKIN0	USART2_RX	CMP0_OUT		QSPI_IO3(5)	EXMC_A19(1)	HRTIMER_ST3CH0		CK_HPDFAUDIO	EVENTOUT
PA7		TIMER16_CH0	TIMER2_CH1	CLA1OUT	TIMER7_MCH0	SPI0_MOSI	TIMER0_MCH0		CMP1_OUT		QSPI_IO2(5)	EXMC_A20(1)	HRTIMER_ST3CH1	TRIGSEL_IN5	UART4_TX	EVENTOUT
PA8	CK_OUT		I2C2_SCL		I2C1_SDA		TIMER0_CH0	USART0_CK	CMP6_OUT	EXMC_A21(1)	TIMER3_ETI	CAN2_RX	SPI1_NSS	HRTIMER_ST0CH0	UART4_RX	EVENTOUT
PA9			I2C2_SMBA		I2C1_SCL		TIMER0_CH1	USART0_TX	CMP4_OUT	TIMER14_BRKIN0	TIMER1_CH2	EXMC_A22(1)	SPI1_SCK	HRTIMER_ST0CH1	TRIGSEL_IN13	EVENTOUT
PA10		TIMER16_BRKIN0		CLA2OUT	I2C1_SMBA	SPI1_MISO	TIMER0_CH2	USART0_RX	CMP5_OUT	EXMC_A23(1)	TIMER1_CH3	TIMER7_BRKIN0		HRTIMER_ST1CH0	TRIGSEL_IN12	EVENTOUT
PA11				CLA3OUT	EXMC_A24(1)	SPI1_MOSI	TIMER0_MCH0	USART0_CTS	CMP0_OUT	CAN0_RX	TIMER3_CH0	TIMER0_CH3	TIMER0_BRKIN2	HRTIMER_ST1CH1	TRIGSEL_IN13	EVENTOUT
PA12		TIMER15_CH0			EXMC_A25(1)		TIMER0_MCH1	USART0_RTS/USART0_DE	CMP1_OUT	CAN0_TX	TIMER3_CH1	TIMER0_ETI		HRTIMER_FLT0	TRIGSEL_IN12	EVENTOUT
PA13	JTMS/SWDIO	TIMER15_MCH0	TIMER0_BRKIN1	I2C3_SCL	I2C0_SCL	IFRP_OUT	TIMER7_BRKIN1	USART2_CTS	CMP7_OUT	EXMC_A5(1)	TIMER3_CH2			TRIGSEL_IN10		EVENTOUT
PA14	JTCK/SWCLK	LPTIMER_OUT		I2C3_SMBA	I2C0_SDA	TIMER7_CH1	TIMER0_BRKIN0	USART1_TX	CMP7_OUT					TRIGSEL_IN11		EVENTOUT
PA15	JTDI	TIMER1_CH0	TIMER7_CH0	CLA3OUT	I2C0_SCL	SPI0_NSS	SPI2_NSS	USART1_RX	UART3_RTS/UART3_DE	TIMER0_BRKIN0		CAN2_TX	TRIGSEL_OUT0	HRTIMER_FLT1	TIMER1_ETI	EVENTOUT

Table 2-11. Port B alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB0			TIMER2_CH2	CLA1OUT	TIMER7_MCH1	HPDF_CKOUT	TIMER0_MCH1			HRTIMER_ST4CH0	QSPI_IO1[5]	EXMC_A1[1]	TRIGSEL_OUT3	HRTIMER_FLT4		EVENTOUT
PB1			TIMER2_CH3		TIMER7_MCH2	HPDF_DATAIN1	TIMER0_MCH2	TIMER19_MCH0	CMP3_OUT	HRTIMER_ST4CH1	QSPI_IO0[5]	EXMC_A2[1]	TRIGSEL_OUT4	HRTIMER_SCOUT		EVENTOUT
PB2	RTC_OUT1	LPTIMER_OUT	TIMER4_CH0	TIMER19_CH0	I2C2_SMBA	HPDF_CKIN1				HRTIMER_ST5CH0	QSPI_IO1[5]	EXMC_A3[1]		HRTIMER_SCIN		EVENTOUT
PB3	JTDO	TIMER1_CH1	TIMER3_ETI	CLA0OUT	TIMER7_MCH0	SPI0_SCK	SPI2_SCK	USART1_TX		HRTIMER_ST5CH1	TIMER2_ETI	CAN2_RX	HRTIMER_SCOUT	HRTIMER_EXEV8	TRIGSEL_OUT7	EVENTOUT
PB4	NJTRST	TIMER15_CH0	TIMER2_CH0	CLA1OUT	TIMER7_MCH1	SPI0_MISO	SPI2_MISO	USART1_RX	UART4_RTS/UART4_DE		TIMER16_BRKIN0	CAN2_TX		HRTIMER_EXEV6	TRIGSEL_OUT6	EVENTOUT
PB5	HPDF_CKIN0	TIMER15_BRKIN0	TIMER2_CH1	TIMER7_MCH2	I2C0_SMBA	SPI0_MOSI	SPI2_MOSI	USART1_CK	I2C2_SDA	CAN1_RX	TIMER16_CH0	LPTIMER_IN0	CLA2OUT	HRTIMER_EXEV5	UART4_CTS	EVENTOUT
PB6	HPDF_DATAIN5	TIMER15_MCH0	TIMER3_CH0		I2C0_SCL	TIMER7_CH0	TIMER7_ETI	USART0_TX	CMP3_OUT	CAN1_TX	TIMER7_BRKIN2	LPTIMER_ETI0	HRTIMER_SCIN	HRTIMER_EXEV3	EXMC_A4[1]	EVENTOUT
PB7	HPDF_CKIN5	TIMER16_MCH0	TIMER3_CH1	I2C3_SDA	I2C0_SDA	TIMER7_BRKIN0	HRTIMER_ST5CH1	USART0_RX	CMP2_OUT	QSPI_DQS[5][6][8]	TIMER2_CH3	LPTIMER_IN1	EXMC_NL/EXMC_NADV[1]	HRTIMER_EXEV2	UART3_CTS	EVENTOUT
PB8		TIMER15_CH0	TIMER3_CH2	HPDF_CKIN7	I2C0_SCL	CLA3OUT		USART2_RX	CMP0_OUT	CAN0_RX	TIMER7_CH1		TIMER0_BRKIN0	HRTIMER_EXEV7		EVENTOUT
PB9		TIMER16_CH0	TIMER3_CH3	HPDF_DATAIN7	I2C0_SDA		IFRP_OUT	USART2_TX	CMP1_OUT	CAN0_TX	TIMER7_CH2	EXMC_A6[1]	TIMER0_MCH2	HRTIMER_EXEV4		EVENTOUT
PB10		TIMER1_CH2		HPDF_DATAIN0			HPDF_DATAIN7	USART2_TX			QSPI_SCK[6]	EXMC_A7[1]	TIMER0_BRKIN0	HRTIMER_FLT2	TRIGSEL_OUT2	EVENTOUT
PB11		TIMER1_CH3		HPDF_DATAIN3			HPDF_CKIN7	USART2_RX			QSPI_CSN[6]	EXMC_A8[1]		HRTIMER_FLT3		EVENTOUT
PB12			TIMER4_ETI		I2C1_SMBA	SPI1_NSS	TIMER0_BRKIN0	USART2_CK		CAN1_RX	HPDF_DATAIN1	EXMC_A9[1]		HRTIMER_ST2CH0		EVENTOUT
PB13						SPI1_SCK	TIMER0_MCH0	USART2_CTS		CAN1_TX	HPDF_CKIN1	EXMC_A10[1]		HRTIMER_ST2CH1		EVENTOUT
PB14		TIMER14_CH0				SPI1_MISO	TIMER0_MCH1	USART2_RTS/USART2_DE	CMP3_OUT		HPDF_DATAIN2	EXMC_A11[1]		HRTIMER_ST3CH0	TRIGSEL_OUT1	EVENTOUT
PB15	RTC_REFIN	TIMER14_CH1	TIMER14_MCH0	CMP2_OUT	TIMER0_MCH2	SPI1_MOSI					HPDF_CKIN2	EXMC_A12[1]		HRTIMER_ST3CH1	TRIGSEL_OUT5	EVENTOUT

Table 2-12. Port C alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC0		LPTIMER_IN0	TIMER0_CH0						HPDF_CKIN0		HPDF_DATAIN4		EXMC_CLK(1)	TRIGSEL_IN8	USART0_RX	EVENTOUT
PC1		LPTIMER_OUT	TIMER0_CH1		HPDF_CKIN4				HPDF_DATAIN0		QSPI_IO0(8)		EXMC_NOE(1)	TRIGSEL_IN9	USART0_TX	EVENTOUT
PC2	HPDF_CKOUT	LPTIMER_IN1	TIMER0_CH2	CMP2_OUT			TIMER19_CH1		HPDF_CKIN1		QSPI_IO1(8)		EXMC_NWE(1)	TRIGSEL_IN2		EVENTOUT
PC3		LPTIMER_ETI0	TIMER0_CH3				TIMER0_BRKIN2		HPDF_DATAIN1		QSPI_IO2(8)		EXMC_NWAIT(1)	HRTIMER_FLT6		EVENTOUT
PC4			TIMER0_ETI		I2C1_SCL			USART0_TX	HPDF_CKIN2		QSPI_IO3(5)		EXMC_NE0(1)	HRTIMER_FLT7		EVENTOUT
PC5			TIMER14_BRKIN0				TIMER0_MCH3	USART0_RX	HPDF_DATAIN2				EXMC_NE1(1)	HRTIMER_EXEV9		EVENTOUT
PC6	HPDF_CKIN3	TIMER0_BRKIN1	TIMER2_CH0	HRTIMER_EXEV9	TIMER7_CH0			CMP5_OUT	I2C3_SCL				EXMC_NE2(1)	HRTIMER_ST5CH0		EVENTOUT
PC7	HPDF_DATAIN3		TIMER2_CH1	HRTIMER_FLT4	TIMER7_CH1			CMP4_OUT	I2C3_SDA				EXMC_NE3(1)	HRTIMER_ST5CH1		EVENTOUT
PC8			TIMER2_CH2	HRTIMER_ST4CH0	TIMER7_CH2		TIMER19_CH2	CMP6_OUT	I2C2_SCL				EXMC_NBL0(1)			EVENTOUT
PC9			TIMER2_CH3	HRTIMER_ST4CH1	TIMER7_CH3		TIMER7_BRKIN2		I2C2_SDA				EXMC_NBL1(1)			EVENTOUT
PC10	HPDF_CKIN5				TIMER7_MCH0	UART3_TX	SPI2_SCK	USART2_TX					EXMC_D0(1)	HRTIMER_FLT5		EVENTOUT
PC11	HPDF_DATAIN5			HRTIMER_EXEV1	TIMER7_MCH1	UART3_RX	SPI2_MISO	USART2_RX	I2C2_SDA				EXMC_D1(1)			EVENTOUT
PC12		TIMER4_CH1		HRTIMER_EXEV0	TIMER7_MCH2	UART4_TX	SPI2_MOSI	USART2_CK					EXMC_A0(1)			EVENTOUT
PC13			TIMER0_BRKIN0		TIMER0_MCH0		TIMER7_MCH3									EVENTOUT
PC14																EVENTOUT
PC15																EVENTOUT

Table 2-13. Port D alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PD0				HPDF_CKIN6			TIMER7_MCH3			CAN0_RX			EXMC_D2(2)	TRIGSEL_IN3		EVENTOUT
PD1				HPDF_DATAIN6	TIMER7_CH3		TIMER7_BRKIN2			CAN0_TX	QSPI_DQS(7)		EXMC_D3(2)	TRIGSEL_IN6		EVENTOUT
PD2			TIMER2_ETI		TIMER7_BRKIN0	UART4_RX					QSPI_SCK(7)					EVENTOUT
PD3			TIMER1_CH0/TIMER1_ETI	HPDF_CKOUT				USART1_CTS			QSPI_CSN(7)		EXMC_CLK(2)			EVENTOUT
PD4			TIMER1_CH1					USART1_RTS/USART1_DE			QSPI_IO0(7)		EXMC_NOE(2)			EVENTOUT
PD5								USART1_TX			QSPI_IO1		EXMC_NWE(2)			EVENTOUT
PD6			TIMER1_CH3	HPDF_CKIN4	HPDF_DATAIN1			USART1_RX			QSPI_IO2(7)		EXMC_NWAIT(2)			EVENTOUT
PD7			TIMER1_CH2	HPDF_DATAIN4			HPDF_CKIN1	USART1_CK			QSPI_IO3(7)		EXMC_NE0(2)			EVENTOUT
PD8				HPDF_CKIN3				USART2_TX					EXMC_D13(1)			EVENTOUT
PD9				HPDF_DATAIN3				USART2_RX					EXMC_D14(1)			EVENTOUT
PD10				HPDF_CKOUT				USART2_CK					EXMC_D15(1)			EVENTOUT
PD11		TIMER4_ETI			I2C3_SMBA			USART2_CTS					EXMC_A16(3)			EVENTOUT
PD12			TIMER3_CH0					USART2_RTS/USART2_DE					EXMC_A17(2)			EVENTOUT
PD13			TIMER3_CH1										EXMC_A18(2)			EVENTOUT
PD14			TIMER3_CH2			SPI0_IO2							EXMC_D0(2)			EVENTOUT
PD15			TIMER3_CH3			SPI0_IO3	SPI1_NSS						EXMC_D1(2)			EVENTOUT

Table 2-14. Port E alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PE0			TIMER3_ETI	TIMER19_MCH3	TIMER15_CH0		TIMER19_ETI	USART0_TX					EXMC_NBL0(2)	HRTIMER_ST6CH0		EVENTOUT
PE1					TIMER16_CH0		TIMER19_CH3	USART0_RX					EXMC_NBL1(2)	HRTIMER_ST6CH1		EVENTOUT
PE2			TIMER2_CH0				TIMER19_CH0						EXMC_A23(2)	HRTIMER_ST7CH0		EVENTOUT
PE3			TIMER2_CH1				TIMER19_CH1						EXMC_A19(2)	HRTIMER_ST7CH1		EVENTOUT
PE4		TIMER0_BRKIN1	TIMER2_CH2	HPDF_DATAIN3			TIMER19_MCH0						EXMC_A20(2)			EVENTOUT
PE5			TIMER2_CH3	HPDF_CKIN3			TIMER19_MCH1						EXMC_A21(2)			EVENTOUT
PE6							TIMER19_MCH2						EXMC_A22(2)			EVENTOUT
PE7			TIMER0_ETI	HPDF_DATAIN2									EXMC_D4(1)			EVENTOUT
PE8		TIMER4_CH2	TIMER0_MCH0	HPDF_CKIN2									EXMC_D5(1)			EVENTOUT
PE9		TIMER4_CH3	TIMER0_CH0	HPDF_CKOUT		SPI0_IO2							EXMC_D6(1)			EVENTOUT
PE10			TIMER0_MCH1	HPDF_DATAIN4		SPI0_IO3					QSPI_SCK(6)		EXMC_D7(1)			EVENTOUT
PE11			TIMER0_CH1	HPDF_CKIN4							QSPI_CSN(6)		EXMC_D8(1)			EVENTOUT
PE12			TIMER0_MCH2	HPDF_DATAIN5							QSPI_IO0(6)		EXMC_D9(1)			EVENTOUT
PE13			TIMER0_CH2	HPDF_CKIN5							QSPI_IO1(6)		EXMC_D10(1)			EVENTOUT
PE14			TIMER0_CH3				TIMER0_BRKIN2				QSPI_IO2(6)		EXMC_D11(1)			EVENTOUT
PE15			TIMER0_BRKIN0				TIMER0_MCH3	USART2_RX			QSPI_IO3(6)		EXMC_D12(1)			EVENTOUT

Table 2-15. Port F alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PF0					I2C1_SDA	SPI1_NSS	TIMER0_MCH2									EVENTOUT
PF1			TIMER19_BRKIN1			SPI1_SCK										EVENTOUT
PF2			TIMER19_CH2		I2C1_SMBA								EXMC_A2(2)			EVENTOUT
PF3			TIMER19_CH3		I2C2_SCL								EXMC_A3(4)			EVENTOUT
PF4			CMP0_OUT	TIMER19_MCH0	I2C2_SDA		HPDF_DATAIN2						EXMC_A4(4)	TRIGSEL_OUT1		EVENTOUT
PF5			TIMER19_MCH1				HPDF_CKIN2						EXMC_A5(4)	TRIGSEL_OUT5		EVENTOUT
PF6		TIMER4_ETI	TIMER3_CH3		I2C1_SCL		TIMER4_CH0	USART2_RTS/USART2_DE			QSPI_IO3(8)					EVENTOUT
PF7			TIMER19_BRKIN0				TIMER4_CH1				QSPI_IO2(8)		EXMC_A1(4)			EVENTOUT
PF8			TIMER19_BRKIN2				TIMER4_CH1				QSPI_IO0(8)		EXMC_A24(4)			EVENTOUT
PF9			TIMER19_BRKIN0	TIMER14_CH0		SPI1_SCK	TIMER4_CH3				QSPI_IO1(8)		EXMC_A25(2)			EVENTOUT
PF10			TIMER19_BRKIN2	TIMER14_CH1		SPI1_SCK					QSPI_SCK(8)		EXMC_A0(2)		USART0_RTS / USART0_DE	EVENTOUT
PF11			TIMER19_ETI										EXMC_NE3(4)			EVENTOUT
PF12			TIMER19_CH0										EXMC_A6(4)			EVENTOUT
PF13			TIMER19_CH1	HPDF_DATAIN6	I2C3_SMBA								EXMC_A7(4)			EVENTOUT
PF14			TIMER19_CH2	HPDF_CKIN6	I2C3_SCL								EXMC_A8(4)			EVENTOUT
PF15			TIMER19_CH3		I2C3_SDA								EXMC_A9(4)			EVENTOUT

Table 2-16. Port G alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PG0			TIMER19_MCH0										EXMC_A10(4)			EVENTOUT
PG1			TIMER19_MCH1										EXMC_A11(4)			EVENTOUT
PG2		TIMER0_BRKIN1	TIMER19_MCH2			SPI0_SCK							EXMC_A12(4)			EVENTOUT
PG3			TIMER19_BRKIN0		I2C3_SCL	SPI0_MISO	TIMER19_MCH3						EXMC_A13(4)			EVENTOUT
PG4			TIMER19_BRKIN2	TIMER7_BRKIN1	I2C3_SDA	SPI0_MOSI							EXMC_A14(4)			EVENTOUT
PG5			TIMER19_ETI			SPI0_NSS							EXMC_A15(4)			EVENTOUT
PG6			TIMER19_BRKIN0		I2C2_SMBA											EVENTOUT
PG7			TIMER19_BRKIN1		I2C2_SCL											EVENTOUT
PG8					I2C2_SDA								EXMC_NE2(4)			EVENTOUT
PG9				TIMER7_BRKIN1			SPI2_SCK	USART0_TX					EXMC_NE1(4)		TIMER14_MCH0	EVENTOUT
PG10(9)	CK_OUT															EVENTOUT

Note:

(1) Functions are available on GD32G553QxTx/VxTx/MxY7TR/MxTx devices only.

(2) Functions are available on GD32G553QxTx/VxTx devices only.

(3) Functions are available on GD32G553QxTx/VxTx/MxY7TR devices only.

(4) Functions are available on GD32G553QxTx devices only.

(5) These QSPI pin functions are highly recommended to be used together, and the supported maximum communication clock is 120MHz for this group. Otherwise the QSPI maximum clock frequency cannot be guaranteed.

(6) These QSPI pin functions are highly recommended to be used together, and the supported maximum communication clock is 120MHz for this group. Otherwise the QSPI maximum clock frequency cannot be guaranteed.

(7) These QSPI pin functions are highly recommended to be used together, and the supported maximum communication clock is 200MHz for this group. Otherwise the QSPI maximum clock frequency cannot be guaranteed.

(8) These QSPI pin functions are highly recommended to be used together, and the supported maximum communication clock is 120MHz for

this group. Otherwise the QSPI maximum clock frequency cannot be guaranteed.

(9) Refer to the description of the NRST_MDSEL bit field of OB_USER option byte in the GD32G5x3 User Manual to configure the NRST-PG10 pin as a PG10 general GPIO function.

3. Functional description

3.1. Arm® Cortex®-M33 core

The Cortex®-M33 processor is a 32-bit processor that possesses low interrupt latency and low-cost debug. The characteristics of integrated and advanced make the Cortex®-M33 processor suitable for market products that require microcontrollers with high performance and low power consumption. The Cortex®-M33 processor is based on the Armv8 architecture and supports a powerful and scalable instruction set including general data processing I/O control tasks, advanced data processing bit field manipulations and DSP. Some system peripherals listed below are also provided by Cortex®-M33:

- Internal Bus Matrix connected with Code bus, System bus, and Private Peripheral Bus (PPB) and debug accesses.
- Nested Vectored Interrupt Controller (NVIC).
- Breakpoint Unit (BPU).
- Data Watchpoint and Trace (DWT).
- Instrumentation Trace Macrocell (ITM).
- Serial Wire JTAG Debug Port (SWJ-DP).
- Trace Port Interface Unit (TPIU).
- Memory Protection Unit (MPU).
- Floating Point Unit (FPU).
- DSP Extension (DSP).

3.2. On-chip memory

- Up to 512KB of on-chip flash memory for instruction and data. Up to 2KB OTP.
- Up to 80KB of SRAM0, 16KB of SRAM1 and 32KB of TCMSRAM.
- Dual bank architecture for read-while-write (RWW) capability.
- 0~7 waiting time within bank0 / bank1 when CPU executes instructions and read data.
- ECC with single bit error correction and double bit errors detection.
- Supports 7-bit ECC function when reading and writing SRAM.
- Provides two execute-only dedicated code read protection (DCRP) area (1 per bank when DBS = 1, 2 for all memory when DBS = 0).
- Provides two secure user area which can be executed only once(1 per bank when DBS = 1, 1 for all memory when DBS = 0).
- Pre-fetch buffer to speed read operations.
- CBUS Instruction cache with 2K bytes which organized as 64 cache line of 4 X 64 bits or 2 X 128 bits.
- CBUS data cache with 512 bytes which organized as 16 cache line of 4 X 64 or 2 X 128 bits.
- 4 erase / program protection areas (2 per bank when DBS=1 and 4 for full memory when

DBS=0) to prevent unexpected operation.

- Low-power mode support.

The GD32G553xx has up to 512KB of on-chip flash memory for instruction and data. The flash memory consists of 512KB main flash organized into 2x256 pages with 1KB capacity when DBS = 1, 256 pages with 2KB capacity when DBS = 0, 2 x 13 KB information block for the boot loader. Each page of main flash memory can be erased individually. ***Table 2-2. GD32G553xx memory map*** shows the memory map of the GD32G553xx series of devices, including Flash, SRAM, peripheral, and other pre-defined regions.

3.3. Clock, reset and supply management

- External 4 to 48 MHz crystal oscillator
- Internal 8 MHz RC oscillator
- Internal 32 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator
- Integrated system clock PLL
- 1.71 to 3.6V application supply and I/Os
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD), BOR (Brown Out Reset), VAVD (V_{DDA} voltage detector), VUVD ($V_{1.1v}$ Under Voltage Detector), VBAT thresholds, temperature thresholds

The Clock Control Unit (CCTL) provides a range of oscillator and clock functions. These include internal RC oscillator and external crystal oscillator, high speed and low speed two types. The frequency of AHB, APB3, APB2 and the APB1 domains can be configured by each prescaler. For GD32G553xxx7, the maximum frequency of the AHB, APB3, APB2 and APB1 domains is 216 / 216 / 216 / 216MHz, the maximum frequency of the system clock can be up to 216 MHz. For GD32G553xxx3, the maximum frequency of the AHB, APB3, APB2 and APB1 domains is 170 / 170 / 170 / 170MHz, the maximum frequency of the system clock can be up to 170 MHz. See ***Figure 2-9. GD32G553xx clock tree*** for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components except for the SW-DP controller and the Backup domain. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from 1.63V and down to 1.61V. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- V_{DD} range: 1.71V to 3.6V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} range: 1.71V to 3.6V, external analog power supplies for ADC, reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} range: 1.71V to 3.6V, power supply for RTC unit, LXTAL oscillator, BPOR and BREG, and three BKP PADs, including PC13 to PC15.

3.4. Boot modes

GD32G553xx supports three BOOT modes, including:

- Boot from main Flash memory (default)
- Boot from system memory
- Boot from on-chip SRAM

In default condition, boot from main Flash memory is selected. The boot loader is located in the internal boot ROM memory (system memory). It is used to reprogram the Flash memory by using USART0 (PA9 and PA10), USART1 (PA2 and PA3), USART2 (PC10 and PC11), I2C1 (PC4 and PA8), I2C2 (PC8 and PC9) and I2C3 (PC6 and PC7).

3.5. Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are sleep mode, deep-sleep mode and standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep mode**

  In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt / event can wake up the system.

- **Deep-sleep mode**

  In Deep-sleep mode, all clocks in the V_{CORE} domain are off, and all of IRC8M, HXTALand PLLs are disabled. The contents of SRAM and registers are preserved. The LDO can operate normally or in low power mode depending on the LDOLP bit in the PMU_CTL0 register. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the 16 external lines, the RTC alarm, RTC Tamper and TimeStamp event or LXTAL clock stuck, RTC wakeupTimer, the LVD/VAVD/VOVD/VUVD, CMP0/1/2/3/4/5/6/7 output, LPTIMER wakeup, CAN0/1/2 wakeup, I2C0/1/2/3 wakeup, and USART0/1/2 wakeup. When exiting the deep-sleep mode, the IRC8M is selected as the system clock.

- **Standby mode**

  In standby mode, the whole V_{CORE} domain is power off, the LDO is shut down, and all of IRC8M, HXTAL and PLL are disabled. Besides, the contents of SRAM and registers in 1.1V power domain are lost in Standby mode. There are five wakeup sources for the Standby mode, including the external reset from NRST pin, the RTC alarm / time stamp / tamper events, the FWDGT reset, LXTAL clock failure detection and the rising edge on WKUP pins.

3.6. Trigger selection controller (TRIGSEL)

- Support different optional trigger inputs.
- Support up to 243 trigger input signals.
- Each peripheral has its corresponding register to select trigger input signal.
- Trigger input source could be external input signal or output of peripheral.
- Trigger selection output could be for external output or peripheral input.

The trigger selection controller (TRIGSEL) allows software to select the trigger input signal for various peripherals. TRIGSEL provides a flexible mechanism, there are up to 243 trigger input signals could be selected. Each peripheral corresponding to the independent trigger selection controller. Configure the corresponding register to select the different trigger signal for the specified trigger input of each peripheral.

3.7. General-purpose and alternate-function I/Os (GPIO and AFIO)

- Up to 107 general purpose I/O pins (GPIO), all mappable on 16 external interrupt lines.
- Each pin weak pull-up / pull-down function.
- Output push-pull / open drain enable control.
- Analog input / output configuration.
- Alternate function input / output configuration.
- The input signals can be qualified to remove unwanted noise.
- GPIO have the capable of state retention when system reset (exclude power reset).

GD32G553xx is up to 107 general purpose I/O pins (GPIO), named PA0~PA15, PB0~PB15, PC0~PC15, PD0~PD15, PE0~PE15, PF0~PF15, PG0~PG10 for the device to implement logic input/output functions. Each GPIO port has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt/Event Controller Unit (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins.

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), input, peripheral alternate function or analog mode. Each GPIO pin can be configured as pull-up, pull-down or no pull-up/pull-down. All GPIOs are high-current capable except for analog mode.

3.8. Direct memory access controller (DMA)

- 14 channels (7 for DMA0 and 7 for DMA1) and each channel are configurable.
- Support independent 8, 16, 32-bit memory and peripheral transfer.
- Support independent fixed and increasing address generation algorithm of memory and peripheral.
- Peripherals supported: Timers, ADC, DAC, SPI, I2C, USART, UART, QSPI, CAU,

HRTIMER, HPDF, FAC, TMU, and CAN.

The direct memory access (DMA) controller provides a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory.

There are 14 channels in the DMA controller (7 for DMA0 and 7 for DMA1). Each channel is dedicated to manage memory access requests from one or more peripherals. An arbiter is implemented inside to handle the priority among DMA requests.

3.9. DMA request multiplexer (DMAMUX)

- 14 channels for DMAMUX request multiplexer.
- 4 channels for DMAMUX request generator.
- Support 21 trigger inputs and 21 synchronization inputs.

DMAMUX is a transmission scheduler for DMA requests. The DMAMUX request multiplexer is used for routing a DMA request line between the peripherals / generated DMA request (from the DMAMUX request generator) and the DMA controller. Each DMAMUX request multiplexer channel selects a unique DMA request line, unconditionally or synchronously with events from its DMAMUX synchronization inputs. The DMA request is pending until it is served by the DMA controller which generates a DMA acknowledge signal (the DMA request signal is de-asserted).

3.10. CRC calculation unit (CRC)

- Supports 7 / 8 / 16 / 32 bit data input.
- For 7(8) / 16 / 32 bit input data length, the calculation cycles are 1 / 2 / 4 AHB clock cycles.
- User configurable polynomial value and size.
- Free 8-bit register is unrelated to calculation and can be used for any other goals by any other peripheral devices.

A cyclic redundancy check (CRC) is an error-detecting code commonly used in digital networks and storage devices to detect accidental changes to raw data. The CRC calculation unit can be used to calculate 7 / 8 / 16 / 32 bit CRC code within user configurable polynomial.

3.11. Configurable logic array (CLA)

- Four independent CLA units, with two input Signal Selector(SIGS), supporting 16 input signals, including external pins, timer channels, CMP, ADC, and CLA asynchronous outputs.
- A Logic-Configure-Unit(LCU) providing 256 programmable digital logic functions is

implemented in each CLA units.

- Programmable asynchronous and synchronous output
- CLA output can be configured to synchronize with external pins and timers.
- Four CLA units can be combined and support complicated logic operations.

The configurable logic array provides 256 programmable digital logic operations for external pins, CMP, ADC and timers without intervention from the CPU. Four independent CLA units are implemented in this module. Each CLA unit supports configurable asynchronous and synchronous output for GPIO pins.

3.12. True random number generator (TRNG)

- LFSR mode and NIST mode to generate random number.
- About 40 periods of TRNG_CLK are needed between two consecutive random numbers in LFSR mode.
- 32bit random number is generated each time in LFSR mode.
- TRNG NIST mode follow the NIST SP800-90B.
- 32bit*4 or 32bit*8 random number is generated each time in NIST mode.
- TRNG has the functions of startup and in-service self-check, associated with specific error flags.
- Disable TRNG module will significantly reduce the chip power consumption.
- 128-bit random value seed is generated from analog noise, so the random number is a true random number.

The true random number generator (TRNG) module can generate a 32-bit random value by using continuous analog noise and it has been pre-certified NIST SP800-90B.

3.13. Cryptographic Acceleration Unit (CAU)

- Supports DES, TDES or AES (128, 192, or 256) algorithms.
- DES/TDES supports Electronic codebook (ECB) or Cipher block chaining (CBC) mode.
- AES supports 128bits-key, 192bits-key or 256 bits-key.
- Multiple modes are supported respectively in DES, TDES and AES, including Electronic codebook (ECB), Cipher block chaining (CBC), Counter mode (CTR), Galois / counter mode (GCM), Galois message authentication code mode (GMAC), Counter with CBC-MAC (CCM), Cipher Feedback mode (CFB) and Output Feedback mode(OFB).
- DMA transfer for incoming and outgoing data is supported.

The cryptographic acceleration unit (CAU) is used to encipher and decipher data with DES, Triple-DES or AES (128, 192, or 256) algorithms. DES / TDES / AES algorithms with different key sizes are supported to perform data encryption and decryption in the CAU in multiple modes. The CAU is a 32-bit peripheral, DMA transfer is supported and data can be accessed in the input and output FIFO.

3.14. Trigonometric Math Unit (TMU)

- 10 kinds of functions.
- Interrupt and DMA requests.
- The fixed point q1.31 / q1.15 format or IEEE754 32-bit single precision floating-point format is configurable.
- Programmable precision.
- CORDIC-algorithm core: circular system and hyperbolic system, rotation pattern and vectoring pattern.

The Trigonometric Math Unit (TMU) is a fully configurable block that execute common trigonometric and arithmetic operations. It can be used to calculate total 10 kinds of functions. The input / output data meet q1.31 or q1.15 fixed point format or IEEE754 32-bit single precision floating-point format.

3.15. Fast Fourier Transform (FFT)

- Support 1024 / 512 / 256 / 128 / 64 / 32 points FFT.
- Support IFFT mode.
- IEEE-754 single precision float point complex number input and output data.
- DMA master to load and store data.
- Support window function configured in memory.
- Support input down sample.

The Fast Fourier Transform (FFT) is an efficient computation of the Discrete Fourier Transform (DFT). The module supports CPU to offload FFT operations. Compared to a software implementation, it can accelerate calculations and time critical tasks. The module supports 6 configruation FFT point number up to 1024, and input and output data should be IEEE-754 single precision float point complex number.

3.16. Analog to digital converter (ADC)

- 12-bit ADC conversion rate is up to 5.3 MSPS.
- 12-bit, 10-bit, 8-bit or 6-bit configurable resolution for ADC.
- Oversampling ratio arbitrarily adjustable from 2x to 1024x.
- ADC supply requirements: 1.62V to 3.6V and typical power supply voltage is 3.3V.
- ADC input voltage range: $V_{SSA} \leq V_{IN} \leq V_{REFP}$.
- Temperature sensor.
- Start-of-conversion can be initiated by software or TRIGSEL.

A 12-bit successive approximation analog-to-digital converter module(ADC) is integrated on the MCU chip. ADC0 has 14 external channels, 5 internal channels (temperature sensor, the battery voltage, DAC0_OUT0, DAC0_OUT1, V_{REFINT} inputs channel), ADC1 has 16 external channels, 3 internal channels (DAC1_OUT0, DAC1_OUT1, V_{REFINT} inputs channel), ADC2

has 15 external channels, 5 internal channels (V_{REFINT} inputs channel, DAC2_OUT0, DAC2_OUT1, high-precision temperature sensor, the battery voltage), ADC3 has 18 external channels, 3 internal channels (DAC3_OUT0, DAC3_OUT1, V_{REFINT} inputs channel). After sampling and conversion, the conversion results can be stored in the corresponding data registers according to the least significant bit(LSB) alignment or the most significant(MSB) bit alignment. An on-chip hardware oversample scheme improves performances and reduces the computational burden of MCU.

To ensure a high accuracy on ADC and DAC, the ADC/DAC independent external reference voltage should be connected to VREFP pins. According to the different packages, VREFP pin can be connected to VDDA pin, or external reference voltage. For packages without VREFP pin, VREFP is internally connected to VDDA.

3.17. Digital to analog converter (DAC)

- Maximum sampling rate of 1 MSPS for DAC0 and DAC1, and maximum sampling rate of 15 MSPS for DAC2 and DAC3.
- 8-bit or 12-bit resolution.
- Left or right data alignment.
- DMA capability for each unit and underrun function.
- Conversion update synchronously.
- Conversion trigged by external triggers.
- Configurable internal buffer.
- External voltage reference, V_{REFP}.
- Output buffer calibration.
- Using sample and keep mode to reduce the power consumption.
- Noise wave generation (LFSR noise mode and Triangle noise mode).
- Sawtooth wave generation.
- Two DAC units in concurrent mode.
- Output can be configured to persist when system reset.

The Digital-to-analog converter converts 12-bit digital data to a voltage on the external pins. The digital data can be set to 8-bit or 12-bit mode, left-aligned or right-aligned mode. DMA can be used to update the digital data on external triggers. The output voltage can be optionally buffered for higher drive capability, and DAC output buffer can be calibrated to improve output accuracy. The sample and keep mode can reduce the power consumption of DAC.

3.18. Comparator (CMP)

- Rail-to-rail comparators.
- Configurable hysteresis.
- Each comparator has configurable analog input source.
- Outputs with blanking source.

- Outputs to I/O.
- Outputs to timers.
- Outputs to EXTI.
- Outputs to NVIC.
- Outputs to TRIGSEL.
- Outputs can be configured to persist when system reset.

The general purpose CMP can work either standalone (all terminal are available on I/Os) or together with the timers.

It can be used to wake up the MCU from low-power mode by an analog signal, provide a trigger source when an analog signal is in a certain condition, achieve some current control by working together with a PWM output of a timer and the DAC.

3.19. VREF

- Stable voltage, and product calibrated.
- Connects to VREFP pin to source off-chip circuits.
- 2.048V, 2.5V or 2.9V configurable reference voltage output.

A precision internal reference circuit is inside. The internal voltage reference unit is used to provide voltage reference for ADC / DAC, or used by off-chip circuit connecting to VREFP pin.

3.20. Real time clock (RTC) and backup registers

- Support calendar function, which can support year, month, date, day, hours, minutes, seconds and subseconds (date is the day of week and day is the day of month).
- Daylight saving compensation supported, which is realized through software
- External high-accurate low frequency (50Hz or 60Hz) clock used to achieve higher calendar accuracy performed by reference clock detection option function.
- Atomic clock adjust (max adjust accuracy is 0.95PPM) for calendar calibration performed by digital calibration function.
- Sub-second adjustment by shift function
- Time-stamp function for saving event time
- Three tamper sources can be chosen and tamper type is configurable (RTC_TAMP0, RTC_TAMP1 and RTC_TAMP2).
- Programmable calendar and two field maskable alarms.
- Maskable interrupt source:
  - Alarm 0 and Alarm 1
  - Time-stamp detection
  - Tamper detection
  - Auto wakeup event
- Thirty-two 32-bit (128 bytes total) universal backup registers which can keep data under power saving mode. Backup register will be reset if tamper event detected.

The RTC provides a time which includes hour / minute / second / sub-second and a calendar includes year / month / day / week day. The time and calendar are expressed in BCD code except sub-second. Sub-second is expressed in binary code. Hour adjust for daylight saving time. Working in power saving mode and smart wakeup is software configurable. Support improving the calendar accuracy using extern accurate low frequency clock.

The RTC is an independent timer which provides a set of continuously running counters in backup registers to provide a real calendar function, and provides an alarm interrupt or an expected interrupt. It is not reset by a system or power reset, or when the device wakes up from standby mode. A prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 KHz from external crystal oscillator.

3.21. Timers and PWM generation

- Three 16-bit Advanced timer (TIMER0, TIMER7, TIMER19), two 16-bit General-L0 timers (TIMER2, TIMER3), two 32-bit General-L0 timers (TIMER1, TIMER4), one 16-bit General-L3 timer (TIMER14), two 16-bit General-L4 timers (TIMER15, TIMER16), two 16-bit Basic timer (TIMER5 & TIMER6).
- Up to 8 independent channels of PWM, output compare or input capture for each general timer and external trigger input.
- 16-bit, motor control PWM advanced timer with programmable dead-time generation for output match.
- Decoder interface controller with two inputs using quadrature decoder and decoder modes.
- 24-bit SysTick timer down counter.
- 2 watchdog timers (free watchdog timer and window watchdog timer).

The advanced timer (TIMER0, TIMER7, TIMER19) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general timer. The 8 independent channels can be used for input capture, output compare, PWM generation (edge-aligned or center-aligned counting modes) and single pulse mode output. It can be synchronized with external signals or to interconnect with other general timers together which have the same architecture and features.

The general level 0 timer, can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TIMER1/4 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TIMER2/3 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. The general level 0 timer also supports an encoder interface with two inputs using quadrature decoder mode and decoder mode.

The general level3 timer module (TIMER14) is a three-channel timer that supports both input capture and output compare. They can generate PWM signals to control motor or be used for power management applications. The general level3 timer has a 16-bit counter that can be

used as an unsigned counter.

The general level4 timer module (TIMER15/16) is a two-channel timer that supports both input capture and output compare. They can generate PWM signals to control motor or be used for power management applications. The general level4 timer has a 16-bit counter that can be used as an unsigned counter.

The basic timer module(TIMER5/6) has a 16-bit counter that can be used as an unsigned counter. The basic timer TRGO0 is connected to DAC by TRIGSEL module.

The GD32G553xx has two watchdog peripherals, free watchdog timer and window watchdog timer. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-bit prescaler. It is clocked from an independent 32 KHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog timer is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wakeup interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter.
- Auto reload capability.
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source.

3.22. High-Resolution Timer (HRTIMER)

- High- resolution timing units: Master_TIMER, Slave_TIMERx (x=0.. 7).
- 16 digital signals outputs channels: they can be controlled by any timing unit and output independently or coupled into 8 pairs.
- Synchronization outputs: synchronize external resources as master.
- Synchronization inputs: be synchronized as a slaver.
- Multiple internal signals connected to the ADC and DAC.
- Various fault input protection scheme: fault input channel and system fault.
- Bunch mode controller to handle light-load operation.
- 10 interrupt vectors: Master_TIMER interrupt, Slave_TIMERx (x=0..7) interrupt, fault interrupts.
- 9 DMA request: Master_TIMER requests, Slave_TIMERx (x=0..7) requests.
- DMA mode for multiple registers update.

HRTIMER has a high-resolution counting clock and can be used for high-precision timing. It

can generate 16 high resolution and flexible digital signals to control motor or be used for power management applications. It has multiple internal signals connected to the ADC and DAC. It can be used for control and monitoring purposes. It can handle various fault input for safe purposes.111

3.23. Low power timer (LPTIMER)

- Counter width: 16-bit.
- Source of counter clock is selectable as internal clock or external clock
- Operating mode: continuous counting mode or single counting mode
- Programmable prescaler: 3 bit.
- Channel output is user-configurable:
  Programmable PWM mode, single pulse mode, set mode
- Selectable trigger: software trigger or hardware input trigger
- Decoder mode: decoder mode 0 and decoder mode 1

The LPTIMER is a 16-bit timer and it is able to keep running in all power modes except for standby mode with its diversity of clock sources. The LPTIMER provides a flexible mechanism of the clock, which reduces the power consumption to a minimum while also achieving the required functions and performance. The LPTIMER can be used as a pulse counter with no internal clock source. The LPTIMER has the ability to wake up the system from the low-power modes, and it is suitable for realizing timeout mode with very low power consumption.

3.24. Infrared interface (IFRP)

- The IFRP output signal is decided by TIMER15_CH0 and TIMER16_CH0.
- To get correct infrared ray signal, TIMER15 should generate low frequence modulation envelope signal, and TIMER16 should generate high frequence carrier signal.
- The IFRP output (PB9/PA13) can control LED interface by setting PB9FMPEN in SYSCFG_CFG1.

Infrared interface (IFRP) is used to control infrared light LED, and send out infrared data to implement infrared ray remote control. There is no register in this module, which is controlled by TIMER15 and TIMER16. The capacity of module's output high current can be improved by set the GPIO pin to Fast Mode.

3.25. Universal synchronous/asynchronous receiver transmitter (USART/UART)

- Programmable baud-rate generator allowing speed up to 27 MBits/s when the clock frequency is 216 MHz and oversampling is by 8, and allowing speed up to 21.25 MBits/s when the clock frequency is 170 MHz and oversampling is by 8.

- Supports both asynchronous and clocked synchronous serial communication modes.
- IrDA support.
- LIN break generation and detection.
- ISO 7816-3 compliant smartcard interface.

The USART (USART0, USART1, USART2) and UART (UART3, UART4) are used to transfer data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART/UART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART/UART transmitter and receiver.

3.26. Inter-integrated circuit (I2C)

- Up to four I2C bus interfaces can support both master and slave mode with a frequency up to 1 MHz (Fast mode plus).
- Provide arbitration function, optional PEC (packet error checking) generation and checking.
- Supports 7-bit and 10-bit addressing mode and general call addressing mode.
- SMBus 3.0 and PMBus 1.3 compatible.
- Wakeup from sleep mode and Deep-sleep mode on I2C address match.

The I2C (inter-integrated circuit) module provides an I2C interface which is an industry standard two-line serial interface for MCU to communicate with external I2C interface. I2C bus uses two serial lines: a serial data line, SDA, and a serial clock line, SCL. The I2C interface implements standard I2C protocol with standard mode (up to 100KHz), fast mode (up to 400KHz) and fast mode plus (up to 1MHz) as well as CRC calculation and checking, SMBus (system management bus), and PMBus (power management bus).

3.27. Controller area network (CAN)

- Supports CAN protocol version 2.0A/B.
- Compliant with the ISO 11898-1:2015 standard.
- Supports CAN classical frame with up to 8 data bytes, baudrate up to 1 Mbit/s.
- Supports CAN FD frame with up to 64 data bytes, baudrate up to 8 Mbit/s.
- Supports time stamp based on 16-bit free running counter.
- Maskable interrupts.
- Supports four communication mode: normal mode, Inactive mode, Loopback and silent mode, and Monitor mode.
- Supports two power saving modes: CAN_Disable mode, and Pretended Networking mode.
- Supports transmitter delay compensation for CAN-FD frames at faster data rates.
- Support two wakeup methods for waking up from Pretended Networking mode: wakeup matching event, and wakup timeout event.

- Global network time, synchronized by a specific message.

CAN bus (Controller Area Network) is a bus standard designed to allow microcontrollers and devices to communicate with each other without a host computer. The CAN interface supports the CAN 2.0A/B protocol, ISO 11898-1:2015 and BOSCH CAN-FD specification.

The CAN module is a CAN Protocol controller with a very flexible mailbox system for transmitting and receiving CAN frames. The mailbox system consists of a set of mailboxes that store configuration and control data, timestamp, message ID, and data. The space of up to 32 mailboxes can also be configured as Rx FIFO with ID filtering against up to 104 extended IDs or 208 standard IDs or 416 partial 8-bit IDs, and configure receive FIFO/mailbox private filter register for up to 32 ID filter table elements.

3.28. Serial peripheral interface (SPI)

- Master or slave operation with full-duplex or simplex mode.
- Separate transmit and receive 32-bit FIFO.
- Data frame size can be 4 to 16 bits.
- Hardware CRC calculation, transmission and checking.
- SPI TI mode supported.
- Quad-SPI configuration available in master mode (only in SPI0).

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). All SPIs can be served by the DMA controller. The serial peripheral interface (SPI) provides a SPI protocol of data transmission and reception function in master or slave mode. Both full-duplex and simplex communication modes are supported, with hardware CRC calculation and checking. Quad-SPI master mode is also supported in SPI0.

3.29. Quad-SPI interface (QSPI)

- Three functional modes: normal mode (address extend), read polling mode and memory map mode.
- Fully programmable command format for both normal mode and memory map mode.
- Integrated FIFO for transmission/reception.
- Support SDR and DDR mode.
- 8, 16, or 32-bit data accesses.
- DMA channel for normal mode.

The QSPI is a specialized interface that can communicate with flash memories. This interface supports single, dual or quad SPI FLASH. It can operate in normal mode, read polling mode and memory map mode.

3.30. External memory controller (EXMC)

- Supported external memory: SRAM, PSRAM, ROM and NOR-Flash.
- Each bank has its own chip-select signal which can be configured independently.
- Independent read/write timing configuration to a sub-set memory type.
- 8 or 16 bits bus width.
- Write FIFO with max 16 words data storage.

The external memory controller EXMC, is used as a translator for MCU to access a variety of external memory. By configuring the related registers, it can automatically convert AMBA memory access protocol into a specific memory access protocol, such as SRAM, ROM, NOR Flash, PSRAM. Users can also adjust the timing parameters in the configuration registers to improve memory access efficiency. EXMC access space is divided into multiple banks; each bank is assigned to access a specific memory type with flexible parameter configuration as defined in the control registers. The EXMC also can be configured to interface with the most common LCD module of Motorola 6800 and Intel 8080 series and reduce the system cost and complexity.

3.31. High-Performance Digital Filter (HPDF)

- 8 multiplex digital serial input channels.
  - configurable SPI and Manchester interfaces.
- 8 internal digital parallel input channels.
  - input with up to 16-bit resolution.
  - internal source: ADC data or memory (CPU / DMA write) data stream.
- Configurable Sinc filter and integrator.
  - the order and oversampling rate (decimation rate) of Sinc filter can be configured.
  - sampling rate of configurable integrator.
- Threshold monitor function.
  - independent Sinc filter, configurable order and oversampling rate (decimation rate).
  - configurable data input source: serial channel input data or HPDF output data.
- Malfunction monitor function.
  - A counter with 8 bits is used to monitor the continuous 0 or 1 in the serial channel input data stream.
- Extreme monitor function.
  - store minimum and maximum values of output data values of HPDF.
- Up to 24-bit output data resolution.
- Clock signal can be provided to external sigma delta modulator.
  - provide configurable clock signal by the CKOUT pin.
- Flexible conversion configuration function.
  - the conversion channel is divided into regular group and inserted group.
  - support multiple conversion modes and startup modes.
- HPDF output data is in signed format.

A high performance digital filter module (HPDF) for external sigma delta (Σ-Δ) modulator is integrated in GD32G553xx. HPDF supports SPI interface and Manchester-coded single-wire interface. The external sigma delta modulator can be connected with MCU by the serial interface, and the serial data stream output by sigma delta modulator can be filtered. In addition, HPDF also supports the parallel data stream input, which can be selected from internal ADC peripherals or from MCU memory.

3.32. Filter arithmetic accelerator (FAC)

- Fixed or float multiplier and accumulator.
- 256 x 32-bit local memory.
- 16-bit fixed-point or 32-bit float point input and output.
- Up to three buffers, two input buffers and one output buffer.
- Buffer can be circular.
- FIR and IIR can be realized.
- Vector functions support convolution, Dot product, correlation functions.
- Data can be read and written through DMA.

The filter arithmetic accelerator unit consist of multiplier, accumulator and address generation logic, so as to index vector elements stored in local memory. Circular buffering is valid for both input and output, which allows to realize finite impulse response (FIR) filters and infinite impulse response (IIR) filters. The unit support CPU to be free from frequent or lengthy filtering operations, compared with software implementation, it can accelerate calculations and the processing speed of time critical tasks.

3.33. Debug mode

- Serial wire JTAG debug port (SWJ-DP).

The GD32G553xx series provide a large variety of debug, trace and test features. They are implemented with a standard configuration of the Arm® CoreSight™ module together with a daisy chained standard TAP controller. Debug and trace functions are integrated into the Arm® Cortex®-M33. The debug system supports serial wire debug (SWD) and trace functions in addition to standard JTAG debug.

3.34. Package and operation temperature

- LQFP128 (GD32G553QxTx), LQFP100 (GD32G553VxTx), WLCSP81 (GD32G553MxY7TR), LQFP80 (GD32G553MxTx), LQFP64 (GD32G553RxTx), LQFP48 (GD32G553CxTx) and QFN48 (GD32G553CxUx).
- Operation temperature range: For GD32G553xxx7, -40°C to +105°C (industrial level). For GD32G553xxx3, -40°C to +125°C (industrial level).

4. Electrical characteristics

4.1. Parameter introduction

- Parameter conditions: Unless otherwise specified, all values given for V_{DD} = V_{DDA} = 3.3 V, T_A = 25°C, and all voltages are referenced to Vss.
- Value guaranteed by design, not 100% tested in production indicates that the value is derived from design or simulation and/or process characteristics.
- Value guaranteed by characterization, not 100% tested in production indicates that the value is derived from random test.
- Value guaranteed by sample, not 100% tested in production indicates that the value is derived from testing parameters with a small sample size.
- If the value is not specially indicated, it means the value guaranteed by 100% tested in production.

See the following table for some abbreviation terms and their descriptions in this chapter.

Table 4-1. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
CAN	Controller Area Network
DAC	Digital-to-Analog Converter
DMA	Direct Memory Access
GPIO	General Purpose Input/Output
JTAG	Joint Test Action Group
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
SPI	Serial Peripheral Interface

4.2. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-2. Absolute maximum ratings(1)

Symbol	Description	Min	Max	Unit
V_{DD}	External voltage range(2)	V_{SS} - 0.3	V_{SS} + 4	V
V_{DDA}	External analog supply voltage(3)	V_{SSA} - 0.3	V_{SSA} + 4	V
V_{BAT}	External battery supply voltage	V_{SS} - 0.3	V_{SS} + 4	V

Symbol	Description	Min	Max	Unit
V_{IN}	Input voltage on 5V tolerant pin(4)	V_{SS} - 0.3	V_{DD} + 4	V
	Input voltage on other I/O	V_{SS} - 0.3	4	V
$\|\Delta V_{DDx}\|$	Variations between different VDD power pins	—	50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between different ground pins(5)	—	50	mV
I_{IO}	Maximum current for GPIO pins	—	20	mA
$\sum I_{IO}$	Maximum current sunk/sourced by all GPIO pin	—	100	
$\sum I_{DD}$	Total current into all VDD pins	—	300	
$\sum I_{SS}$	Total current into all VSS pins	—	300	
I_{INJ}	Injected current on each GPIO pin(5)	—	-5/0	
ΣI_{INJ}	Total injected current on all GPIO pins(6)	—	±25	
T_{STG}	Storage temperature range	-65	150	°C
T_J	Maximum junction temperature for grade 7 devices	—	125	°C
	Maximum junction temperature for grade 3 devices	—	135	

(1) Value guaranteed by design, not 100% tested in production.
(2) All main power and ground pins should be connected to an external power source within the allowable range.
(3) It is recommended that VDD and VDDA are powered by the same source. The maximum difference between VDD and VDDA does not exceed 300 mV during power-up and operation.
(4) V_{IN} maximum value cannot exceed 5.5 V.
(5) I_{INJ} must never be exceeded. Negative injection on any analog input pins disturbs the analog performance of the device.
(6) When several inputs are submitted to a current injection, the maximum ΣI_{INJ} is the absolute sum of the positive and negative injected currents (instantaneous values).

4.3. Operating conditions characteristics

Table 4-3. General operating conditions(1)(6)

Symbol	Description	Conditions	Min(1)	Typ(1)	Max(1)	Unit
V_{DD}	Supply voltage	—	1.71	3.3	3.6	V
V_{DDA}	Analog supply voltage	ADC used,f_{ADCMAX} = 50 MHz	1.71	3.3	3.6	V
		ADC used,f_{ADCMAX} = 80 MHz	2.4			
		DAC output buffer OFF, DAC_OUT Pin not connected (internal connection only)	1.71			
		DAC work in other mode	1.8			
		VREFBUF used	V_{REFP}+0.3			
V_{BAT}(2)(7)	Battery supply voltage	—	1.71	—	3.6	V
V_{CORE}	Core logic supply voltage powered by internal voltage regulator	LDOVS[4:0]=01100	—	1.1	—	V
		LDOVS[4:0]=01110	—	1.15	—	

Symbol	Description	Conditions	Min(1)	Typ(1)	Max(1)	Unit
f_{HCLK}	AHB clock frequency for grade 7 devices	Vcore=1.15V	—	—	216	MHz
		Vcore=1.1V	—	—	170	
	AHB clock frequency for grade 3 devices	—	—	—	170	
f_{APB1}	APB1 clock frequency for grade 7 devices	Vcore=1.15V	—	—	216	
		Vcore=1.1V	—	—	170	
	APB1 clock frequency for grade 3 devices	—	—	—	170	
f_{APB2}	APB2 clock frequency for grade 7 devices	Vcore=1.15V	—	—	216	
		Vcore=1.1V	—	—	170	
	APB2 clock frequency for grade 3 devices	—	—	—	170	
f_{APB3}	APB3 clock frequency for grade 7 devices	Vcore=1.15V	—	—	216	
		Vcore=1.1V	—	—	170	
	APB3 clock frequency for grade 3 devices	—	—	—	170	
P_D(3)	Power dissipation at T_A = 105°C of LQFP128(4)	—	—	—	418	mW
	Power dissipation at T_A = 125°C of LQFP128(4)		—	—	209	
	Power dissipation at T_A = 105°C of LQFP100(4)		—	—	407	
	Power dissipation at T_A = 125°C of LQFP100(4)		—	—	203	
	Power dissipation at T_A = 105°C of WLCSP81(4)		—	—	445	
	Power dissipation at T_A = 105°C of LQFP80(4)		—	—	386	
	Power dissipation at T_A = 125°C of LQFP80(4)		—	—	193	
	Power dissipation at T_A = 105°C of LQFP64(4)		—	—	367	
	Power dissipation at T_A = 125°C of LQFP64(4)		—	—	183	
	Power dissipation at T_A = 105°C of LQFP48(4)		—	—	287	
	Power dissipation at T_A = 125°C of LQFP48(4)		—	—	144	
	Power dissipation at T_A = 105°C of QFN48(4)		—	—	699	
	Power dissipation at T_A = 125°C of QFN48(4)		—	—	350	

Symbol	Description	Conditions	Min(1)	Typ(1)	Max(1)	Unit
T_A	Operating temperature range for grade 7 devices	Maximum power dissipation	-40	—	105	°C
	Operating temperature range for grade 3 devices	Maximum power dissipation	-40	—	115	
		Low-power dissipation(5)	-40	—	125	
T_J	Junction temperature for grade 7 devices	—	-40	—	125	°C
	Junction temperature for grade 3 devices		-40	—	135	

(1) Value guaranteed by design, not 100% tested in production.

(2) In the application which V_{BAT} supply the backup domains, if the VBAT voltage drops below the minimum value, when V_{DD} is powered on again, it is necessary to refresh the registers of backup domains and enable LXTAL again.

(3) If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.

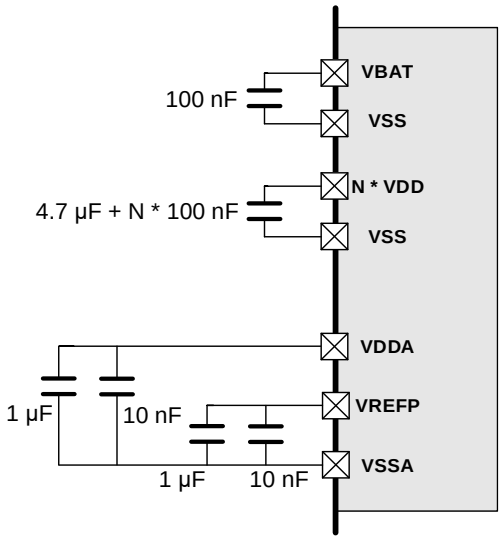
(4) For grade 7 devices, the parameter of T_A = 105°C, For grade 3 device, the parameter of T_A = 125°C.

(5) In low-power dissipation state(In limited power dissipation state), T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section : Thermal characteristics*).

(6) For the specific usage differences between grade 7 and grade 3 devices, please refer to the application note.

(7) When both V_{DD} and V_{BAT} are powered simultaneously, it is required that $V_{BAT} \leq V_{DD} + 0.3$ V.

Figure 4-1. Recommended power supply decoupling capacitors(1)(2)



(1) VREFN pins are internally connected to VSSA pins.

(2) All decoupling capacitors need to be as close as possible to the pins on the PCB board.

4.4. Power supply requirement characteristics

Table 4-4. Power supply requirement characteristics(1)

Symbol	Description	Conditions	Min	Max	Unit
t_{VDD}(1)	V_{DD} rise time rate	—	0	∞	µs/V
	V_{DD} fall time rate		10	∞	
t_{VDDA}(1)	V_{DDA} rise time rate	—	0	∞	
	V_{DDA} fall time rate		10	∞	

(1) Value guaranteed by design, not 100% tested in production.

Table 4-5. Start-up timings of Operating conditions(1)(2)(3)

Symbol	Description	Conditions	Typ	Unit
t_{ST}	Start-up time	Clock source from IRC8M	110(4)	µs
			11.86(5)	ms

(1) Value guaranteed by sample, not 100% tested in production.
(2) After power-up, the start-up time is the time between the rising edge of NRST high and the first I/O instruction conversion in SystemInit function.
(3) PLL is off.
(4) Excluding the time to initialize SRAM during startup.
(5) Including the time to initialize 128kB SRAM by software during startup.

Table 4-6. Wake-up time from power saving modes(1)(2)

Symbol	Description	Conditions	Min	Typ	Max	Unit
t_{Sleep}	Wakeup from Sleep mode	—	—	2.04		µs
$t_{Deep-sleep}$	Wakeup from Deep-sleep mode（LDO in normal mode）	—	—	4.08	—	µs
	Wakeup from Deep-sleep mode（LDO in low power mode）	—	—	4.08	—	µs
$t_{Standby}$	Wakeup from Standby mode	Excluding the time to initialize SRAM during wakeup	—	104	—	µs
		Including the time to initialize 128kB SRAM by software during wakeup	—	10.34	—	ms

(1) Value guaranteed by sample, not 100% tested in production.
(2) The wakeup time is measured from the wakeup event to the point at which the application code reads the first instruction in Systeminit function under the below conditions: V_{DD} = V_{DDA} = 3.3 V, IRC8M = System clock = 8 MHz.

4.5. Power consumption

The power consumption is measured as described in ***Figure 4 1. Power consumption measurement diagram***. The current consumption values are derived from the tests powered by V_{DD} = V_{DDA} except BKP_ONLY mode, while the current is I_{SUM}. In BKP_ONLY mode, the RTC unit and LXTAL oscillator are powered by the V_{BAT}, while the current is I_{BAT}. Unless otherwise stated, V_{DD} = V_{DDA} = 3.3 V is applied to supply pins in typical current consumption columns, and V_{DD} = V_{DDA} = $V_{DD(MAX)}$ is applied in maximum current consumption columns.

Figure 4-2. Power consumption measurement diagram

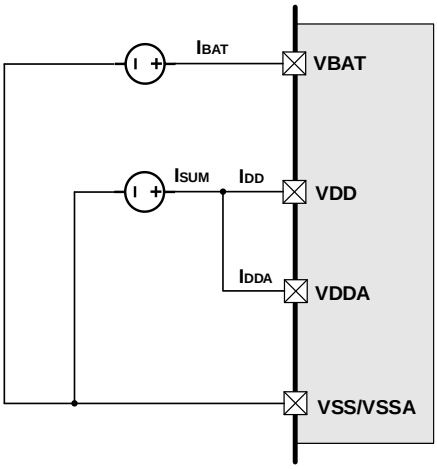


Table 4-7. Power consumption in Run mode(1)(2)

Symbol	Description	Conditions				Typ				Max			Unit
		General	Peripherals	Execute from	f_{HCLK1}	25°C	85°C	105°C	125°C	85°C	105°C	125°C	
I_{SUM}	Sum of supply current from VDD and VDDA (Run mode)	HXTAL_bypass = 8 MHz, PLL on, System clock = f_{HCLK1}	All disabled	EFLASH	216 MHz	69.8	76.3	80.4	91.2	97.7	111.9	137.6	mA
					170 MHz	54.4	60.1	63.8	73.3	77.8	90.5	113.4	
					120 MHz	40.3	45.9	49.6	58.9	61.6	74.7	97.6	
					80 MHz	28.9	34.4	38.0	47.2	48.7	62.1	84.8	
					32 MHz	15.3	20.7	24.3	33.4	34.0	47.7	70.2	
					8 MHz	8.3	13.6	17.2	26.2	26.6	40.3	62.7	
		HXTAL_bypass = 8 MHz, PLL on, System clock = f_{HCLK1}	All enabled		216 MHz	157.5	165.7	169.8	180.3	203.6	217.3	241.3	
					170 MHz	120.0	126.8	130.5	139.9	156.2	168.3	189.8	
					120 MHz	86.8	93.2	96.9	106.1	116.4	128.9	150.6	
					80 MHz	60.1	66.1	69.8	78.9	84.8	97.8	120.1	
					32 MHz	27.8	33.5	37.1	46.1	47.9	61.6	84.0	
					8 MHz	11.4	16.8	20.4	29.4	30.1	43.9	66.2	
		HXTAL_bypass = 8 MHz, PLL on, System clock = f_{HCLK1}	All disabled	SRAM	216 MHz	63.4	69.9	74.1	85.0	90.2	104.1	130.0	
					170 MHz	49.4	55.0	58.8	68.7	71.7	84.7	108.2	
					120 MHz	36.7	42.3	46.1	55.9	57.3	70.6	94.3	
					80 MHz	26.6	32.1	35.8	45.6	45.9	59.5	83.3	
					32 MHz	14.4	19.7	23.5	33.3	32.8	46.5	70.3	
					8 MHz	8.1	13.3	17.1	26.8	26.1	39.7	63.5	
		HXTAL_bypass = 8 MHz, PLL on, System clock = f_{HCLK1}	All enabled		216 MHz	151.0	159.0	163.3	174.7	195.3	209.0	233.1	
					170 MHz	115.3	122.0	125.9	136.1	150.2	162.4	184.4	
					120 MHz	83.4	89.7	93.6	103.6	112.0	124.6	147.2	
					80 MHz	57.8	63.8	67.6	77.5	81.7	94.7	117.9	
					32 MHz	26.9	32.5	36.3	46.0	46.5	60.2	83.8	
					8 MHz	11.2	16.5	20.2	29.9	29.4	43.2	66.8	

(1) Value guaranteed by characterization, not 100% tested in production.

(2) During power consumption test, GPIO needs to be configure as Analog Input mode.

Table 4-8. Power consumption in Run mode with different codes(1)(2)(3)(4)

Symbol	Description	Conditions			Typ	Unit	Typ	Unit
		General	Execute from	Code				
I_{SUM}	Sum of supply current from VDD and VDDA	HXTAL_bypass = 8 MHz, PLL on, System clock = 216 MHz, f_{HCLK1} = 216 MHz, All peripherals disabled	EFLASH	Coremark	70.32	mA	0.326	mA /MHz
			SRAM	Coremark	66.83		0.309	
		HXTAL_bypass = 8 MHz, PLL on, System clock = 170 MHz, f_{HCLK1} = 170 MHz, All peripherals disabled	EFLASH	Coremark	58.89		0.346	
			SRAM	Coremark	53.90		0.317	

(1) Value guaranteed by characterization, not 100% tested in production.
(2) During power consumption test, GPIO needs to be configure as Analog Input mode.
(3) The pre-fetch buffer is enabled when fetching from EFLASH.
(4) Code compiled with high optimization for space in SRAM.

Table 4-9. Power consumption in Sleep mode(1)(2)(3)

Symbol	Description	Conditions			Typ				Max			Unit
		General	peripherals	f_{HCLK1}	25°C	85°C	105°C	125°C	85°C	105°C	125°C	
I_{SUM}	Sum of supply current from VDD and VDDA (Sleep mode)	HXTAL_bypass = 8 MHz, PLL on	All peripheral disabled	216 MHz	48.7	55.1	59.1	69.0	74.1	89.0	113.7	mA
				170 MHz	39.8	46.2	50.2	60.2	63.9	79.1	103.8	
				120 MHz	30.1	36.4	40.4	50.3	53.0	68.4	93.0	
				80 MHz	22.3	28.5	32.5	42.4	44.3	59.8	84.5	
				32 MHz	12.8	18.9	23.0	32.9	34.2	49.8	74.3	
				8 MHz	7.9	14.0	18.0	27.9	28.9	44.5	68.9	
		HXTAL_bypass = 8 MHz, PLL on	All peripheral enabled	216 MHz	136.4	144.3	148.4	158.8	178.4	192.4	216.4	
				170 MHz	109.0	116.6	120.7	131.0	145.4	159.7	184.6	
				120 MHz	79.0	86.2	90.3	100.5	109.6	124.3	149.1	
				80 MHz	54.9	61.8	65.9	76.0	81.4	96.5	121.3	
				32 MHz	26.0	32.4	36.4	46.4	48.5	64.2	88.8	
				8 MHz	11.1	17.3	21.3	31.2	32.4	48.1	72.6	

(1) Value guaranteed by characterization, not 100% tested in production.
(2) When analog peripheral blocks such as ADCs, DACs, HXTAL, LXTAL, IRC48M, or IRC32K are ON, an additional power consumption should be considered.
(3) During power consumption test, GPIO needs to be configure as Analog Input mode.

Table 4-10. Power consumption in Deep-sleep mode (1)(2)

Symbol	Description	Conditions		Typ(3)				Max			Unit
		General	V_{DD}	25°C	85°C	105°C	125°C	85°C	105°C	125°C	
I_{SUM}	Sum of supply current from VDD and VDDA (Deep-sleep mode)	LDO in normal mode, IRC32K off, RTC off	1.71V	5.15	9.30	12.41	19.49	19.42	29.03	50.82	mA
			3.3V	5.18	9.38	12.44	19.55	19.50	29.08	50.91	
			3.6V	6.88	10.96	13.97	21.05	20.99	30.57	52.38	
		LDO in Low power mode, IRC32K off, RTC off	1.71V	5.08	9.23	12.28	19.31	19.27	28.83	50.43	
			3.3V	5.10	9.27	12.31	19.37	19.33	28.88	50.49	
			3.6V	6.75	10.81	13.81	20.84	20.79	30.31	51.92	

(1) Value guaranteed by characterization, not 100% tested in production.
(2) During power consumption test, GPIO needs to be configure as Analog Input mode.
(3) V_{CORE} = 1.0V.

Table 4-11. Power consumption in Standby mode (1)

Symbol	Description	Conditions		Typ				Max			Unit
		General	V_{DD}	25°C	85°C	105°C	125°C	85°C	105°C	125°C	
I_{SUM}	Sum of supply current from VDD and VDDA (Standby mode)	LXTAL off, IRC32K on, RTC on	1.71V	1.22	2.12	3.77	8.62	2.76	4.74	10.90	µA
			3.3V	2.19	3.92	6.23	12.46	4.61	7.20	14.69	
			3.6V	2.52	4.92	7.81	14.97	5.99	9.27	17.34	
		LXTAL off, IRC32K on, RTC off	1.71V	1.10	2.03	3.66	8.56	2.66	4.64	10.89	
			3.3V	1.95	3.69	6.03	12.32	4.40	6.99	14.60	
			3.6V	2.27	4.67	7.57	14.78	5.77	9.04	17.16	
		LXTAL off, IRC32K off, RTC off	1.71	0.92	1.86	3.53	6.03	2.51	4.52	10.91	
			3.3V	1.73	3.51	5.90	12.41	4.23	6.87	14.85	
			3.6V	1.91	4.34	7.27	14.63	5.45	8.72	17.06	

(1) Value guaranteed by characterization, not 100% tested in production.

Table 4-12. Power consumption in BKP_ONLY mode(1)(2)

Symbol	Description	Conditions		Typ				Unit
		General	V_{BAT}	25°C	85°C	105°C	125°C	
I_{BAT}	RTC current from VBAT, LXTAL at 32768Hz	VDD off, RTC on	1.71V	0.78	1.02	1.35	2.03	μA
			3.3V	1.01	1.34	1.76	2.61	
			3.6V	1.11	1.52	2.01	2.98	

(1) Value guaranteed by sample, not 100% tested in production.

(2) LSE high driving.

4.6. EMC characteristics

System level ESD (Electrostatic discharge, according to IEC 61000-4-2) and EFT (Electrical Fast Transient/burst, according to IEC 61000-4-4) testing result is given in the ***Table 4-13. System level ESD and EFT characteristics(1)***. System level ESD is for end-customer operation, it includes ESD field events on system level occur in an unprotected area (outside EPA). System level ESD protection necessary to satisfy higher ESD levels.

Table 4-13. System level ESD and EFT characteristics(1)

Symbol	Description	Conditions	Package	Class	Level
V_{ESD}	Contact / Air mode high voltage stressed on all I/O pins	V_{DD}=3.3 V, T_J=25 °C f_{HCLK} = 216 MHz IEC 61000-4-2	LQFP128	CD 8kV AD 15kV	4A
			LQFP48	CD 8kV AD 15kV	4A
V_{EFT}(2)	Fast transient high voltage burst stressed on Power and GND	V_{DD}=3.3 V, T_J=25 °C f_{HCLK} = 216 MHz IEC 61000-4-4	LQFP128	4kV	4A
			LQFP48	4kV	4A

(1) Value guaranteed by characterization, not 100% tested in production.

(2) EFT test can pass 5kV.

EMI (Electromagnetic Interference) emission test result is given in the ***Table 4-14. EMI characteristics***, The electromagnetic field emitted by the device are monitored while an application, executing EEMBC code, is running. The test is compliant with SAE J1752-3:2017 standard which specifies the test board and the pin loading.

Table 4-14. EMI characteristics(1)

Symbol	Parameter	Conditions	Package	Tested frequency band	Max vs. [f_{HXTAL}/f_{HCLK}]	Unit
					8/216 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_J=25 °C f_{HCLK} = 216 MHz, conforms to SAE J1752-3:2017	LQFP128	0.15 MHz to 30 MHz	-4.64	dBμV
				30 MHz to 130 MHz	2.44	
				130 MHz to 1 GHz	4.56	
			LQFP48	0.15 MHz to 30 MHz	-7.12	

Symbol	Parameter	Conditions	Package	Tested frequency band	Max vs. [f_{HXTAL}/f_{HCLK}]	Unit
					8/216 MHz	
				30 MHz to 130 MHz	1.44	
				130 MHz to 1 GHz	4.88	

(1) Value guaranteed by characterization, not 100% tested in production.

Component level ESD include HBM (Human body model, according to ANSI/ESDA/JEDEC JS-001) and CDM (ANSI/ESDA/JEDEC JS-002), that ESD field events during manufacturing in an ESD protected area, such as PCB assembly/repair, IC assembly/test and Fab environment. The ESD protected area (EPA) has many measures, for instance ESD protective packaging, grounding person wrist strap to ground (or flooring/footwear), grounded work surface and ionizer.

Static latch-up (LU, according to JEDEC78) test is based on the two measurement methods, I/O current injection value (I-test) and power supply over-voltage value.

Table 4-15. Component level ESD and latch-up characteristics(1)

Symbol	Description	Conditions	Package	Max	Unit	Level
V_{HBM}	Human body model electrostatic discharge voltage (Any pin combination)	T_J = 25 °C JS-001-2017	LQFP128	2000	V	2
V_{CDM}	Charge device model electrostatic discharge voltage (All pins)	T_J = 25 °C JS-002-2018	LQFP128	500	V	C2a
LU	I-test	T_A = 125 °C JESD78F	LQFP128	200	mA	Class II Level A
	V_{supply} over voltage			5.4	V	

(1) Value guaranteed by characterization, not 100% tested in production.

4.7. Power supply supervisor characteristics

Table 4-16. Power supply supervisor characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{LVD}	Low voltage Detector level selection	LVDT[2:0] = 000(rising edge)	—	2.15	—	V
		LVDT[2:0] = 000(falling edge)	—	2.05	—	
		LVDT[2:0] = 001(rising edge)	—	2.30	—	
		LVDT[2:0] = 001(falling edge)	—	2.20	—	
		LVDT[2:0] = 010(rising edge)	—	2.45	—	
		LVDT[2:0] = 010(falling edge)	—	2.35	—	
		LVDT[2:0] = 011(rising edge)	—	2.60	—	
		LVDT[2:0] = 011(falling edge)	—	2.50	—	
		LVDT[2:0] = 100(rising edge)	—	2.75	—	

Symbol	Description	Conditions	Min	Typ	Max	Unit
		LVDT[2:0] = 100(falling edge)	—	2.65	—	
		LVDT[2:0] = 101(rising edge)	—	2.90	—	
		LVDT[2:0] = 101(falling edge)	—	2.80	—	
		LVDT[2:0] = 110(rising edge)	—	3.00	—	
		LVDT[2:0] = 110(falling edge)	—	2.90	—	
$V_{LVDhyst}$	LVD hysteresis	—	—	100	—	mV
V_{POR}	Power on reset threshold	—	—	1.63	—	V
V_{PDR}	Power down reset threshold	—	—	1.61	—	V
$V_{PDRhyst}$	PDR hysteresis	—	—	20	—	mV
V_{BOR}	Brownout level selection	BOR_TH[1:0] = 01(rising edge)	—	2.3	—	V
		BOR_TH[1:0] = 01(falling edge)	—	2.2	—	
		BOR_TH[1:0] = 10(rising edge)	—	2.6	—	
		BOR_TH[1:0] = 10(falling edge)	—	2.5	—	
		BOR_TH[1:0] = 11(rising edge)	—	2.9	—	
		BOR_TH[1:0] = 11(falling edge)	—	2.8	—	
$V_{BORhyst}$	BOR hysteresis	—	—	100	—	mV
$t_{RSTTEMPO}$	Reset temporization	—	—	254	—	us
V_{AVD}	Analog voltage detector for V_{DDA} level selection	VAVDVC[1:0] = 00(rising edge)	—	1.8	—	V
		VAVDVC[1:0] = 00(falling edge)	—	1.7	—	
		VAVDVC[1:0] = 01(rising edge)	—	2.2	—	
		VAVDVC[1:0] = 01(falling edge)	—	2.1	—	
		VAVDVC[1:0] = 10(rising edge)	—	2.6	—	
		VAVDVC[1:0] = 10(falling edge)	—	2.5	—	
		VAVDVC[1:0] = 11(rising edge)	—	2.9	—	
		VAVDVC[1:0] = 11(falling edge)	—	2.8	—	
V_{hyst_AVD}	Hysteresis of V_{DDA} voltage detector	—	—	100	—	mV
V_{OVD}	Analog voltage detector for $V_{1.1V}$ over level selection	VOVDVC[1:0] = 00(rising edge)	—	1.25	—	V
		VOVDVC[1:0] = 00(falling edge)	—	1.225	—	
		VOVDVC[1:0] = 01(rising edge)	—	1.35	—	
		VOVDVC[1:0] = 01(falling edge)	—	1.325	—	
		VOVDVC[1:0] = 10(rising edge)	—	1.45	—	

Symbol	Description	Conditions	Min	Typ	Max	Unit
		VOVDVC[1:0] = 10(falling edge)	—	1.425	—	
		VOVDVC[1:0] = 11(rising edge)	—	1.55	—	
		VOVDVC[1:0] = 11(falling edge)	—	1.525	—	
V_{hyst_OVD}	Hysteresis of $V_{1.1V}$ over voltage detector	—	—	25	—	mV
V_{UVD}	Analog voltage detector for $V_{1.1V}$ under level selection	VUVDVC[1:0] = 00(rising edge)	—	0.975	—	V
		VUVDVC[1:0] = 00(falling edge)	—	0.95	—	
		VUVDVC[1:0] = 01(rising edge)	—	0.875	—	
		VUVDVC[1:0] = 01(falling edge)	—	0.85	—	
		VUVDVC[1:0] = 10(rising edge)	—	0.775	—	
		VUVDVC[1:0] = 10(falling edge)	—	0.75	—	
		VUVDVC[1:0] = 11(rising edge)	—	0.675	—	
		VUVDVC[1:0] = 11(falling edge)	—	0.65	—	
V_{hyst_UVD}	Hysteresis of $V_{1.1V}$ voltage under detector	—	—	25	—	mV

(1) Value guaranteed by design, not 100% tested in production.

4.8. Voltage reference buffer characteristics

Table 4-17. Voltage reference buffer characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Supply voltage	Normal mode, V_{DDA}=3.3V	VREFS = 00	2.4	3.3	3.6	V
			VREFS = 01	2.8	3.3	3.6	
			VREFS = 10	3.135	3.3	3.6	
		Degraded mode(3)	VREFS = 00	1.65	—	2.4	
			VREFS = 01	1.65	—	2.8	
			VREFS = 10	1.65	—	3.135	
V_{REFBUF_OUT}	Voltage Reference Buffer Output	Normal mode, at 3.3V, -40~105°C for grade 7 devices	VREFS = 00	2.018(2)	2.048	2.078(2)	
			VREFS = 01	2.47(2)	2.5	2.53(2)	
			VREFS = 1X	2.87(2)	2.9	2.93(2)	
		Normal mode, at 3.3V, -40~125°C for grade 3 devices	VREFS = 00	2.018(2)	2.048	2.078(2)	
			VREFS = 01	2.47(2)	2.5	2.53(2)	
			VREFS = 1X	2.87(2)	2.9	2.93(2)	
		Degraded mode(3)	VREFS = 01	V_{DDA} - 0.27	—	V_{DDA}	
TRIM	Trim step resolution	—		—	0.11	0.13	%
C_L	Load capacitor	—		0.5	1	1.5	μF

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ESR	Equivalent Serial Resistor of CL	—		—	—	2	Ω
I_{LOAD}	Load current	—		—	—	6.5	mA
t_{START}	Start-up time	C_L=0.5 µF		—	751	—	µs
		C_L=1 µF		—	751	—	
		C_L=1.5 µF		—	751	—	
I_{DDA} (V_{REFBUF})	V_{REFBUF} consumption from V_{DDA}	I_{LOAD} = 0 µA		—	29	34.2	µA
		I_{LOAD} = 500 µA		—	29	34.2	
		I_{LOAD} = 4 mA		—	29	34.2	
I_{INRUSH}(4)	Control of maximum DC current drive on V_{REFBUF_OUT} during startup phase	—		—	12.6	—	mA
$Regu_{(LINE)}$(5)	Line regulation	I_{load} = 500 µA		—	450	—	ppm /V
		I_{load} = 4 mA		—	480	—	
$Regu_{(LOAD)}$	Load regulation	500 µA ≤ I_{LOAD} ≤ 4 mA	Normal mode	—	24	—	ppm / mA
T_{COEFF}	Temperature drift	−40 °C < T_J < +135 °C		—	—	60(6)	ppm / °C
PSRR	Power supply rejection	DC	—	—	60	—	dB
		100kHz	—	—	45	—	

(1) Value guaranteed by design, not 100% tested in production.

(2) Value guaranteed by characterization, not 100% tested in production.

(3) In degraded mode, the voltage reference buffer can not maintain accurately the output voltage which follows (VDDA – drop voltage).

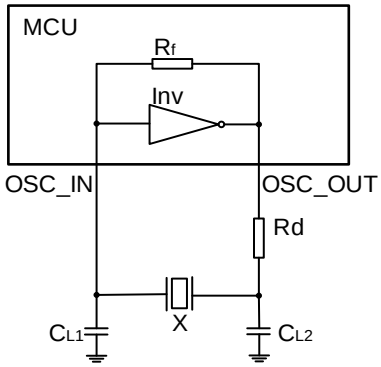
(4) To correctly control V_{REFBUF} inrush current during start-up phase and scaling change, the V_{DDA} voltage should be in the range (2.4 V to 3.6 V) for VREFS = 00, (2.8V to 3.6 V) for VREFS = 01, (3.135V to 3.6 V) for VREFS = 1X.

(5) Line regulation is given for overall supply variation, in normal mode.

(6) The value represents the total VRREFBUF combined temperature drift caused by all modules, with the temperature drift caused by VREFBUF being 15 ppm / °C.

4.9. External clock characteristics

Figure 4-3. Internal structure diagram of OSCIN and OSCOUT pin



It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine which load capacitors will best tune their resonator/crystal to the microcontroller device for optimum start-up and operation over temperature/voltage extremes.

Table 4-18. High speed external clock (HXTAL) generated from a crystal/ceramic characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{HXTAL}	Crystal or ceramic frequency	1.71 V ≤ V_{DD} ≤ 3.6 V	4	8	48	MHz
R_F	Feedback resistor	V_{DD} = 3.3 V	—	400	—	kΩ
C_{HXTAL}(2)	Recommended load capacitance on OSCIN and OSCOUT	—	—	20	30	pF
$Ducy_{(HXTAL)}$	Crystal or ceramic duty cycle	—	30	50	70	%
g_m(3)	Oscillator transconductance	Startup	—	30	—	mA/V
$I_{DDHXTAL}$	Crystal or ceramic operating current	V_{DD} = 3.3 V Rm=30 Ω, CL=10 pF, f_{HCLK} = f_{IRC8M} = 8 MHz	—	0.55	—	mA
$t_{START(HXTAL)}$	Crystal or ceramic startup time	V_{DD} = 3.3 V, f_{HCLK} = f_{IRC8M} = 8 MHz	—	2	—	ms

(1) Value guaranteed by design, not 100% tested in production.

(2) C_{HXTAL1} = C_{HXTAL2} = 2*(C_{LOAD} - C_S), For C_{HXTAL1} and C_{HXTAL2}, it is recommended matching capacitance on OSCIN and OSCOUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

(3) More details about g_m could be found in ***AN052 GD32 MCU Resonator-Based Clock Circuits***.

Table 4-19. High speed external clock characteristics (HXTAL in bypass mode) (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{HXTAL_ext}	External clock source or oscillator frequency	1.71 V ≤ V_{DD} ≤ 3.6 V	1	—	50	MHz
V_{HXTALH}	OSCIN input pin high level voltage	V_{DD} = 3.3 V	0.7 V_{DD}	—	V_{DD}	V
V_{HXTALL}	OSCIN input pin low level voltage		V_{SS}	—	0.3 V_{DD}	V
$t_{H/L(HXTAL)}$	OSCIN high or low time	—	5	—	—	ns
$t_{R/F(HXTAL)}$	OSCIN rise or fall time	—	—	—	10	ns
C_{IN}	OSCIN input capacitance	—	—	5	—	pF
$Ducy_{(HXTAL)}$	Duty cycle	—	40	—	60	%

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-4. High-speed external clock source AC timing diagram

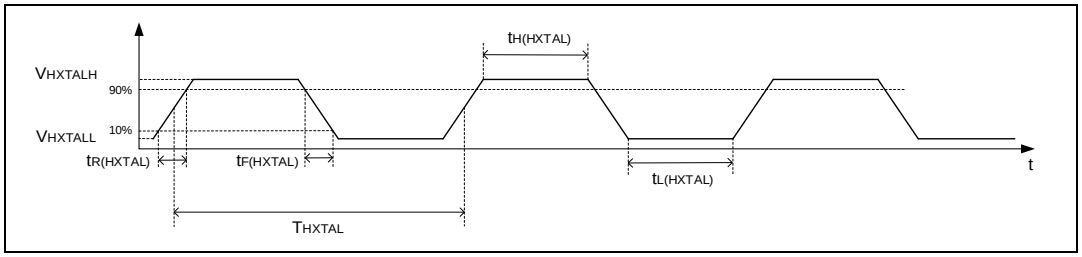


Table 4-20. Low speed external clock (LXTAL) generated from a crystal/ceramic characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{LXTAL}	Crystal or ceramic frequency	V_{DD} = 3.3 V	—	32.768	—	kHz
C_{LXTAL}(2)	Recommended matching capacitance on OSC32IN and OSC32OUT	—	—	10	—	pF
$Ducy_{(LXTAL)}$	Crystal or ceramic duty cycle	—	30	—	70	%
g_m(3)	Oscillator transconductance	Low driving capability	—	5.8	—	μA/V
		Medium driving capability	—	9.1	—	
		Higher driving capability	—	12	—	
$I_{DDLXTAL}$	Crystal or ceramic operating current	LXTALDRI[1:0] = 01	—	500	—	nA
		LXTALDRI[1:0] = 10	—	670	—	
		LXTALDRI[1:0] = 11	—	790	—	
$t_{START(LXTAL)}$	Crystal or ceramic startup time	—	—	2	—	s

(1) Value guaranteed by design, not 100% tested in production.

(2) $C_{LXTAL1} = C_{LXTAL2} = 2*(C_{LOAD} - C_S)$, For C_{LXTAL1} and C_{LXTAL2}, it is recommended matching capacitance on OSC32IN and OSC32OUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

(3) More details about g_m could be found in ***AN052 GD32 MCU Resonator-Based Clock Circuits***.

Table 4-21. Low speed external user clock characteristics (LXTAL in bypass mode) (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{LXTAL_ext}	External clock source or oscillator frequency	V_{DD} = 3.3 V	—	32.768	1000	kHz
V_{LXTALH}	OSC32IN input pin high level voltage	—	0.7 V_{DD}	—	V_{DD}	V
V_{LXTALL}	OSC32IN input pin low level voltage	—	V_{SS}	—	0.3 V_{DD}	
$t_{H/L(LXTAL)}$	OSC32IN high or low time	—	450	—	—	ns
$t_{R/F(LXTAL)}$	OSC32IN rise or fall time	—	—	—	50	
C_{IN}	OSC32IN input capacitance	—	—	5	—	pF
$Ducy_{(LXTAL)}$	Duty cycle	—	30	50	70	%

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-5. Low-speed external clock source AC timing diagram

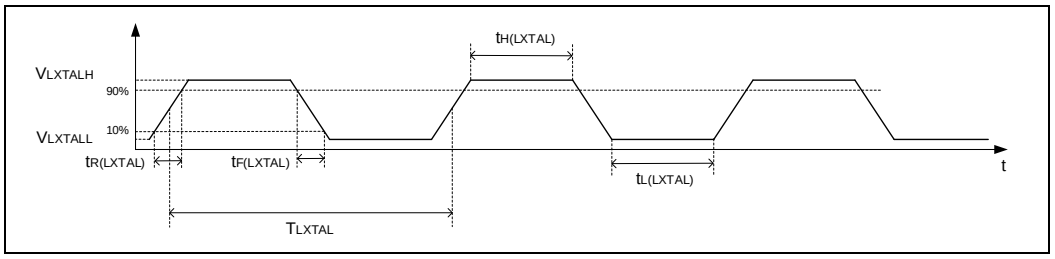
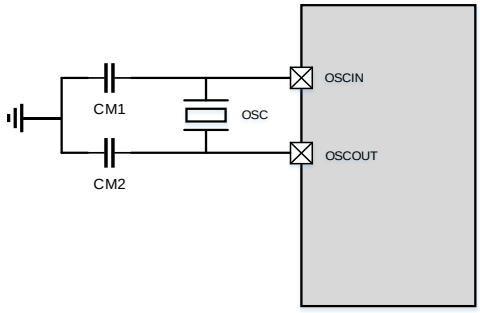


Figure 4-6. Recommended external OSCIN and OSCOUT pins circuit for crystal



4.10. Internal clock characteristics

Table 4-22. High speed internal clock (IRC8M) characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{IRC8M}	High Speed Internal Oscillator (IRC8M) frequency	V_{DD} = V_{DDA} = 3.3 V	—	8	—	MHz
$Drift_{IRC8M}$	IRC8M oscillator Frequency drift, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +105 °C for grade 7 devices	-2.5(2)	—	2.5(2)	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +125 °C for grade 3 devices	-2.5(2)	—	2.5(2)	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C	-1.5(3)	—	1.5(3)	%
	IRC8M oscillator Frequency drift, User trimming step	—	—	0.3	—	%
$Ducy_{IRC8M}$	IRC8M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V	45	50	55	
Δ_{VDD}(IRC8M)	IRC8M oscillator frequency drift over V_{DD}	V_{DD}=1.71 V to 3.6 V	-0.5(2)	—	0.5(2)	
$I_{DDA(IRC8M)}$	IRC8M oscillator operating current	V_{DD} = V_{DDA} = 3.3 V	36	70	85	μA
$t_{START(IRC8M)}$	IRC8M oscillator startup time	V_{DD} = V_{DDA} = 3.3 V	1.1	1.2	1.7	μs
$t_{stab(IRC8M)}$	IRC8M oscillator stabilization time	V_{DD} = V_{DDA} = 3.3 V	—	1.2	1.7	

(1) Value guaranteed by design, not 100% tested in production.
(2) Value guaranteed by characterization, not 100% tested in production.
(3) Value guaranteed by production.

Table 4-23. Low speed internal clock (IRC32K) characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{IRC32K}	Low Speed Internal oscillator (IRC32K) frequency	V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C	30(2)	32.0(1)	34(2)	kHz
		T_A = -40 to 105 °C for grade 7 devices	28(2)	—	36(2)	
		T_A = -40 to 125 °C for grade 3 devices	28(2)	—	36(2)	
$I_{DDAIRC32K}$(1)	IRC32K oscillator operating current	V_{DD} = V_{DDA} = 3.3 V, f_{HCLK} = f_{HXTAL_PLL} = 180 MHz	—	0.33	—	μA
$t_{START(IRC32K)}$(1)	IRC32K oscillator startup time	V_{DD} = V_{DDA} = 3.3 V, f_{HCLK} = f_{HXTAL_PLL} = 180 MHz	—	34	—	μs
$t_{STAB(IRC32K)}$(1)	IRC32K oscillator stabilization time	5% of final frequency	—	32	87	μs

(1) Value guaranteed by design, not 100% tested in production.
(2) Value guaranteed by characterization, not 100% tested in production.

4.11. PLL characteristics

Table 4-24. PLL characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	PLL supply voltage of HV	—	1.71	3.3	3.6	V
f_{PLL_IN}(2)	PLL input clock frequency	—	2.66	—	16	MHz
f_{PLL_OUT}	PLL output clock frequency	—	96	—	480	MHz
f_{VCO_OUT}	PLL VCO output clock frequency	—	96	—	480	MHz
$f_{PLL\_OUT\_duty\ cycle}$	Dutycycle PLL output clock frequency	—	45	—	55	%
t_{LOCK}	PLL lock time	—	—	—	400	μs
Jitter(2)	RMS cycle-to-cycle Jitter	PLL VCO clock 300 MHz	—	20.2	—	ps
	RMS period Jitter		—	15.1	—	
I_{DD}	Current consumption on V_{DD}	PLL VCO clock 480 MHz	—	570	—	μA
		PLL VCO clock 96 MHz	—	182	—	

(1) Value guaranteed by design, not 100% tested in production.
(2) The input reference clock frequency of the pre divided PLL.

4.12. Memory characteristics

Table 4-25. Flash memory characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
$I_{DD(FLASH)}$	Max supply current from V_{DD} during FLASH operation	Erasing	—	—	4.8	mA
		Programming	—	—	3.8	
PE_{CYC}(2)	Number of guaranteed program /erase cycles before	T_A range(3)	100	—	—	kcycles

Symbol	Description	Conditions	Min	Typ	Max	Unit
	failure (Endurance)					
t_{RET}(2)	Data retention time	T_A = 85°C after up to 0 kcycle(4)	25	—	—	years
		T_A = 85°C after up to 10 kcycles(4)	15	—	—	
		T_A = 55℃ after up to 10 kcycles(4)	30	—	—	
t_{PROG}	Double word programming time	—	—	80	—	μs
t_{PROG_PAGE}	One page (2 Kbytes) programming time	Normal programming	—	20	—	ms
t_{PROG_BANK}	One bank (256 Kbyte) programming time	Normal programming	—	2621	—	
t_{ERASE}	Page erase time	—	1	—	20	
t_{MERASE}	Mass erase time	—	—	—	20	

(1) Value guaranteed by design, not 100% tested in production.
(2) Value guaranteed by characterization, not 100% tested in production.
(3) For grade 7 devices, T_A range = -40°C ~+105°C. For grade 3 devices, T_A range = -40°C ~+125°C.
(4) Cycling performed over the whole temperature range

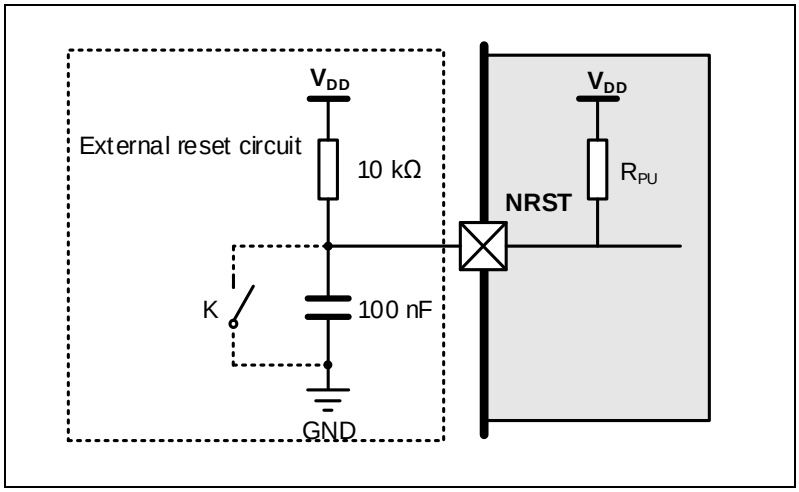
4.13. NRST pin characteristics

Table 4-26. NRST pin characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST Input low level voltage	—	—	—	0.3 V_{DD}	V
$V_{IH(NRST)}$	NRST Input high level voltage		0.7 V_{DD}	—	—	
V_{hyst}	Schmidt trigger Voltage hysteresis	V_{DD} = V_{DDA} = 1.71 V	—	383	—	mV
		V_{DD} = V_{DDA} = 3.3 V	—	540	—	
		V_{DD} = V_{DDA} = 3.6 V	—	570	—	
t_{NRST_F}	Generated filtered reset pulse duration	—	—	—	100	ns
t_{NRST_NF}	Generated not filtered reset pulse duration	—	350	—	—	

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-7. Recommended external NRST pin circuit(1)



(1) Unless the voltage on NRST pin go below $V_{IL(NRST)}$ level, the device would not generate a reliable reset.

4.14. GPIO current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below VSS or above VDD (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures. The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the -5 μA/+0 μA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Table 4-27. GPIO current injection susceptibility(1)

Symbol	Description		Functional susceptibility		Unit
			Negative injection	Positive injection	
I_{INJ}(1)	Injected current on pin	Input current on 5V tolerant pin	-5	NA	mA
		Input current on other I/O(Except BOOT0)	-5	0	
		BOOT0	0	NA	

(1) Value guaranteed by design, not 100% tested in production.

4.15. GPIO characteristics

More details about GPIO could be found in ***AN092 GD32 MCU GPIO structure and precautions***.

Table 4-28. I/O static characteristics

Symbol	Description		Conditions	Min	Typ	Max	Unit
V_{IL}(1)	Standard IO Low level input voltage		1.71 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	—	—	0.39 V_{DD} - 0.06	V
	5V-tolerant IO Low level input voltage		1.71 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	—	—	0.39 V_{DD} - 0.06	V
V_{IH}(1)	Standard IO High level input voltage		1.71 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	0.49 V_{DD} + 0.26	—	—	V
	5V-tolerant IO High level input voltage		1.71 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	0.49 V_{DD} + 0.26	—	—	V
V_{HYS}(1)	Input hysteresis		1.71 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	—	510	—	mV
I_{LEAK}	Standard IO input leakage current		V_{SS} ≤ V_{IN} ≤ V_{DD}	-2(2)	—	2(2)	uA
	5V-tolerant IO input leakage current		V_{IN} = 5 V	-2.5(1)	—	2.5(1)	
R_{PU}(1)	Internal pull-up resistor	All pins	—	—	40	—	kΩ
R_{PD}(1)	Internal pull-down resistor	All pins	—	—	40	—	kΩ
C_{IO}(1)	I/O pin capacitance		I/O pin capacitance	—	5	—	pF

(1) Value guaranteed by design, not 100% tested in production.

(2) Value guaranteed by production.

Table 4-29. Output voltage characteristics for all I/Os except PC13, PC14, PC15 (1)(2)

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{OL} (IO_speed = 12MHz)	Low level output voltage for an IO Pin (I_{IO} = +1 mA)	V_{DD} = 1.71 V	0.09	0.11	0.12	V
		V_{DD} = 3.3 V	0.06	0.07	0.08	
		V_{DD} = 3.6 V	0.06	0.07	0.08	
	Low level output voltage for an IO Pin (I_{IO} = +4 mA)	V_{DD} = 3.3 V	0.24	0.27	0.32	
		V_{DD} = 3.6 V	0.23	0.27	0.31	
V_{OH} (IO_speed = 12MHz)	High level output voltage for an IO Pin (I_{IO} = +1 mA)	V_{DD} = 1.71 V	1.49	1.57	1.59	V
		V_{DD} = 3.3 V	3.17	3.22	3.23	
		V_{DD} = 3.6 V	3.48	3.52	3.53	
	High level output voltage for an IO Pin (I_{IO} = +4 mA)	V_{DD} = 3.3 V	2.92	2.97	3.00	
		V_{DD} = 3.6 V	3.24	3.29	3.32	
V_{OL}	Low level output	V_{DD} = 1.71 V	0.14	0.19	0.23	V

Symbol	Description	Conditions	Min	Typ	Max	Unit
(IO_speed = 60MHz)	voltage for an IO Pin (I_{IO} = +4 mA)	V_{DD} = 3.3 V	0.09	0.13	0.17	
		V_{DD} = 3.6 V	0.09	0.13	0.17	
	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 3.3 V	0.18	0.25	0.33	
		V_{DD} = 3.6 V	0.17	0.25	0.33	
	Low level output voltage for an IO Pin (I_{IO} = +15 mA)	V_{DD} = 3.3 V	0.34	0.48	0.64	
		V_{DD} = 3.6 V	0.33	0.47	0.64	
V_{OH} (IO_speed = 60MHz)	High level output voltage for an IO Pin (I_{IO} = +4 mA)	V_{DD} = 1.71 V	1.42	1.47	1.60	V
		V_{DD} = 3.3 V	3.11	3.15	3.19	
		V_{DD} = 3.6 V	3.41	3.46	3.50	
	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 3.3 V	2.91	3.00	3.08	
		V_{DD} = 3.6 V	3.22	3.31	3.39	
	High level output voltage for an IO Pin (I_{IO} = +15 mA)	V_{DD} = 3.3 V	2.54	2.71	2.88	
		V_{DD} = 3.6 V	2.87	3.04	3.21	
V_{OL} (IO_speed = 85MHz)	Low level output voltage for an IO Pin (I_{IO} = +4 mA)	V_{DD} = 1.71 V	0.09	0.14	0.18	V
		V_{DD} = 3.3 V	0.06	0.10	0.14	
		V_{DD} = 3.6 V	0.06	0.10	0.14	
	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.71 V	0.19	0.30	0.39	
		V_{DD} = 3.3 V	0.13	0.20	0.28	
		V_{DD} = 3.6 V	0.12	0.20	0.28	
	Low level output voltage for an IO Pin (I_{IO} = +15 mA)	V_{DD} = 3.3 V	0.24	0.38	0.52	
		V_{DD} = 3.6 V	0.24	0.37	0.51	
V_{OH} (IO_speed = 85MHz)	High level output voltage for an IO Pin (I_{IO} = +4 mA)	V_{DD} = 1.71 V	1.49	1.53	1.61	V
		V_{DD} = 3.3 V	3.13	3.18	3.23	
		V_{DD} = 3.6 V	3.44	3.49	3.53	
	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.71 V	1.23	1.33	1.45	
		V_{DD} = 3.3 V	2.98	3.07	3.15	
		V_{DD} = 3.6 V	3.29	3.38	3.46	
	High level output voltage for an IO Pin (I_{IO} = +15 mA)	V_{DD} = 3.3 V	2.69	2.85	3.01	
		V_{DD} = 3.6 V	3.01	3.17	3.33	
V_{OL} (IO_speed = 100/220MHz)	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.71 V	0.14	0.22	0.30	V
		V_{DD} = 3.3 V	0.10	0.16	0.23	
		V_{DD} = 3.6 V	0.09	0.16	0.23	
	Low level output voltage for an IO Pin (I_{IO} = +10 mA)	V_{DD} = 1.71 V	0.18	0.28	0.38	
		V_{DD} = 3.3 V	0.12	0.20	0.29	
		V_{DD} = 3.6 V	0.12	0.20	0.29	
	Low level output	V_{DD} = 3.3 V	0.24	0.40	0.58	

Symbol	Description	Conditions	Min	Typ	Max	Unit
	voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 3.6 V	0.23	0.39	0.59	
V_{OH} (IO_speed = 100/220MHz)	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.71 V	1.35	1.43	1.53	
		V_{DD} = 3.3 V	3.03	3.12	3.19	
		V_{DD} = 3.6 V	3.34	3.42	3.50	
	High level output voltage for an IO Pin (I_{IO} = +10 mA)	V_{DD} = 1.71 V	1.25	1.36	1.62	
		V_{DD} = 3.3 V	2.97	3.07	3.16	
		V_{DD} = 3.6 V	3.27	3.38	3.47	
	High level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 3.3 V	2.62	2.83	3.02	
		V_{DD} = 3.6 V	2.95	3.15	3.33	

(1) Value guaranteed by characterization, not 100% tested in production.

(2) All pins except PC13 / PC14 / PC15. Since PC13 to PC15 are supplied through the Power Switch, which can only be obtained by a small current (typical source capability:3 mA shared between these IOs, but sink capability is same as other IO), the speed of GPIOs PC13 to PC15 should not exceed 2 MHz when they are in output mode (maximum load: 30 pF).

Table 4-30. I/O port AC characteristics(1)(2)(3)

Speed	Symbol	Description	Conditions	Min	Typ	Max	Unit
00	t_R/t_F	Output high to low level fall time and output low to high level rise time	2.5 ≤ V_{DD} ≤ 3.6 V, C_L = 10 pF	—	—	6.2	ns
			1.71 ≤ V_{DD} ≤ 2.5 V, C_L = 10 pF	—	—	9.7	
			2.5 ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF	—	—	14.1	
			1.71 ≤ V_{DD} ≤ 2.5 V, C_L = 30 pF	—	—	21.7	
			2.5 ≤ V_{DD} ≤ 3.6 V, C_L = 50 pF	—	—	22	
			1.71 ≤ V_{DD} ≤ 2.5 V, C_L = 50 pF	—	—	34	
01	t_R/t_F	Output high to low level fall time and output low to high level rise time	2.5 ≤ V_{DD} ≤ 3.6 V, C_L = 10 pF	—	—	2.6	ns
			1.71 ≤ V_{DD} ≤ 2.5 V, C_L = 10 pF	—	—	4.2	
			2.5 ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF	—	—	5.6	
			1.71 ≤ V_{DD} ≤ 2.5 V, C_L = 30 pF	—	—	9.1	
			2.5 ≤ V_{DD} ≤ 3.6 V, C_L = 50 pF	—	—	8.5	
			1.71 ≤ V_{DD} ≤ 2.5 V, C_L = 50 pF	—	—	13.9	
10	t_R/t_F	Output high to low level fall time and output low to high level rise time	2.5 ≤ V_{DD} ≤ 3.6 V, C_L = 10 pF	—	—	2.0	ns
			1.71 ≤ V_{DD} ≤ 2.5 V, C_L = 10 pF	—	—	3.3	
			2.5 ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF	—	—	4.0	
			1.71 ≤ V_{DD} ≤ 2.5 V, C_L = 30 pF	—	—	6.6	
			2.5 ≤ V_{DD} ≤ 3.6 V, C_L = 50 pF	—	—	6.3	
			1.71 ≤ V_{DD} ≤ 2.5 V, C_L = 50 pF	—	—	10.0	
11	t_R/t_F	Output high to low level fall time and output low to high level rise time	2.5 ≤ V_{DD} ≤ 3.6 V, C_L = 10 pF	—	—	1.5	ns
			1.71 ≤ V_{DD} ≤ 2.5 V, C_L = 10 pF	—	—	2.5	
			2.5 ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF	—	—	2.9	
			1.71 ≤ V_{DD} ≤ 2.5 V, C_L = 30 pF	—	—	4.8	
			2.5 ≤ V_{DD} ≤ 3.6 V, C_L = 50 pF	—	—	4.4	
			1.71 ≤ V_{DD} ≤ 2.5 V, C_L = 50 pF	—	—	7.2	

(1) The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.
(2) Value guaranteed by design, not 100% tested in production.
(3) The data is for reference only, and the specific values are related to PCB Layout.

4.16. High-precision temperature sensor characteristics

Table 4-31. High-precision temperature sensor characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{25}	Uncalibrated Offset	T_J = 25 °C	—	1012	—	mV
E_{OFF}	Uncalibrated Offset Error	T_J = 25 °C	—	±4.2	—	mV
Avg_Slope	Average slope	—	—	3.2	—	mV/°C
E_M	Slope Error	—	—	35	—	μV/°C
LIN	Linearity	T_J = -40 °C to 135 °C	—	1.6	—	°C
t_{s_temp}	ADC sampling time when reading the temperature	—	10	—	—	μs
t_{ON}	Turn-on Time	f_{ADC} = 5 MHz, t_{s_temp} = 10 μs	—	37.8	—	μs
ETOT(2)(3)(4)	Temp Sensor Error Using Typical Slope and Factory-Calibrated Offset	T_J = -40 °C to 135 °C	—	-3 ~ 4	—	°C

(1) Value guaranteed by design, not 100% tested in production.
(2) The error is the average result of 100 times and represents the chip junction temperature error. The chip self-heating shall be considered when testing ambient temperature
(3) The error caused by ADC conversion and provided temperature calculation formula is not included.
(4) Note: ADC2 clock should not be configured greater than 5MHz and the sampling time should greater than ts_temp when use the high precision temperature sensor by ADC conversion.

Table 4-32. High-precision temperature sensor calibration values

Symbol	Parameter	Memory address
HPTS_CAL	High-precision temperature sensor raw data acquired value at 25°C(±3°C), V_{DD} = V_{DDA} = 3.3V(±14mV), V_{REFP} = 3.3 V(±0.6mV)	0x1FFFB3D8-0x1FFFB3D9

4.17. Temperature sensor characteristics

Table 4-33. Temperature sensor characteristics(1)

Symbol	Description	Min	Typ	Max	Unit
T_L	VSENSE linearity with temperature	—	±5	—	°C
Avg_Slope	Average slope	—	3.99	—	mV/°C
V_{25}	Voltage at 25 °C	—	1.25	—	V
t_{S_temp}(2)	ADC sampling time when reading the temperature	—	17.1	—	μs
$t_{START-RUN}$	Start-up time in Run mode (start-up of buffer)	—	5	8	
t_{START_CONT}(3)	Start-up time when entering in continuous mode	—	5	8	

Symbol	Description	Min	Typ	Max	Unit
$I_{DD(TS)}$	Temperature sensor consumption from VDD, when selected by ADC	—	8	11	uA

(1) Value guaranteed by design, not 100% tested in production.
(2) Shortest sampling time can be determined in the application by multiple iterations.
(3) Continuous mode means RUN mode or Temperature Sensor ON.

Table 4-34. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	Temperature sensor raw data acquired value at 25°C(±3°C), V_{DD} = V_{DDA} = 3.3V(±14mV), V_{REFP} = 3.3 V(±0.6mV)	0x1FFFB3F8-0x1FFFB3F9

4.18. ADC characteristics

Table 4-35. ADC characteristics(1)(3)

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage	—	1.71	3.3	3.6	V
V_{IN}	ADC input voltage range	—	0	—	V_{REFP}	V
V_{REFP}(2)	Positive Reference Voltage	V_{DDA} > 2.4 V	2	—	V_{DDA}	V
		V_{DDA} < 2.4 V	V_{DDA}			V
f_{ADC}	ADC clock	V_{DDA} = 1.71 V to 2.4 V	0.1	—	50	MHz
		V_{DDA} = 2.4 V to 3.6 V	0.1	—	80	MHz
f_S	Sampling rate	12-bit	—	—	5.33	MSPS
		10-bit	—	—	6.15	
		8-bit	—	—	7.27	
		6-bit	—	—	8.89	
V_{AIN}	Analog input voltage	42 external; 15 internal	0	—	V_{REFP}	V
R_{AIN}	External input impedance	See *Equation 1*	—	—	70.09	kΩ
R_{ADC}	Input sampling switch resistance	—	—	—	0.8	kΩ
C_{ADC}	Input sampling capacitance	No pin/pad capacitance included	—	—	2.87	pF
t_{CAL}	Calibration time	f_{ADC} = 80 MHz	—	902	—	1/ f_{ADC}
t_s	Sampling time	f_{ADC} = 80 MHz	2.5	—	640.5	1/ f_{ADC}
t_{CONV}	Total conversion time(including sampling time)	12-bit	—	12.5	—	1 / f_{ADC}
		10-bit	—	10.5	—	
		8-bit	—	8.5	—	
		6-bit	—	6.5	—	
t_{SU}	Startup time	—	—	—	1	µs
$I_{DDA\_D\ (ADC)}$	ADC consumption on V_{DDA} and V_{REF}, Differential mode	f_{ADC} = 80 MHz	—	1480.5	—	µA
$I_{DDA\_SE\ (ADC)}$	ADC consumption on V_{DDA} and V_{REF}, Single-ended	f_{ADC} = 80 MHz	—	1152.4	—	µA

Symbol	Description	Conditions	Min	Typ	Max	Unit
	mode					
$I_{DD\ (ADC)}$	ADC consumption on V_{DD} per f_{ADC}	—	—	24	—	μA/MHz

(1) Value guaranteed by design, not 100% tested in production.

(2) V_{REFP} should always be equal to or less than V_{DDA}, especially during power up.

(3) V_{REFN} internally connected to V_{SSA}.

Equation 1:

R_{AIN} max formula $R_{AIN} < \frac{T_s}{f_{ADC} * C_{ADC} * \ln(2^{N+2})} - R_{ADC}$

The formula above (Equation 1) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 4-36. ADC R_{AIN} max for f_{ADC} = 80 MHz (12-bit ADC) (1)

Reslolution	T_s (cycles)	t_s (μs)(2)	$R_{AIN\ max}$ (kΩ)(3)
12 bits	2.5	0.03125	-
	6.5	0.08125	0.26
	12.5	0.15625	1.24
	24.5	0.30625	3.21
	47.5	0.59375	6.97
	92.5	1.15625	14.33
	247.5	3.09375	39.70
	640.5	8.00625	-
10 bits	2.5	0.03125	-
	6.5	0.08125	0.44
	12.5	0.15625	1.58
	24.5	0.30625	3.87
	47.5	0.59375	8.27
	92.5	1.15625	16.86
	247.5	3.09375	46.46
	640.5	8.00625	-
8 bits	2.5	0.03125	-
	6.5	0.08125	0.68
	12.5	0.15625	2.06
	24.5	0.30625	4.81
	47.5	0.59375	10.08
	92.5	1.15625	20.39
	247.5	3.09375	55.91
	640.5	8.00625	-
6 bits	2.5	0.03125	-
	6.5	0.08125	1.06
	12.5	0.15625	2.78
	24.5	0.30625	6.21
	47.5	0.59375	12.80

Reslolution	T_s (cycles)	t_s (μs)(2)	$R_{AIN\ max}$ (kΩ)(3)
	92.5	1.15625	25.69
	247.5	3.09375	70.09
	640.5	8.00625	-

(1) Value guaranteed by design, not 100% tested in production.

(2) For channels of internal temperature sensor (V_{SENSE}) and internal reference voltage (V_{REFINT}), sampling time not less than 17.1us will be recommended.

(3) Extra internal capacitors (such as pin capacitors, etc.) need to be considered when calculating the actual R_{AIN}. Here we take 5 pF for the extra internal capacitance, C_{ADC} = 2.87pF + 5pF = 7.87pF.

Table 4-37. Internal reference voltage calibration values

Symbol	Test conditions	Memory address
V_{REFINT}(1)	V_{DD} = V_{DDA} = V_{REFP} = 3.3 V, Temperature = 25 °C	0x1FFFB3FC-0x1FFFB3FD

(1) V_{REFINT} is internally connected to the ADC_IN19 input channel.

Table 4-38. 12-bit ADC accuracy(1)

Symbol	Parameter	Test conditions	Typ	Max	Unit
EO(2)	Offset error	Single ended	±2	±3.5	LSB
		Differential	±1	±2	
DNL(2)	Differential linearity error	Single ended	±1	1.4/-1	
		Differential	±1	1.2/-1	
INL(2)	Integral linearity error	Single ended	1.2/-1	2/-1	
		Differential	±1	1.6/-1	
ENOB(2)	Effective number of bits	Single ended	10.8	—	Bits
		Differential	11.0	—	
SNDR(2)	Signal-to-noise and distortion ratio	Single ended	67.1	—	dB
		Differential	68.3	—	
SNR(2)	Signal-to-noise ratio	Single ended	68.5	—	
		Differential	70.2	—	
THD	Total harmonic distortion	Single ended	-72.6	—	
		Differential	-73.4	—	

(1) Value guaranteed by characterization, not 100% tested in production.

(2) V_{DDA} = V_{REFP} = 3.3 V, fADC = 50 MHz, the calibration time for the ADC is 16 times.

Figure 4-8. Differential linearity error

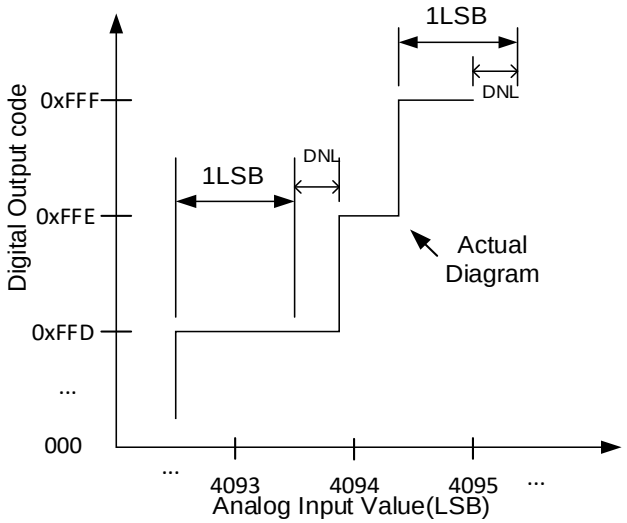
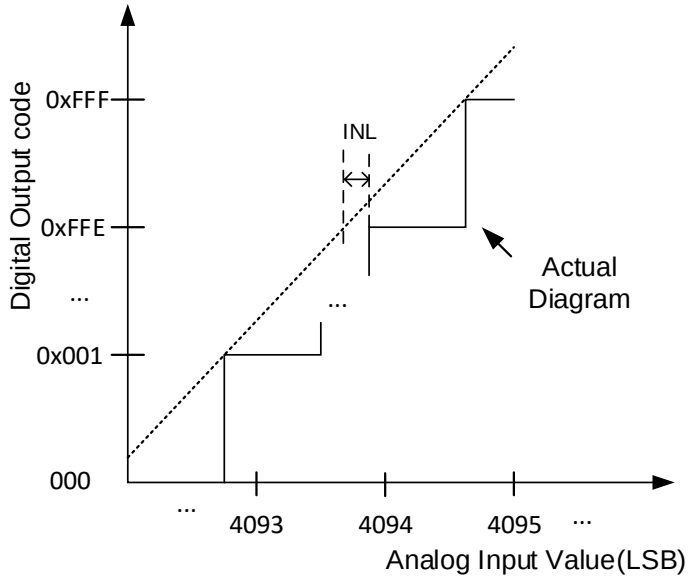


Figure 4-9. Integral linearity error



4.19. Temperature and V_{BAT} monitoring

Table 4-39. VBAT monitoring characteristics(1)

Symbol	Description	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	—	50	—	kΩ
Q	Ratio on V_{BAT} measurement	—	1/3	—	—
Er	Error on Q	-5	—	5	%
$t_{SAMPLE(VBAT)}$	ADC sampling time when reading V_{BAT} input	17.1	—	—	μs
$V_{BAT(high)}$	High supply monitoring	—	3.56	—	V
$V_{BAT(low)}$	Low supply monitoring	—	1.36	—	

(1) Value guaranteed by design, not 100% tested in production.

Table 4-40. V_{BAT} charging characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VCRSEL = 0	—	5	—	kΩ
		VCRSEL = 1	—	1.5	—	

(1) Value guaranteed by design, not 100% tested in production.

Table 4-41. Temperature monitoring characteristics(1)

Symbol	Description	Min	Typ	Max	Unit
$TEMP_{high}$	High temperature monitoring	—	120	—	°C
$TEMP_{low}$	Low temperature monitoring	—	-28	—	

(1) Value guaranteed by design, not 100% tested in production.

4.20. DAC characteristics

Table 4-42. 1MSPS DAC characteristics(1)(2)

Symbol	Description	Conditions		Min	Typ	Max	Unit
V_{DDA}	Operating voltage	DAC output buffer OFF, DAC_OUT Pin not connected (internal connection only)		1.71	3.3	3.6	V
		Other modes		1.80			
V_{REFP}	Positive Reference Voltage	DAC output buffer OFF, DAC_OUT Pin not connected (internal connection only)		1.71	—	V_{DDA}	V
		Other modes		1.80			
R_{LOAD}	Load resistance	Resistive load with buffer ON	Connected to VSSA	5	—	—	kΩ
			Connected to VDDA	5	—	—	kΩ
Ro	Impedance output	Impedance output with buffer OFF		—	—	15	kΩ
R_{BON}	Output impedance sample and hold mode, output buffer ON	DAC output buffer ON		—	—	3.5	kΩ
R_{BOFF}	Output impedance sample and hold mode, output buffer OFF	DAC output buffer OFF		—	—	18	
C_{LOAD}	Load capacitance	DAC output buffer ON		—	—	50	pF
C_{SH}		Sample and Hold mode		—	0.1	1	μF
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON		0.2	—	V_{DDA}-0.2	V
		DAC output buffer OFF		0	—	V_{REFP}-LSB	
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest	Normal mode, DAC output buffer ON, CL ≤ 50 pF,	±1 LSB	—	1.6	2.9	μs
			±2 LSB	—	1.55	2.85	
			±4 LSB	—	1.48	2.8	

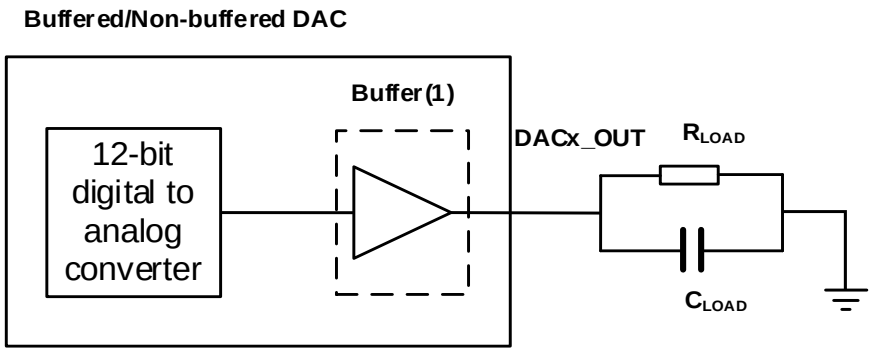
Symbol	Description	Conditions		Min	Typ	Max	Unit
	input codes when DAC_OUT reaches the final value of ±0.5LSB, ±1LSB, ±2LSB,	RL ≥ 5 kΩ	±8 LSB	—	1.4	2.75	
		Normal mode, DAC output buffer OFF, ±1LSB CL=10 pF		—	2	3.5	
t_{WAKEUP}	Wakeup time from off state until the final value of ±1LSB is reached	Normal mode, DAC output buffer ON, CL ≤ 50 pF, RL = 5 kΩ		—	5	10	µs
		Normal mode, DAC output buffer OFF, CL ≤ 10 pF		—	2	5	
PSRR	Power supply rejection ratio (to V_{DDA})	No R_{Load}, C_{LOAD} = 50 pF		-55	-80	—	dB
Update rate	Max frequency for a correct DAC_OUT change from code i to i±1LSBs	C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 5 kΩ		—	—	4	MS/s
t_{SAMP}	Sampling time in Sample and Hold mode, C_L=100 nF (code transition between the lowest input code and the highest input code when DAC_OUT reaches the ±1LSB final value)	MODE0[2:0] = 100 / 101 or MODE1[2:0] = 100 / 101 (BUFFER ON)		—	1.1	1.4	ms
		MODE0[2:0] = 110 or MODE1[2:0] = 110 (BUFFER OFF)		—	9.5	11.1	
		MODE0[2:0] = 111 or MODE1[2:0] = 111 (INTERNAL BUFFER OFF)		—	2.2	3.9	µs
C_{lint}	Internal sample and hold capacitor	—		5.2	7	8.8	pF
t_{TRIM}	Middle code offset trim time	Minimum time to verify the each code		50	—	—	µs
V_{offset}	Middle code offset for 1 trim code step	V_{REFP} = 3.6 V		—	1500	—	µV
		V_{REFP} = 1.8 V		—	750	—	
I_{DDA}	DAC current consumption in quiescent mode	DAC output buffer ON	No load, middle code (0x800)	—	340	—	uA
			No load, worst code (0xF1C)	—	360	—	
		DAC output buffer OFF	No load, middle/ worst code (0x800)	—	—	0.1	
		Sample and Hold mode, C_{SH}=100 nF		—	340*ducy	—	
$I_{DDVREFP}$	DAC current consumption in quiescent mode	DAC output buffer ON	No load, middle code (0x800)	—	95	—	uA
			No load, worst code (0xF1C)	—	130	—	
		DAC output	No load, middle	—	85	—	

Symbol	Description	Conditions		Min	Typ	Max	Unit
		buffer OFF	code (0x800)				
		Sample and Hold mode, Buffer ON, C_{SH}=100 nF (middle code)		—	95*du cy	—	
		Sample and Hold mode, Buffer OFF, C_{SH}=100 nF (middle code)		—	85*du cy	—	

(1) Value guaranteed by design, not 100% tested in production.

(2) V_{REFN} internally connected to V_{SSA}.

Figure 4-10. 12-bit buffered /non-buffered DAC



(1) The DAC integrates an output buffer to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the MODEx bit in the MDCR register.

Table 4-43. 1MSPS DAC accuracy(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
DNL	Differential non linearity	DAC output buffer ON	-2	—	2	LSB
		DAC output buffer OFF	-2	—	2	
INL	Integral non linearity	DAC output buffer ON	-6	—	6	LSB
		DAC output buffer OFF	-6	—	6	
Offset	Offset error at code 0x800	DAC output buffer ON	-7	—	7	LSB
		DAC output buffer OFF	-7	—	7	
Gain	Gain error	DAC output buffer ON	-0.5	—	0.5	%
		DAC output buffer OFF	-0.5	—	0.5	

(1) Value guaranteed by characterization, not 100% tested in production.

Table 4-44. 15MSPS DAC characteristics(1)(3)

Symbol	Description	Conditions		Min	Typ	Max	Unit
V_{DDA}	Operating voltage	—		1.71	3.3	3.6	V
V_{REFP}	Positive Reference Voltage	—		1.71	—	V_{DDA}	V
V_{DAC_OUT}	Voltage on DAC_OUT output	—		0	—	V_{REFP}-LSB	V
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest	with one comparator on DAC output	10% - 90%	—	16	18	ns
			5% - 95%	—	21	24	
			1% - 99%	—	33	43	

Symbol	Description	Conditions		Min	Typ	Max	Unit
	input codes when DAC_OUT reaches final value)		32 LSB	—	38	59	
			1 LSB	—	62	88	
t_{WAKEUP}(2)	Wakeup time from off state until the final value of ±1LSB is reached	Normal mode, CL ≤ 10 pF		—	1	2	µs
PSRR	Power supply rejection ratio (to V_{DDA})	—		-95	-140	—	dB
t_{SAMP}	Sampling time in Sample and Hold mode, (code transition between the lowest input code and the highest input code when DAC_OUT reaches the ±1LSB final value)	—		—	0.5	1	µs
C_{lint}	Internal sample and hold capacitor	—		—	5	6.25	pF
dV/dt (hold phase)	Voltage decay rate in Sample and hold mode, during hold phase	C_{SH} = 5 pF, T_A = 55°C		—	250000	—	µV/ ms
I_{DDA}	DAC current consumption in quiescent mode	No load, middle code (0x800)		—	—	0.1	uA
$I_{DDVREFP}$	DAC current consumption in quiescent mode	No load, middle code (0x800)		—	660	—	uA

(1) Value guaranteed by design, not 100% tested in production.
(2) In buffered mode, the output can overshoot above the final value for low input code (starting from min value).
(3) V_{REFN} internally connected to V_{SSA}.

Table 4-45. 15MSPS DAC accuracy(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
DNL	Differential non linearity(2)	—	-3	—	3	LSB
INL	Integral non linearity(3)	C_{LOAD} ≤ 50 pF, No R_{LOAD}	-6	—	6	

(1) Value guaranteed by characterization, not 100% tested in production.
(2) Difference between two consecutive codes -1 LSB.
(3) Difference between measured value at code i and the value at code i on a line drawn between code 0 and last code 4095. Offset error is included.

4.21. CAN characteristics

Refer to ***Table 4-28. I/O static characteristics*** for more details on the input/output alternate function characteristics (CANTX and CANRX).

4.22. Comparators characteristics

Table 4-46. CMP characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage	—	1.62	3.3	3.6	V
V_{IN}	Input voltage range	—	0	—	V_{DDA}	V
V_{SC}	Scaler offset voltage	—	—	3.3	10	mV
$I_{DDA(SCALER)}$	Scaler static consumption from V_{DDA}	CMPxBEN=0 (bridge disable)	—	200	226	nA
		CMPxBEN=1 (bridge enable)	—	800	930	
t_{START_SCALER}	Scaler startup time	—	—	—	60	μs
t_D	Propagation delay for 200mV step with 100 mV overdrive	50pF load on output	—	35(2)	—	ns
t_{START}	Comparator startup time to reach propagation delay specification	—	—	—	2	μs
$I_{DDA(CMP)}$	Current consumption from V_{DDA}	Static	—	433	436	uA
		With 50 kHz ±100 mV overdrive square signal	—	392	—	
V_{offset}	Offset error	Full VDDA voltage range, full temperature range	—	-3 ~ 4	—	mV
V_{hyst}	Hysteresis Voltage	CMPxHST[2:0] = 000	—	0	—	mV
		CMPxHST[2:0] = 001	6.8	8.8	15.1	
		CMPxHST[2:0] = 010	13.6	17.6	30.4	
		CMPxHST[2:0] = 011	20.4	26.5	46.0	
		CMPxHST[2:0] = 100	25.7	35.5	62.1	
		CMPxHST[2:0] = 101	28.8	44.6	78.9	
		CMPxHST[2:0] = 110	30.9	53.9	96.6	
		CMPxHST[2:0] = 111	32.5	63.3	116.3	

(1) Value guaranteed by design, not 100% tested in production.
(2) Value guaranteed by sample, not 100% tested in production.

4.23. Trigonometric Math Unit (TMU) characteristics

The TMU unit has 10 different operation modes.

Table 4-47. TMU supported instructions characteristics(1)

Mode	The first input data	The second input data	The first output data	The second output data	Cycles
Mode 0	θ	m	m*cos(θ)	m*sin(θ)	2+iteration steps/4(2)
Mode 1	θ	m	m*sin(θ)	m*cos(θ)	
Mode 2	x	y	atan2 (y,x)	$\sqrt{x^2+y^2}$	

Mode	The first input data	The second input data	The first output data	The second output data	Cycles
Mode 3	x	y	$\sqrt{x^2+y^2}$	atan2 (y,x)	
Mode 4	x	None	$\tan^{-1}$ (x)	None	
Mode 5	x	None	cosh (x)	sinh (x)	
Mode 6	x	None	sinh (x)	cosh (x)	
Mode 7	x	None	$\tanh^{-1}$ (x)	None	
Mode 8	x	None	ln (x)	None	
Mode 9	x	None	$\sqrt{x}$	None	

(1) Value guaranteed by design, not 100% tested in production.

(2) The number of iterations is configured using the TMU_CS -> ITRTNUM[3:0] bits. Refer to the ***GD32G5x3 User Manual*** which is selected to set the number of iterations.

4.24. I2C characteristics

Table 4-48. I2C characteristics(1)(2)(3)

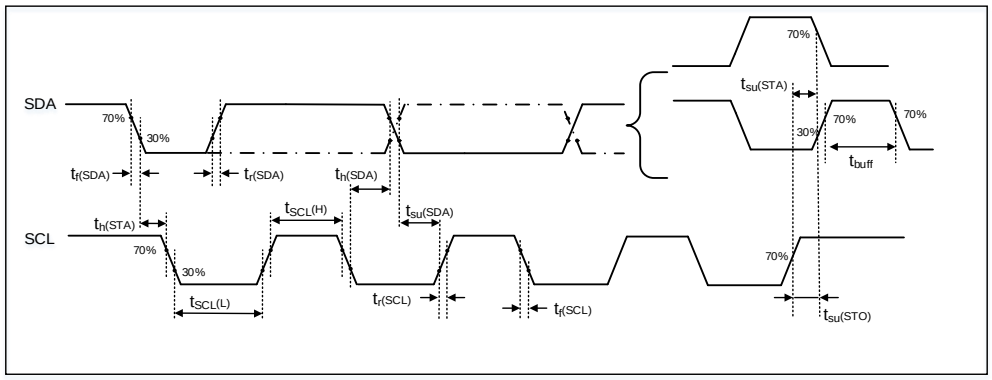
Symbol	Description	Conditions	Standard mode		Fast mode		Fast mode plus		Unit
			Min	Max	Min	Max	Min	Max	
$t_{SCL(H)}$	SCL clock high time	—	4.0	—	0.6	—	0.2	—	μs
$t_{SCL(L)}$	SCL clock low time	—	4.7	—	1.3	—	0.5	—	μs
$t_{su(SDA)}$	SDA setup time	—	250	—	100	—	50	—	ns
$t_{h(SDA)}$	SDA data hold time	—	0	—	0	—	0	—	ns
$t_{r(SDA/SCL)}$	SDA and SCL rise time	—	—	1000	20	300	—	120	ns
$t_{f(SDA/SCL)}$	SDA and SCL fall time	—	—	300	—	300	—	120	ns
$t_{h(STA)}$	Start condition hold time	—	4.0	—	0.6	—	0.26	—	μs

(1) Value guaranteed by design, not 100% tested in production.

(2) To ensure the standard mode I2C frequency, f_{PCLK1} must be at least 2 MHz, To ensure the fast mode I2C frequency, f_{PCLK1} must be at least 4 MHz. To ensure the fast mode plus I2C frequency, f_{PCLK1} must be at least a multiple of 10 MHz.

(3) The device should provide a data hold time of 300 ns at least in order to bridge the undefined region of the falling edge of SCL.

Figure 4-11. I2C bus timing diagram



4.25. SPI characteristics

Table 4-49. Standard SPI characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency for grade 7 devices	—	—	—	27	MHz
	SCK clock frequency for grade 3 devices	—	—	—	21.25	
$t_{SCK(H)}$	SCK clock high time for grade 7 devices	Master mode, f_{PCLKx} =216 MHz, presc = 8	—	18.5	—	ns
	SCK clock high time for grade 3 devices	Master mode, f_{PCLKx} =170 MHz, presc = 8	—	23.5	—	
$t_{SCK(L)}$	SCK clock low time for grade 7 devices	Master mode, f_{PCLKx} = 216 MHz, presc = 8	—	18.5	—	ns
	SCK clock low time for grade 3 devices	Master mode, f_{PCLKx} = 170 MHz, presc = 8	—	23.5	—	
SPI master mode						
$t_{V(MO)}$	Data output valid time	—	—	—	10	ns
$t_{SU(MI)}$	Data input setup time	—	1	—	—	ns
$t_{H(MI)}$	Data input hold time	—	0	—	—	ns
SPI slave mode						
$t_{SU(NSS)}$	NSS enable setup time	—	0	—	—	ns
$t_{H(NSS)}$	NSS enable hold time	—	1	—	—	ns
$t_{A(SO)}$	Data output access time	—	—	8	—	ns
$t_{DIS(SO)}$	Data output disable time	—	—	9	—	ns
$t_{V(SO)}$	Data output valid time	—	—	9	—	ns
$t_{SU(SI)}$	Data input setup time	—	0	—	—	ns
$t_{H(SI)}$	Data input hold time	—	1	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-12. SPI timing diagram - master mode

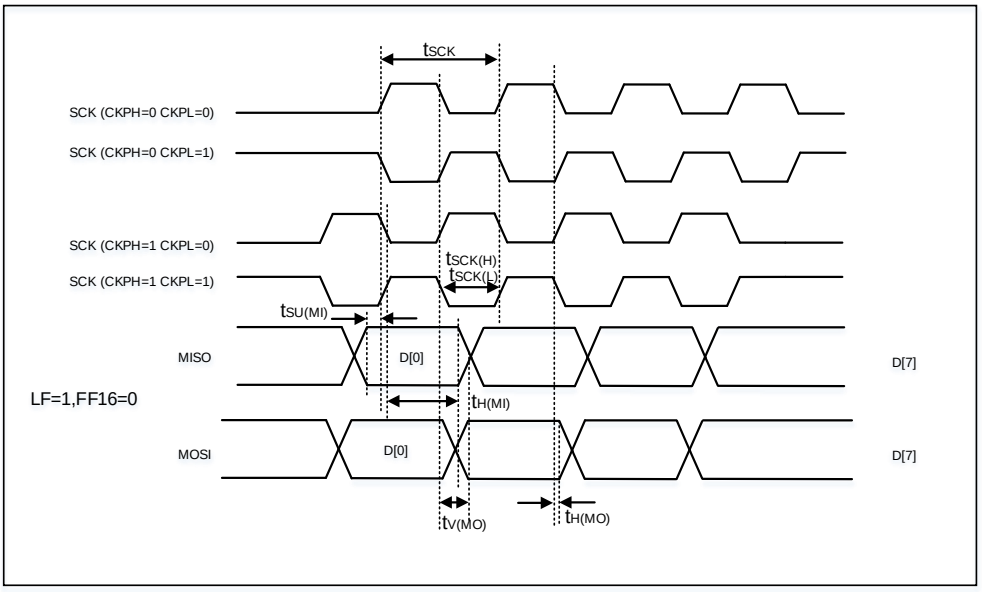


Figure 4-13. SPI timing diagram - slave mode(CKPH=0)

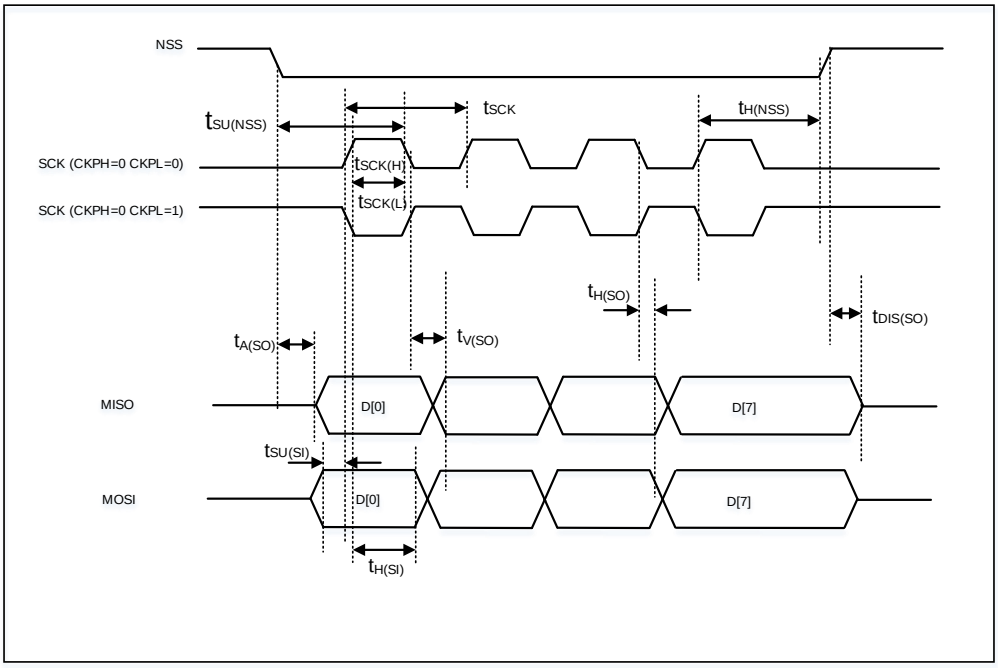
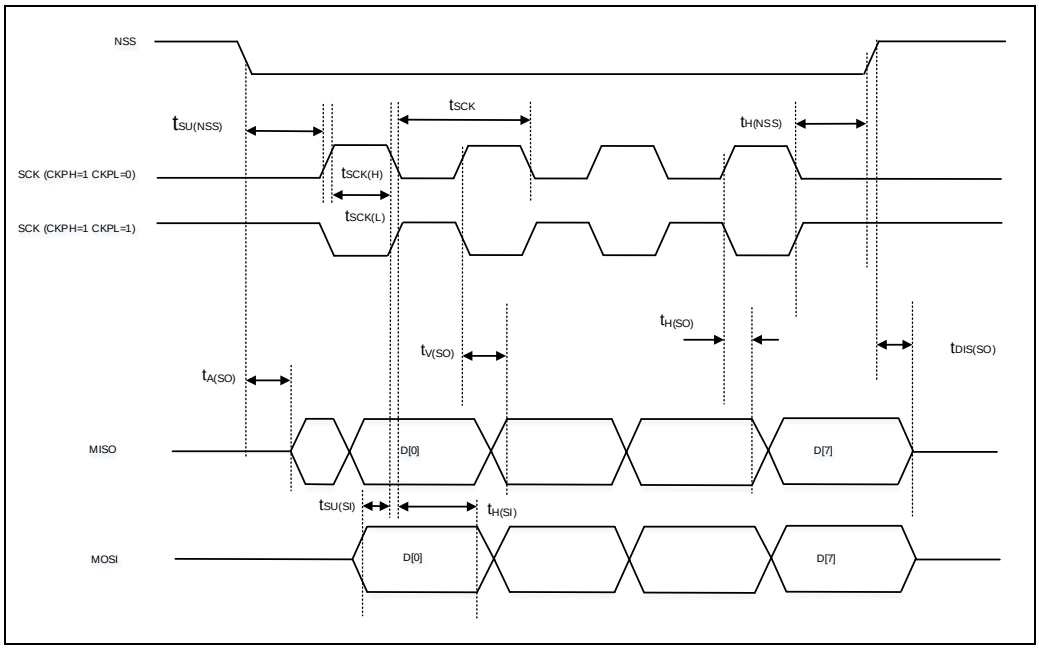


Figure 4-14. SPI timing diagram - slave mode(CKPH=1)



4.26. USART characteristics

Table 4-50. USART characteristics in Synchronous mode (For GD32G553xxx7) (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	f_{PCLKx} = 216 MHz	—	—	27	MHz
$t_{SCK(H)}$	SCK clock high time		18.5	—	—	ns
$t_{SCK(L)}$	SCK clock low time		18.5	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

Table 4-51. USART characteristics in Synchronous mode(For GD32G553xxx3) (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	f_{PCLKx} = 170 MHz	—	—	21.25	MHz
$t_{SCK(H)}$	SCK clock high time		23.5	—	—	ns
$t_{SCK(L)}$	SCK clock low time		23.5	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

Table 4-52. USART characteristics in Smartcard mode (For GD32G553xxx7) (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	f_{PCLKx} = 216 MHz	—	—	108	MHz
$t_{SCK(H)}$	SCK clock high time		4.6	—	—	ns
$t_{SCK(L)}$	SCK clock low time		4.6	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

Table 4-53. USART characteristics in Smartcard mode(For GD32G553xxx3) (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	f_{PCLKx} = 170 MHz	—	—	85	MHz
$t_{SCK(H)}$	SCK clock high time		5.8	—	—	ns

Symbol	Description	Conditions	Min	Typ	Max	Unit
$t_{SCK(L)}$	SCK clock low time		5.8	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

4.27. EXMC characteristics

Table 4-54. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)(2)(3)

Symbol	Description	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	6*Tfclk-1	6*Tfclk+1	ns
$t_{V(NOE\_NE)}$	EXMC_NEx low to EXMC_NOE low	0	—	ns
$t_{w(NOE)}$	EXMC_NOE low time	6*Tfclk-1	6*Tfclk+1	ns
$t_{h(NE\_NOE)}$	EXMC_NOE high to EXMC_NE high hold time	0	—	ns
$t_{v(A\_NE)}$	EXMC_NEx low to EXMC_A valid	0	—	ns
$t_{v(BL\_NE)}$	EXMC_NEx low to EXMC_BL valid	0	—	ns
$t_{su(DATA\_NE)}$	Data to EXMC_NEx high setup time	4*Tfclk-1	—	ns
$t_{su(DATA\_NOE)}$	Data to EXMC_NOEx high setup time	4*Tfclk-1	—	ns
$t_{h(DATA\_NOE)}$	Data hold time after EXMC_NOE high	0	—	ns
$t_{h(DATA\_NE)}$	Data hold time after EXMC_NEx high	0	—	ns
$t_{v(NADV\_NE)}$	EXMC_NEx low to EXMC_NADV low	0	—	ns
$t_{w(NADV)}$	EXMC_NADV low time	2*Tfclk-1	2*Tfclk+1	ns

(1) C_L = 30 pF.

(2) Value guaranteed by design, not 100% tested in production.

(3) Based on configure: AddressSetupTime = 2, AddressHoldTime = 3, DataSetupTime = 4.

Table 4-55. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)(2)(3)

Symbol	Description	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	7*Tfclk-1	7*Tfclk+1	ns
$t_{V(NWE\_NE)}$	EXMC_NEx low to EXMC_NWE low	0	—	ns
$t_{w(NWE)}$	EXMC_NWE low time	4*Tfclk-1	4*Tfclk+1	ns
$t_{h(NE\_NWE)}$	EXMC_NWE high to EXMC_NE high hold time	1*Tfclk-1	1*Tfclk+1	ns
$t_{v(A\_NE)}$	EXMC_NEx low to EXMC_A valid	0	—	ns
$t_{V(NADV\_NE)}$	EXMC_NEx low to EXMC_NADV low	0	—	ns
$t_{w(NADV)}$	EXMC_NADV low time	2*Tfclk-1	2*Tfclk+1	ns
$t_{h(AD\_NADV)}$	EXMC_AD(address) valid hold time after EXMC_NADV high	3*Tfclk-1	—	ns
$t_{h(A\_NWE)}$	Address hold time after EXMC_NWE high	1*Tfclk-1	—	ns
$t_{h(BL\_NWE)}$	EXMC_BL hold time after EXMC_NWE high	1*Tfclk-1	—	ns
$t_{v(BL\_NE)}$	EXMC_NEx low to EXMC_BL valid	0	—	ns
$t_{v(DATA\_NADV)}$	EXMC_NADV high to DATA valid	0	—	ns
$t_{h(DATA\_NWE)}$	Data hold time after EXMC_NWE high	1*Tfclk-1	1*Tfclk+1	ns

(1) C_L = 30 pF.

(2) Value guaranteed by design, not 100% tested in production.

(3) Based on configure: AddressSetupTime = 2, AddressHoldTime = 3, DataSetupTime = 4.

Table 4-56. Asynchronous multiplexed PSRAM/NOR read timings(1)(2)(3)

Symbol	Description	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	9*Tfclk-1	9*Tfclk+1	ns
$t_{V(NOE\_NE)}$	EXMC_NEx low to EXMC_NOE low	5*Tfclk-1	5*Tfclk+1	ns
$t_{w(NOE)}$	EXMC_NOE low time	4*Tfclk-1	4*Tfclk+1	ns
$t_{h(NE\_NOE)}$	EXMC_NOE high to EXMC_NE high hold time	0	—	ns
$t_{v(A\_NE)}$	EXMC_NEx low to EXMC_A valid	0	—	ns
$t_{v(A\_NOE)}$	Address hold time after EXMC_NOE high	0	—	ns
$t_{v(BL\_NE)}$	EXMC_NEx low to EXMC_BL valid	0	—	ns
$t_{h(BL\_NOE)}$	EXMC_BL hold time after EXMC_NOE high	0	—	ns
$t_{su(DATA\_NE)}$	Data to EXMC_NEx high setup time	4*Tfclk-1	—	ns
$t_{su(DATA\_NOE)}$	Data to EXMC_NOEx high setup time	4*Tfclk-1	—	ns
$t_{h(DATA\_NOE)}$	Data hold time after EXMC_NOE high	0	—	ns
$t_{h(DATA\_NE)}$	Data hold time after EXMC_NEx high	0	—	ns
$t_{v(NADV\_NE)}$	EXMC_NEx low to EXMC_NADV low	0	—	ns
$t_{w(NADV)}$	EXMC_NADV low time	2*Tfclk-1	2*Tfclk+1	ns
$T_{h(AD\_NADV)}$	EXMC_AD(adress) valid hold time after EXMC_NADV high	3*Tfclk-1	3*Tfclk+1	ns

(1) C_L = 30 pF.
(2) Value guaranteed by design, not 100% tested in production.
(3) Based on configure: AddressSetupTime = 2, AddressHoldTime = 3, DataSetupTime = 4.

Table 4-57. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)(3)

Symbol	Description	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	10*Tfclk-1	10*Tfclk+1	ns
$t_{V(NWE\_NE)}$	EXMC_NEx low to EXMC_NWE low	2*Tfclk-1	2*Tfclk+1	ns
$t_{w(NWE)}$	EXMC_NWE low time	7*Tfclk-1	7*Tfclk+1	ns
$t_{h(NE\_NWE)}$	EXMC_NWE high to EXMC_NE high hold time	1*Tfclk-1	—	ns
$t_{v(A\_NE)}$	EXMC_NEx low to EXMC_A valid	0	—	ns
$t_{V(NADV\_NE)}$	EXMC_NEx low to EXMC_NADV low	0	—	ns
$t_{w(NADV)}$	EXMC_NADV low time	2*Tfclk-1	2*Tfclk+1	ns
$t_{h(AD\_NADV)}$	EXMC_AD(address) valid hold time after EXMC_NADV high	3*Tfclk-1	—	ns
$t_{h(A\_NWE)}$	Address hold time after EXMC_NWE high	1*Tfclk-1	—	ns
$t_{h(BL\_NWE)}$	EXMC_BL hold time after EXMC_NWE high	0	—	ns
$t_{v(BL\_NE)}$	EXMC_NEx low to EXMC_BL valid	0	—	ns
$t_{v(DATA\_NADV)}$	EXMC_NADV high to DATA valid	3*Tfclk-1	—	ns
$t_{h(DATA\_NWE)}$	Data hold time after EXMC_NWE high	1*Tfclk-1	—	ns

(1) C_L = 30 pF.
(2) Value guaranteed by design, not 100% tested in production.
(3) Based on configure: AddressSetupTime = 2, AddressHoldTime = 3, DataSetupTime = 4.

Table 4-58. Synchronous multiplexed PSRAM/NOR read timings(1)(2)(3)

Symbol	Description	Min	Max	Unit
$t_{w(CLK)}$	EXMC_CLK period	4*Tfclk	—	ns

Symbol	Description	Min	Max	Unit
$t_{d(CLKL-NExL)}$	EXMC_CLK low to EXMC_NEx low	0	—	ns
$t_{d(CLKH-NExH)}$	EXMC_CLK high to EXMC_NEx high	2*Tfclk-1	—	ns
$t_{d(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	—	ns
$t_{d(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	—	ns
$t_{d(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	0	—	ns
$t_{d(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	2*Tfclk-1	—	ns
$t_{d(CLKL-NOEL)}$	EXMC_CLK low to EXMC_NOE low	0	—	ns
$t_{d(CLKH-NOEH)}$	EXMC_CLK high to EXMC_NOE high	2*Tfclk-1	—	ns
$t_{d(CLKL-ADV)}$	EXMC_CLK low to EXMC_AD valid	0	—	ns
$t_{d(CLKL-ADIV)}$	EXMC_CLK low to EXMC_AD invalid	0	—	ns

(1) C_L = 30 pF.
(2) Value guaranteed by design, not 100% tested in production.
(3) Based on configure: BurstAccessMode = Enable; Memory Type = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); Data Latency = 1.

Table 4-59. Synchronous multiplexed PSRAM write timings(1)(2)(3)

Symbol	Description	Min	Max	Unit
$t_{w(CLK)}$	EXMC_CLK period	4*Tfclk	—	ns
$t_{d(CLKL-NExL)}$	EXMC_CLK low to EXMC_NEx low	0	—	ns
$t_{d(CLKH-NExH)}$	EXMC_CLK high to EXMC_NEx high	2*Tfclk-1	—	ns
$t_{d(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	—	ns
$t_{d(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	—	ns
$t_{d(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	0	—	ns
$t_{d(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	2*Tfclk-1	—	ns
$t_{d(CLKL-NWEL)}$	EXMC_CLK low to EXMC_NWE low	0	—	ns
$t_{d(CLKH-NWEH)}$	EXMC_CLK high to EXMC_NWE high	2*Tfclk-1	—	ns
$t_{d(CLKL-ADIV)}$	EXMC_CLK low to EXMC_AD invalid	0	—	ns
$t_{d(CLKL-DATA)}$	EXMC_A/D valid data after EXMC_CLK low	0	—	ns
$t_{h(CLKL-NBLH)}$	EXMC_CLK low to EXMC_NBL high	0	—	ns

(1) C_L = 30 pF.
(2) Value guaranteed by design, not 100% tested in production.
(3) Based on configure: BurstAccessMode = Enable; MemoryType = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); DataLatency = 1.

Table 4-60. Synchronous non-multiplexed PSRAM/NOR read timings(1)(2)(3)

Symbol	Description	Min	Max	Unit
$t_{w(CLK)}$	EXMC_CLK period	4*Tfclk	—	ns
$t_{d(CLKL-NExL)}$	EXMC_CLK low to EXMC_NEx low	0	—	ns
$t_{d(CLKH-NExH)}$	EXMC_CLK high to EXMC_NEx high	2*Tfclk-1	—	ns
$t_{d(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	—	ns
$t_{d(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	—	ns
$t_{d(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	0	—	ns
$t_{d(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	2*Tfclk-1	—	ns
$t_{d(CLKL-NOEL)}$	EXMC_CLK low to EXMC_NOE low	0	—	ns
$t_{d(CLKH-NOEH)}$	EXMC_CLK high to EXMC_NOE high	2*Tfclk-1	—	ns

(1) C_L = 30 pF.
(2) Value guaranteed by design, not 100% tested in production.
(3) Based on configure: BurstAccessMode = Enable; MemoryType = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); DataLatency = 1.

Table 4-61. Synchronous non-multiplexed PSRAM write timings(1)(2)(3)

Symbol	Description	Min	Max	Unit
$t_{w(CLK)}$	EXMC_CLK period	4*Tfclk	—	ns
$t_{d(CLKL-NExL)}$	EXMC_CLK low to EXMC_NEx low	0	—	ns
$t_{d(CLKH-NExH)}$	EXMC_CLK high to EXMC_NEx high	2*Tfclk-1	—	ns
$t_{d(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	—	ns
$t_{d(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	—	ns
$t_{d(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	2*Tfclk-1	—	ns
$t_{d(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	0	—	ns
$t_{d(CLKL-NWEL)}$	EXMC_CLK low to EXMC_NWE low	0	—	ns
$t_{d(CLKH-NWEH)}$	EXMC_CLK high to EXMC_NWE high	2*Tfclk-1	—	ns
$t_{d(CLKL-DATA)}$	EXMC_A/D valid data after EXMC_CLK low	0	—	ns
$t_{h(CLKL-NBLH)}$	EXMC_CLK low to EXMC_NBL high	0	—	ns

(1) C_L = 30 pF.
(2) Value guaranteed by design, not 100% tested in production.
(3) Based on configure: BurstAccessMode = Enable; MemoryType = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); DataLatency = 1.

4.28. QSPI characteristics

Table 4-62. Standard QSPI characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SDR mode						
f_{SCK}	SCK clock frequency for grade 7 devices	—	—	—	200	MHz
	SCK clock frequency for grade 3 devices	—	—	—	170	
$t_{SCK(H)}$	SCK clock high time, even division	—	t(CK)/2	—	t(CK)/2+1	ns
	SCK clock high time, odd division	—	(n/2)*t(CK)/(n+1)	—	(n/2)*t(CK)/(n+1)+1	ns
$t_{SCK(L)}$	SCK clock high time, even division	—	t(CK)/2–1	—	t(CK)/2	ns
	SCK clock high time, odd division	—	(n/2+1)*t(CK)/(n+1)–1	—	(n/2+1)*t(CK) /(n+1)	ns
$t_{V(MO)}$	Data output valid time	—	—	0.5	1	ns
$t_{H(MO)}$	Data output hold time	—	1	—	—	ns
$t_{SU(MI)}$	Data input setup time	—	1	—	—	ns
$t_{H(MI)}$	Data input hold time	—	2.5	—	—	ns
DDR mode						

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency for grade 7 devices	—	—	—	200	MHz
	SCK clock frequency for grade 3 devices	—	—	—	170	
$t_{SCK(H)}$	SCK clock high time, even division	—	t(CK)/2	—	t(CK)/2+1	ns
	SCK clock high time, odd division	—	(n/2)*t(CK)/(n+1)	—	(n/2)*t(CK)/(n+1)+1	ns
$t_{SCK(L)}$	SCK clock high time, even division	—	t(CK)/2–1	—	t(CK)/2	ns
	SCK clock high time, odd division	—	(n/2+1)*t(CK)/(n+1)–1	—	(n/2+1)*t(CK) /(n+1)	ns
$t_{V(SO)}$	Data output valid time	—	—	0.5	1	ns
$t_{H(SO)}$	Data output hold time	—	0.5	—	—	ns
$t_{SU(SI)}$	Data input setup time	—	1	—	—	ns
$t_{H(SI)}$	Data input hold time	—	1	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

Table 4-63. Standard QSPI (f_{SCKMAX}=120 MHz) characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SDR mode						
f_{SCK}	SCK clock frequency	—	—	—	120	MHz
$t_{SCK(H)}$	SCK clock high time, even division	—	t(CK)/2	—	(CK)/2+1	ns
	SCK clock high time, odd division	—	(n/2)*t(CK)/(n+1)	—	(n/2)*t(CK)/(n+1)+1	ns
$t_{SCK(L)}$	SCK clock high time, even division	—	t(CK)/2–1	—	t(CK)/2	ns
	SCK clock high time, odd division	—	(n/2+1)*t(CK)/(n+1)–1	—	(n/2+1)*t(CK) /(n+1)	ns
$t_{V(MO)}$	Data output valid time	—	—	0.5	1	ns
$t_{H(MO)}$	Data output hold time	—	1.5	—	—	ns
$t_{SU(MI)}$	Data input setup time	—	1.5	—	—	ns
$t_{H(MI)}$	Data input hold time	—	4	—	—	ns
DDR mode						
f_{SCK}	SCK clock frequency	—	—	—	120	MHz
$t_{SCK(H)}$	SCK clock high time, even division	—	t(CK)/2	—	(CK)/2+1	ns
	SCK clock high time, odd division	—	(n/2)*t(CK)/(n+1)	—	(n/2)*t(CK)/(n+1)+1	ns
$t_{SCK(L)}$	SCK clock high time, even division	—	t(CK)/2–1	—	t(CK)/2	ns
	SCK clock high time, odd division	—	(n/2+1)*t(CK)/(n+1)–1	—	(n/2+1)*t(CK) /(n+1)	ns
$t_{V(SO)}$	Data output valid time	—	—	1	2	ns
$t_{H(SO)}$	Data output hold time	—	1	—	—	ns
$t_{SU(SI)}$	Data input setup time	—	1	—	—	ns
$t_{H(SI)}$	Data input hold time	—	1	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-15. QSPI timing diagram - SDR mode

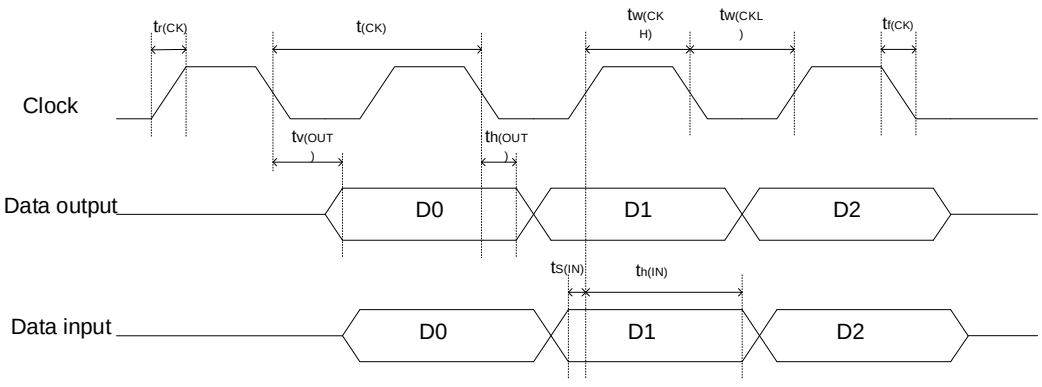
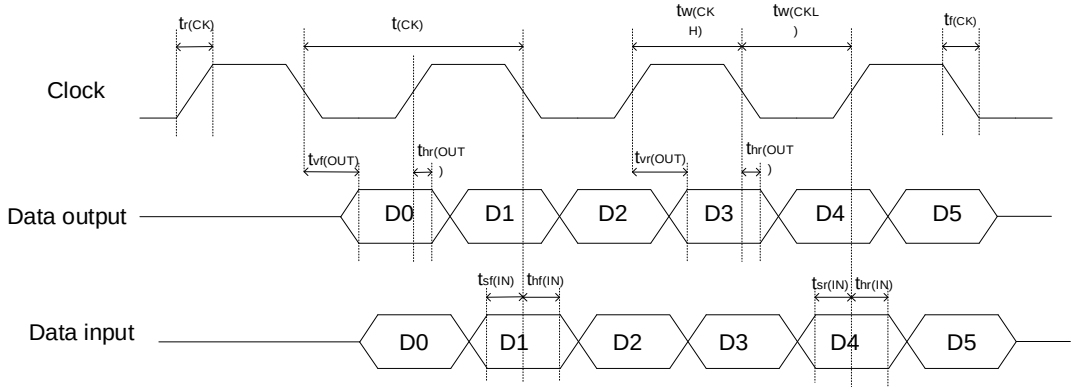


Figure 4-16. QSPI timing diagram - DDR mode



4.29. CPDM characteristics

Table 4-64. CPDM characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{init}	Initial delay	—	2	—	9	ps
t_{Δ}	Unit Delay	—	31	—	65	ps

(1) Value guaranteed by design, not 100% tested in production.

4.30. HPDF characteristics

Table 4-65. HPDF characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{HPDFCLK}$	HPDF clock	—	—	f_{APB2}	f_{SYSCLK}	MHz
f_{CKIN} ($1 / T_{CKIN}$)	Input clock frequency	SPI mode(SITYP[1:0]=01)	—	—	$20(f_{HPDFCLK}/4)$	
f_{CKOUT}	Output clock frequency	—	—	—	20	
$Duty_{CKOUT}$	Output clock frequency duty cycle	—	30	50	75	%
$t_{wh(CKIN)}$ $t_{wl(CKIN)}$	Input clock high and low time	SPI mode(SITYP[1:0]=01), External clock mode(SPICKSS[1:0]=0)	$T_{CKIN}/2-0.5$	$T_{CKIN}/2$	—	ns
t_{SU}	Data input setup time	SPI mode(SITYP[1:0]=01), External clock mode(SPICKSS[1:0]=0)	1	—	—	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_h	Data input hold time	SPI mode(SITYP[1:0]=01), External clock mode(SPICKSS[1:0]=0)	1	—	—	ns
$T_{Manchester}$	Manchester data period(recovered clock period)	Manchester mode(SITYP[1:0]=10 or 11), Internal clock mode(SPICKSS[1:0]≠0)	(CKOUTDIV +1)*$T_{HPDFCLK}$	—	(2*CKOUTDIV +1)*$T_{HPDFCLK}$	

(1) Value guaranteed by design, not 100% tested in production.

(2) Output speed is set to OSPDy[1:0]=10; Capacitive load C = 30 pF; Measurement points are done at COMS levels: 0.5*V_{DD}.

4.31. High-resolution Timer (HRTIMER) characteristics

Table 4-66. HRTIMER characteristics (For GD32G553xxx7) (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
$f_{HRTIMER}$	HRTIMER input clock for DLL	Under T_A conditions	130	—	216	MHz
$t_{HRTIMER}$			4.63	—	7.69	ns
$t_{res(HRTIMER)}$	Timer resolution time	f_{HPMER} = 216 MHz	—	145	—	ps
$RES_{HRTIMER}$	Timer resolution	—	—	—	16	bit
t_{DTG}	Dead time generator clock period	—	0.125	—	16	$t_{HRTIMER}$
		$f_{HRTIMER}$ = 216 MHz	0.578	—	74.1	ns
$\|t_{DTR}\|$ / $\|t_{DTF}\|$	Dead time range (absolute value)	—	—	—	511	t_{DTG}
		$f_{HRTIMER}$ = 216 MHz	—	—	37.85	µs
f_{CHPFRQ}	Chopper stage clock frequency	—	1/256	—	1/16	$f_{HRTIMER}$
		$f_{HRTIMER}$ = 216 MHz	0.844	—	13.5	MHz
t_{1STPW}	Chopper first pulse length	—	16	—	256	$t_{HRTIMER}$
		$f_{HRTIMER}$ = 216 MHz	0.074	—	1.185	µs

(1) Value guaranteed by design, not 100% tested in production.

Table 4-67. HRTIMER characteristics (For GD32G553xxx3) (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
$f_{HRTIMER}$	HRTIMER input clock for DLL	Under T_A conditions	130	—	170	MHz
$t_{HRTIMER}$			5.88	—	7.69	ns
$t_{res(HRTIMER)}$	Timer resolution time	f_{HPMER} = 170 MHz	—	184	—	ps
$RES_{HRTIMER}$	Timer resolution	—	—	—	16	bit
t_{DTG}	Dead time generator clock period	—	0.125	—	16	$t_{HRTIMER}$
		$f_{HRTIMER}$ = 170 MHz	0.734	—	94.1	ns
$\|t_{DTR}\|$ / $\|t_{DTF}\|$	Dead time range (absolute value)	—	—	—	511	t_{DTG}
		$f_{HRTIMER}$ = 170 MHz	—	—	48.07	µs
f_{CHPFRQ}	Chopper stage clock frequency	—	1/256	—	1/16	$f_{HRTIMER}$
		$f_{HRTIMER}$ = 170 MHz	0.66	—	10.63	MHz
t_{1STPW}	Chopper first pulse	—	16	—	256	$t_{HRTIMER}$

Symbol	Description	Conditions	Min	Typ	Max	Unit
	length	$f_{HRTIMER}$ = 170 MHz	0.094	—	1.505	μs

(1) Value guaranteed by design, not 100% tested in production.

Table 4-68. HRTIMER output response to fault protection(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
$t_{LAT(DF)}$	Digital fault response latency	Propagation delay from HRTIMER_FLTx digital input to HRTIMER_STxCHy output pin	—	—	24	ns
$t_{W(FLT)}$	Minimum fault pulse width for grade 7 devices	—	10	—	—	
	Minimum fault pulse width for grade 3 devices		15	—	—	
$t_{LAT(AF)}$	Analog fault response latency	Propagation delay from comparator CMPx_IPx input to HRTIMER_STxCHy output pin	—	—	35	

(1) Value guaranteed by design, not 100% tested in production.

Table 4-69. HRTIMER output response to external event 0 to 4 (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
$t_{LAT(DEEV)}$	Digital external event response latency	Propagation delay from HRTIMER_EXEVx digital input to HRTIMER_STxCHy output pin(30pF load)	—	—	24	ns
$t_{W(FLT)}$	Minimum external event pulse width for grade 7 devices	—	10	—	—	
	Minimum external event pulse width for grade 3 devices		15	—	—	
$t_{LAT(AEEV)}$	Analog external event response latency	Propagation delay from comparator CMPx_IPx input pin to HRTIMER_STxCHy output pin(30pF load)	—	—	35	

(1) Value guaranteed by design, not 100% tested in production.

Table 4-70. HRTIMER output response to external event 0 to 9(Synchronous mode(1))

Symbol	Description	Conditions	Min	Typ	Max	Unit
$T_{PROP(HRTIMER)}$	External event response latency in HRTIMER	HRTIMER internal propagation delay(3)	5	—	6	$t_{HRTIMER}$(2)
$t_{LAT(DEEV)}$	Digital external event response latency	Propagation delay from HRTIMER_EXEVx digital input to HRTIMER_STxCHy output pin(30pF load)	—	—	40	ns
$t_{W(FLT)}$	Minimum external event	—	10	—	—	

Symbol	Description	Conditions	Min	Typ	Max	Unit
	pulse width for grade 7 devices					
	Minimum external event pulse width for grade 3 devices		15	—	—	
$t_{LAT(AEEV)}$	Analog external event response latency	Propagation delay from comparator CMPx_IPx input pin to HRTIMER_STxCHy output pin(30pF load)	—	—	50	
$T_{JIT(EEV)}$	External event response jitter	Jitter of the delay from HRTIMER_EXEVx digital input or CMPx_IPx input pin to HRTIMER_STxCHy output pin(30pF load)	—	—	1	$t_{HRTIMER}$(2)
$T_{JIT(PW)}$	Jitter on output pulse width in response to an external event	—	—	—	0	$t_{HRTIMER}$(2)

(1) Value guaranteed by design, not 100% tested in production.

(2) $t_{HRTIMER}$ = 1 / $f_{HRTIMER}$ with $f_{HRTIMER}$ = 216 MHz depending on the clock controller configuration.

(3) This parameter does not take into account latency introduced by GPIO or comparator.

Table 4-71. HRTIMER synchronization input / output(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
$t_{W(SYNCIN)}$	Minimum pulse width on SYNCIN inputs, including HRTIMER_SCIN	—	2	—	—	$t_{HRTIMER}$(2)
$t_{LAT(DF)}$	Response time to external synchronization request	—	—	—	1	$t_{HRTIMER}$(2)
$t_{W(AF)}$	Pulse width on HRTIMER_SCOUT output	—	—	16	—	$t_{HRTIMER}$(2)
		$f_{HRTIMER}$ = 216 MHz	—	74	—	ns
		$f_{HRTIMER}$ = 170 MHz	—	94	—	

(1) Value guaranteed by design, not 100% tested in production.

(2) $t_{HRTIMER}$ = 1 / $f_{HRTIMER}$ with $f_{HRTIMER}$ = 216 MHz depending on the clock controller configuration.

4.32. TIMER characteristics

Table 4-72. TIMER characteristics (For GD32G553xxx7) (1)

Symbol	Description	Conditions	Min	Max	Unit
t_{res}	Timer resolution time	—	1	—	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 216 MHz	4.6	—	ns
f_{EXT}	Timer external clock frequency	—	0	$f_{TIMERxCLK}$/2	MHz
		$f_{TIMERxCLK}$ = 216 MHz	0	108	MHz
RES	Timer resolution	TIMERx (except TIMER1/4)	—	16	bit

Symbol	Description	Conditions	Min	Max	Unit
		TIMER1/4	—	32	
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	—	1	65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 216 MHz	0.0046	301.46	μs
	32-bit counter clock period when internal clock is selected (only TIMER1/4)	—	1	2^{32}	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 216 MHz	$4.6x10^{-9}$	19.7	s
t_{MAX_COUNT}	Maximum possible count (except TIMER1/4)	—	—	65536x65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 216 MHz	—	19.7	s
	Maximum possible count (only TIMER1/4)	—	—	$65536x2^{32}$	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 216 MHz	—	361.979	h

(1) Value guaranteed by design, not 100% tested in production.

Table 4-73. TIMER characteristics (For GD32G553xxx3) (1)

Symbol	Description	Conditions	Min	Max	Unit
t_{res}	Timer resolution time	—	1	—	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 170 MHz	5.88	—	ns
f_{EXT}	Timer external clock frequency	—	0	$f_{TIMERxCLK}/2$	MHz
		$f_{TIMERxCLK}$ = 170 MHz	0	85	MHz
RES	Timer resolution	TIMERx (except TIMER1/4)	—	16	bit
		TIMER1/4	—	32	
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	—	1	65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 170 MHz	0.00588	385.5	μs
	32-bit counter clock period when internal clock is selected (only TIMER1/4)	—	1	2^{32}	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 170 MHz	$5.88x10^{-9}$	25.26	s
t_{MAX_COUNT}	Maximum possible count (except TIMER1/4)	—	—	65536x65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 170 MHz	—	25.26	s
	Maximum possible count (only TIMER1/4)	—	—	$65536x2^{32}$	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 170 MHz	—	459.93	h

(1) Value guaranteed by design, not 100% tested in production.

4.33. WDGT characteristics

Table 4-74. FWDGT min/max timeout period at 32 kHz (IRC32K)(1)

Prescaler divider	PSC[2:0] bits	Min timeout RLD[11:0] = 0x000	Max timeout RLD[11:0] = 0xFFF	Unit
1/4	000	0.125	512	ms
1/8	001	0.25	1024	
1/16	010	0.5	2048	
1/32	011	1.0	4096	

Prescaler divider	PSC[2:0] bits	Min timeout RLD[11:0] = 0x000	Max timeout RLD[11:0] = 0xFFF	Unit
1/64	100	2.0	8192	
1/128	101	4.0	16384	
1/256	110 or 111	8.0	32768	

(1) Value guaranteed by design, not 100% tested in production.

Table 4-75. WWDGT min-max timeout value at 100 MHz (f_{PCLK1})(1)

Prescaler divider	PSC[1:0]	Min timeout value CNT[6:0] = 0x40	Unit	Max timeout value CNT[6:0] = 0x7F	Unit
1/1	00	40.96	µs	2.621	ms
1/2	01	81.92		5.242	
1/4	10	163.84		10.485	
1/8	11	327.68		20.971	

(1) Value guaranteed by design, not 100% tested in production.

4.34. JTAG Timing

Table 4-76. JTAG Scan Interface Timing (For GD32G553xxx7) (1)

Symbol	Description	Min	Max	Unit
$t_{C(JTAG)}$	Cycle time, JTAG low and high period	18.5	—	ns
$t_{SU(TDI/TMS - TCKr)}$	Setup time, TDI, TMS before TCK rise (TCKr)	7	—	ns
$t_{H(TCKr -TDI/TMS)}$	Hold time, TDI, TMS after TCKr	1	—	ns
$t_{H(TCKf -TDO)}$	Hold time, TDO after TCKf	6	—	ns
$t_{D(TCKf -TDO)}$	Delay time, TDO valid after TCK fall (TCKf)	—	6.5	ns

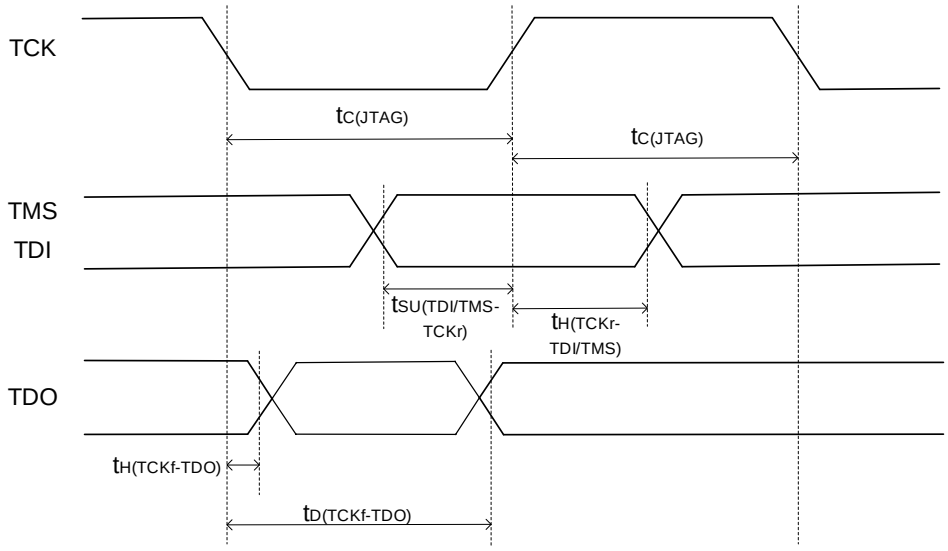
(1) Value guaranteed by design, not 100% tested in production

Table 4-77. JTAG Scan Interface Timing (For GD32G553xxx3) (1)

Symbol	Description	Min	Max	Unit
$t_{C(JTAG)}$	Cycle time, JTAG low and high period	23.5	—	ns
$t_{SU(TDI/TMS - TCKr)}$	Setup time, TDI, TMS before TCK rise (TCKr)	9	—	ns
$t_{H(TCKr -TDI/TMS)}$	Hold time, TDI, TMS after TCKr	2	—	ns
$t_{H(TCKf -TDO)}$	Hold time, TDO after TCKf	8	—	ns
$t_{D(TCKf -TDO)}$	Delay time, TDO valid after TCK fall (TCKf)	—	8.5	ns

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-17. JTAG timing diagram



4.35. SWD Timing

Table 4-78. SWD Interface Timing (For GD32G553xxx7) (1)

Symbol	Description	Min	Max	Unit
$t_{CYC(SWCK)}$	SWCLK clock cycle time	18.5	—	ns
$t_{H(SWCK)}$	SWCLK clock high pulse width	9	—	ns
$t_{L(SWCK)}$	SWCLK clock low pulse width	9	—	ns
$t_{R(SWCK)}$	SWCLK clock rise time	—	1	ns
$t_{F(SWCK)}$	SWCLK clock fall time	—	1	ns
$t_{SU(SWD)}$	SWDIO setup time	7	—	ns
$t_{H(SWD)}$	SWDIO hold time	1	—	ns
$t_{D(SWD)}$	SWDIO data delay time	6	6.5	ns

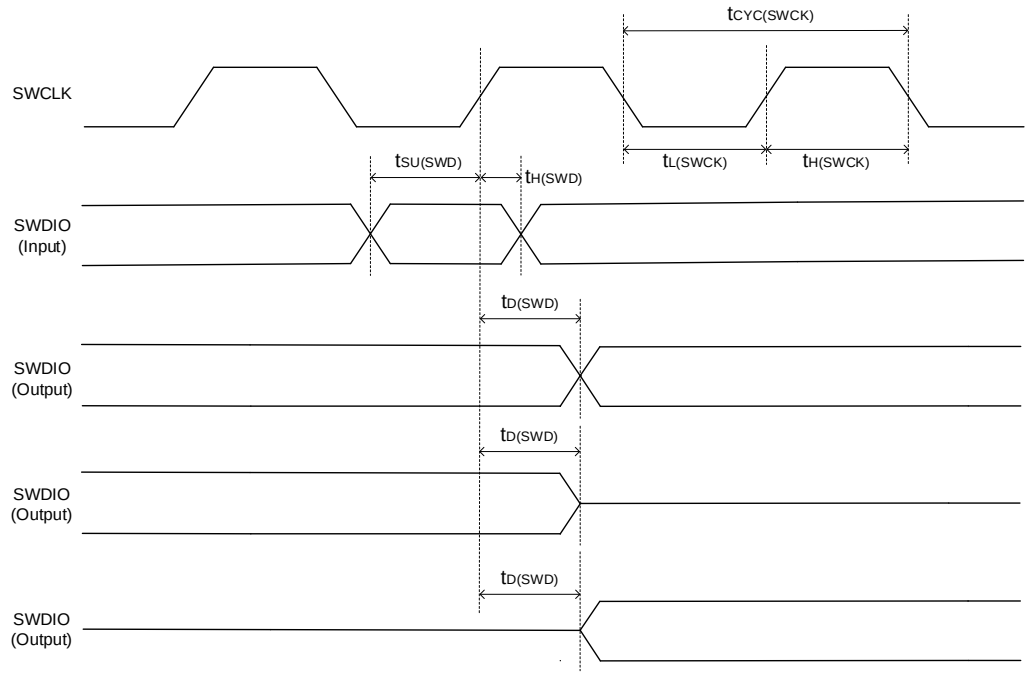
(1) Value guaranteed by design, not 100% tested in production.

Table 4-79. SWD Interface Timing (For GD32G553xxx3) (1)

Symbol	Description	Min	Max	Unit
$t_{CYC(SWCK)}$	SWCLK clock cycle time	23.5	—	ns
$t_{H(SWCK)}$	SWCLK clock high pulse width	10.5	—	ns
$t_{L(SWCK)}$	SWCLK clock low pulse width	10.5	—	ns
$t_{R(SWCK)}$	SWCLK clock rise time	—	2	ns
$t_{F(SWCK)}$	SWCLK clock fall time	—	2	ns
$t_{SU(SWD)}$	SWDIO setup time	9	—	ns
$t_{H(SWD)}$	SWDIO hold time	2	—	ns
$t_{D(SWD)}$	SWDIO data delay time	8	8.5	ns

Value guaranteed by design, not 100% tested in production.

Figure 4-18. SWD timing diagram



5. Package information

5.1. LQFP128 package outline dimensions

Figure 5-1. LQFP128 package outline

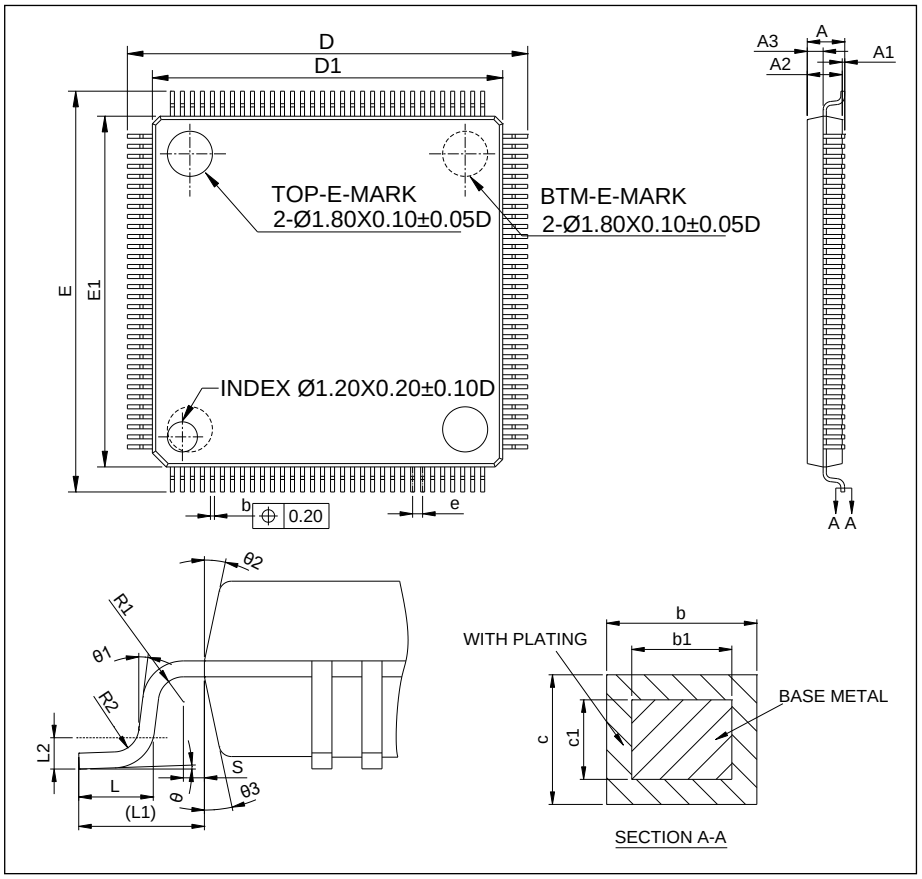


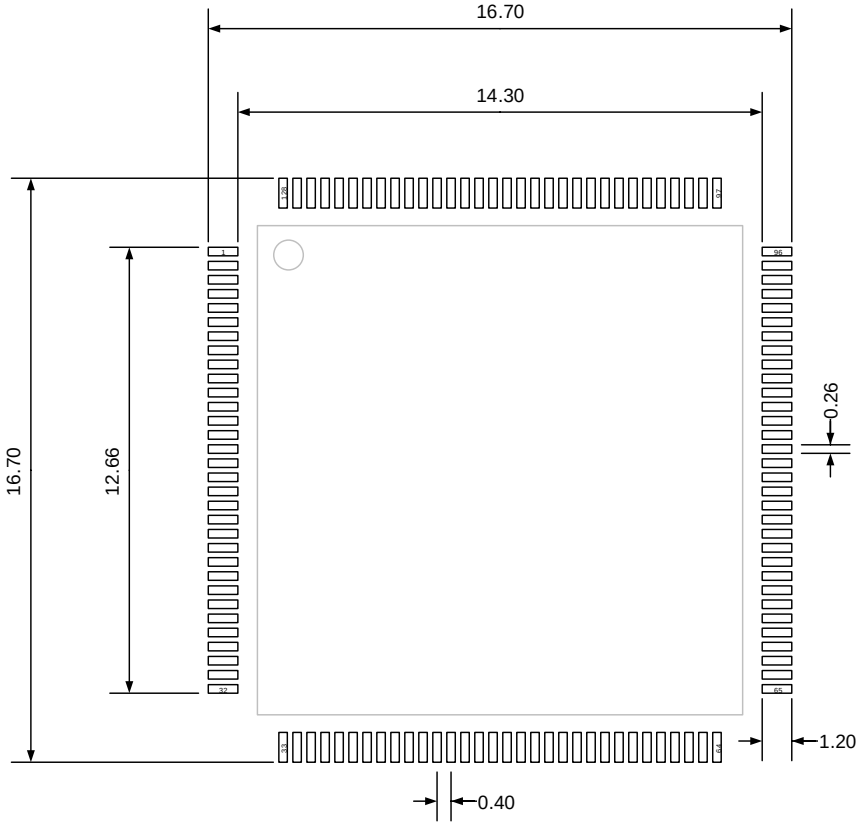
Table 5-1. LQFP128 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.14	—	0.23
b1	0.13	0.16	0.19
c	0.13	—	0.18
c1	0.12	0.127	0.134
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
e	—	0.40	—

Symbol	Min	Typ	Max
L	0.45	0.60	0.75
L1	—	1.00	—
L2	—	0.25	—
R1	0.08	—	—
R2	0.08	—	0.20
S	0.20	—	—
θ	0°	3.5°	7°
θ1	0°	—	—
θ2	11°	12°	13°
θ3	11°	12°	13°

(Original dimensions are in millimeters)

Figure 5-2. LQFP128 recommended footprint



(Original dimensions are in millimeters)

5.2. LQFP100 package outline dimensions

Figure 5-3. LQFP100 package outline

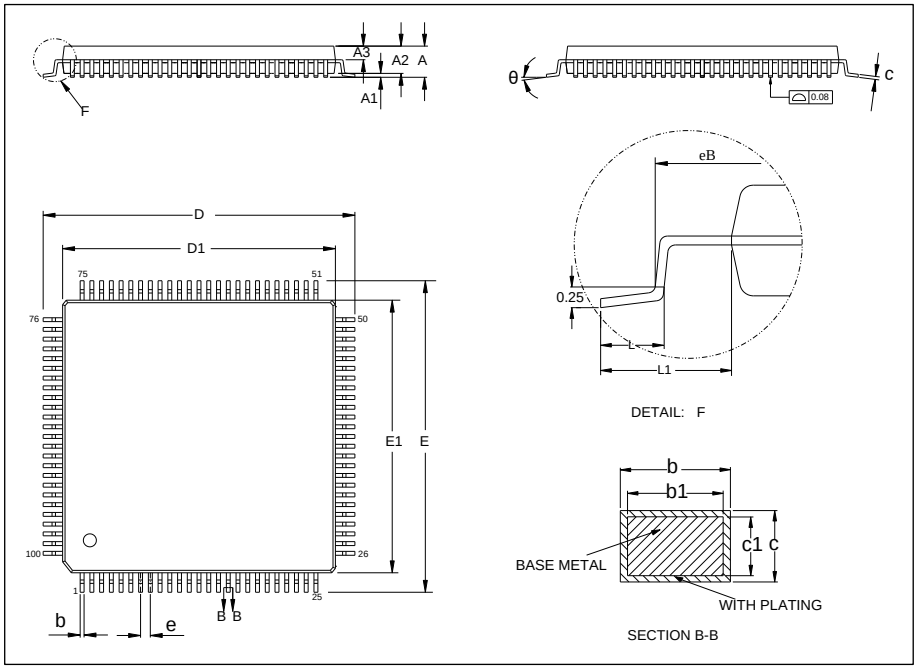
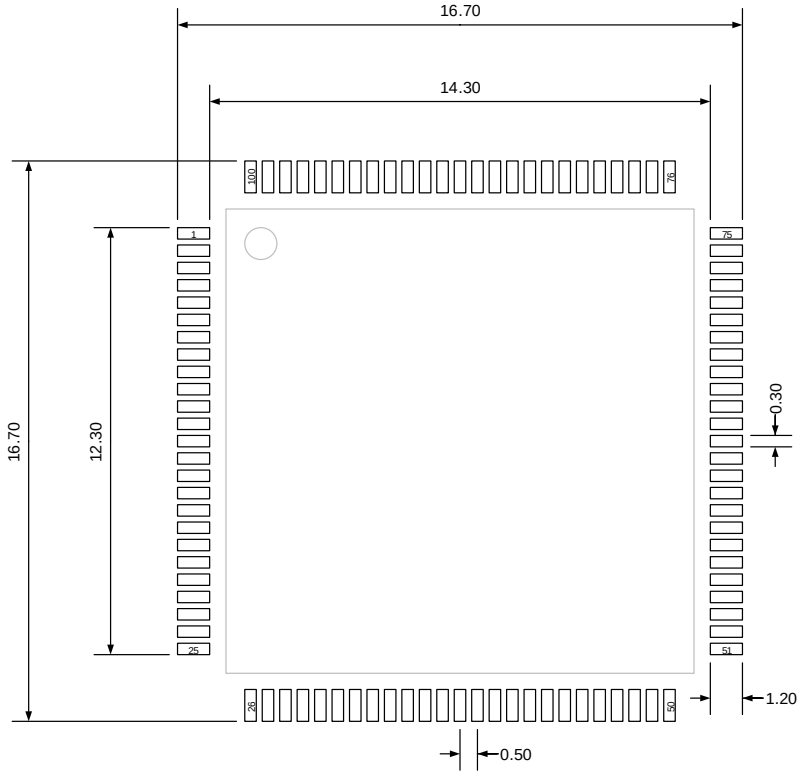


Table 5-2. LQFP100 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17	—	0.27
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
e	0.40	0.50	0.60
eB	15.05	—	15.35
L	0.45	—	0.75
L1	—	1.00	—
θ	0°	—	7°

(Original dimensions are in millimeters)

Figure 5-4. LQFP100 recommended footprint



(Original dimensions are in millimeters)

5.3. WLCSP81 package outline dimensions

Figure 5-5. WLCSP81 package outline

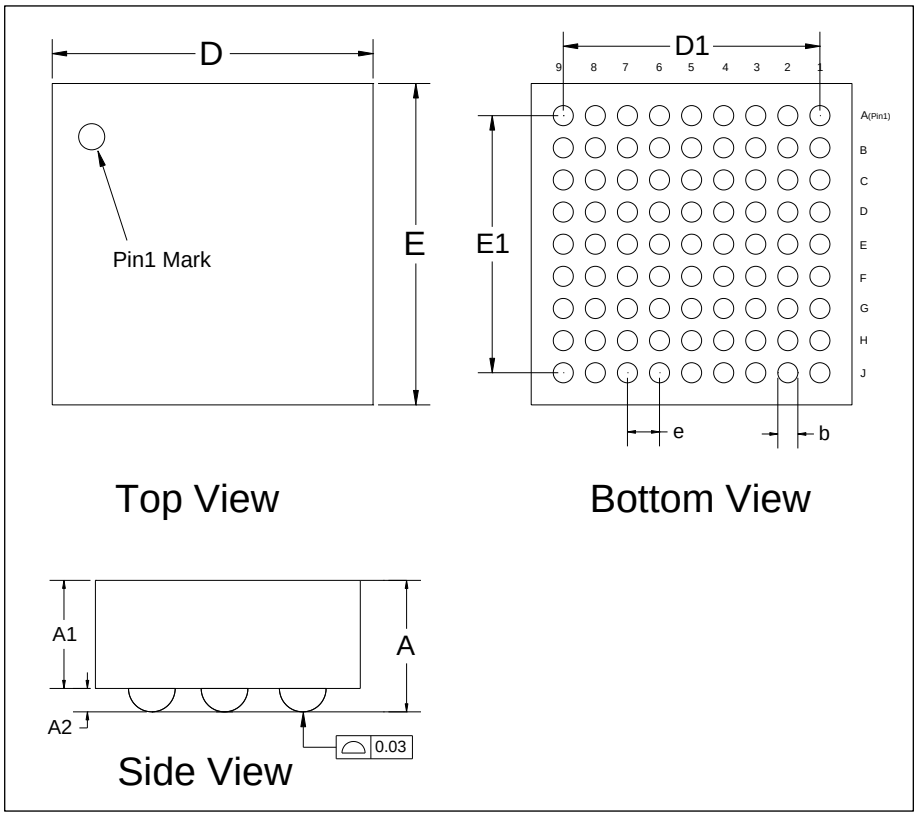
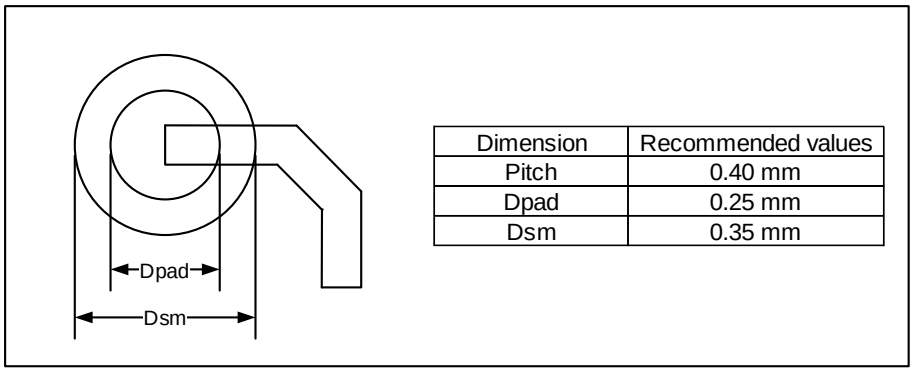


Table 5-3. WLCSP81 package dimensions

Symbol	Min	Typ	Max
A	0.53	0.58	0.63
A1	—	0.43	—
A2	0.12	0.15	0.18
b	0.20	0.25	0.30
D	3.90	4.00	4.10
D1	3.10	3.20	3.30
E	3.90	4.00	4.10
E1	3.10	3.20	3.30
e	0.35	0.40	0.45

(Original dimensions are in millimeters)

Figure 5-6. WLCSP81 recommended footprint



Dimension	Recommended values
Pitch	0.40 mm
Dpad	0.25 mm
Dsm	0.35 mm

(Original dimensions are in millimeters)

5.4. LQFP80 package outline dimensions

Figure 5-7. LQFP80 package outline

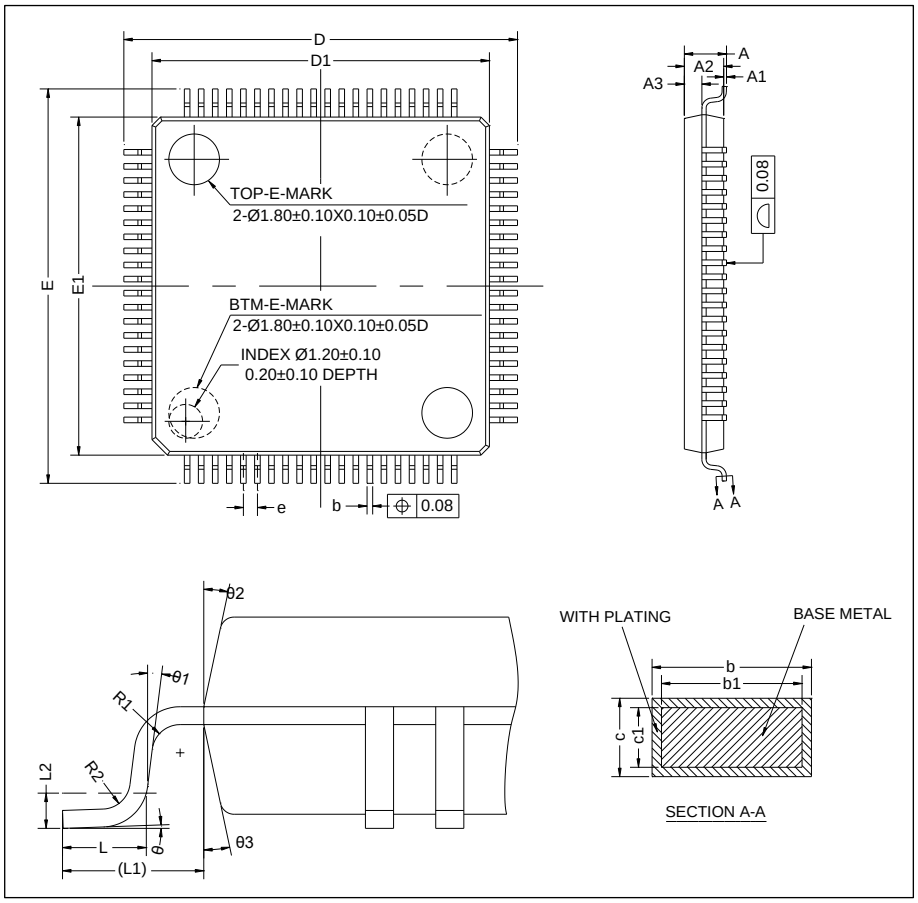


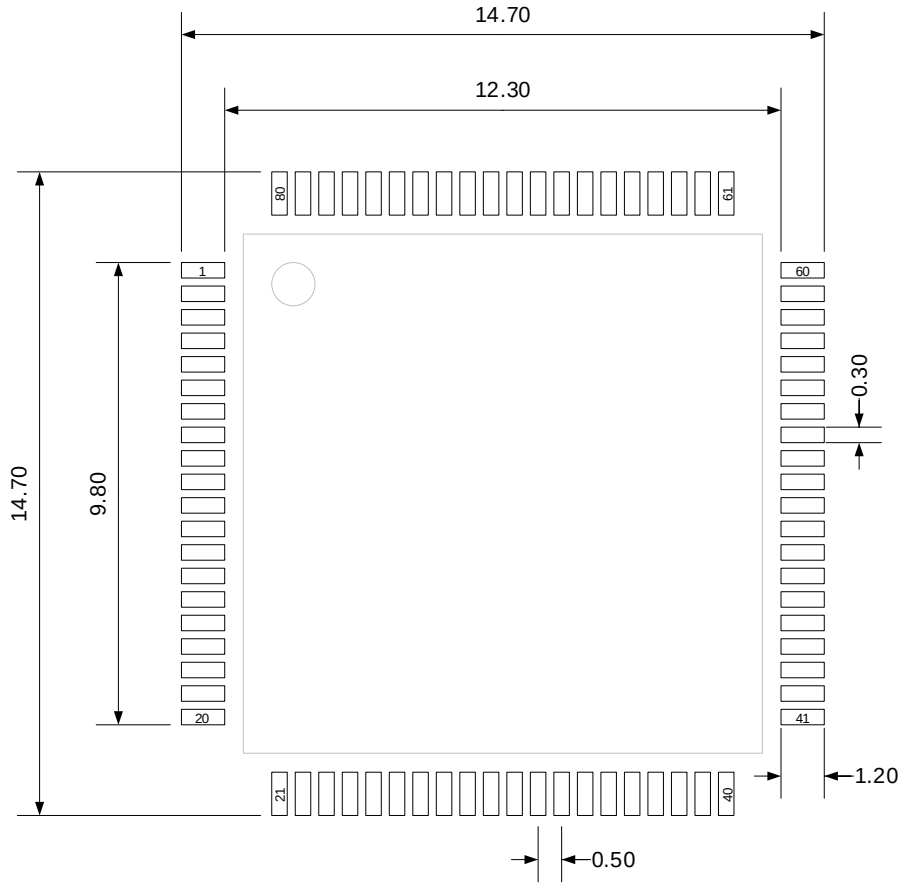
Table 5-4. LQFP80 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.27
b1	0.17	0.20	0.23
c	0.13	—	0.18
c1	0.12	0.127	0.134
D	13.80	14.00	14.20
D1	11.90	12.00	12.10
E	13.80	14.00	14.20
E1	11.90	12.00	12.10
e	—	0.50	—
L	0.45	0.60	0.75
L1	—	1.00	—

Symbol	Min	Typ	Max
L2	—	0.25	—
R1	0.08	—	—
R2	0.08	—	0.20
θ	0°	3.5°	7°
θ1	0°	—	—
θ2	11°	12°	13°
θ3	11°	12°	13°

(Original dimensions are in millimeters)

Figure 5-8. LQFP80 recommended footprint



(Original dimensions are in millimeters)

5.5. LQFP64 package outline dimensions

Figure 5-9. LQFP64 package outline

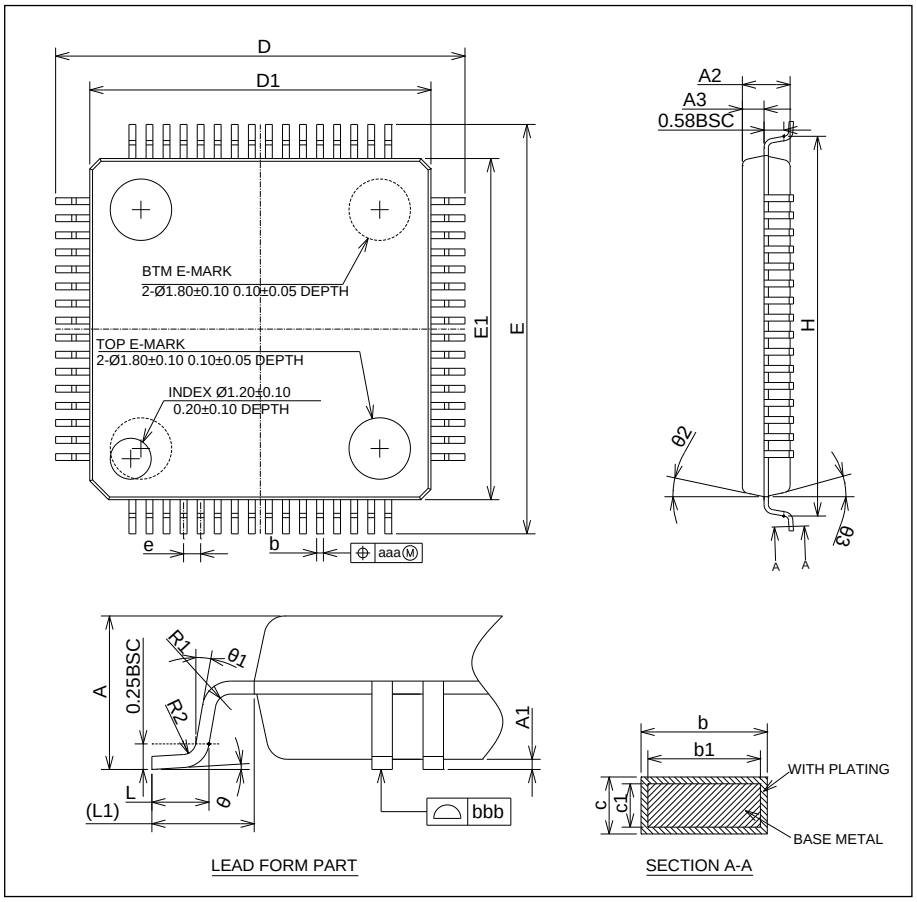


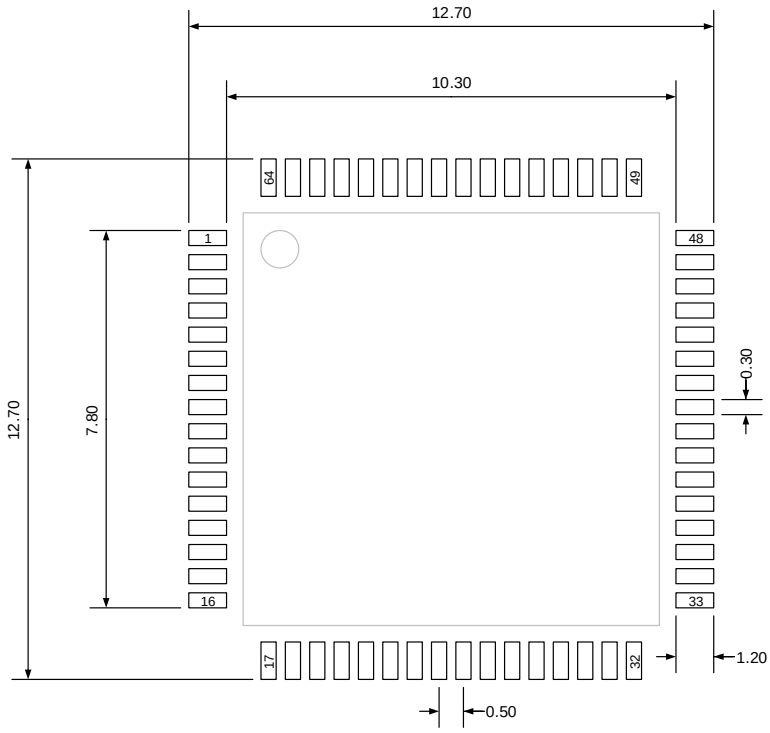
Table 5-5. LQFP64 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.27
b1	0.17	0.20	0.23
c	0.13	—	0.18
c1	0.117	0.127	0.137
D	11.95	12.00	12.05
D1	9.90	10.00	10.10
E	11.95	12.00	12.05
E1	9.90	10.00	10.10
e	0.40	0.50	0.60
H	11.09	11.13	11.17
L	0.53	—	0.70

Symbol	Min	Typ	Max
L1	—	1.00	—
R1	—	0.15	—
R2	—	0.13	—
θ	0°	3.5°	7°
θ1	0°	—	—
θ2	11°	12°	13°
θ3	11°	12°	13°
aaa	—	0.08	—
bbb	—	0.08	—

(Original dimensions are in millimeters)

Figure 5-10. LQFP64 recommended footprint



(Original dimensions are in millimeters)

5.6. LQFP48 package outline dimensions

Figure 5-11. LQFP48 package outline

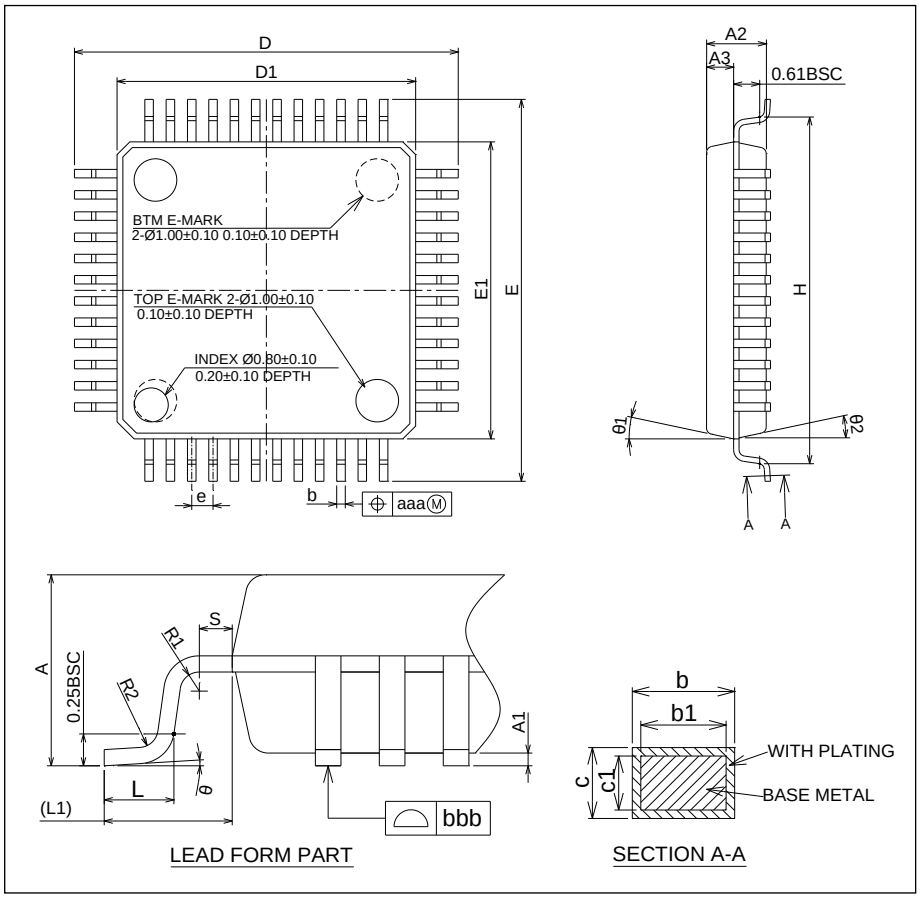


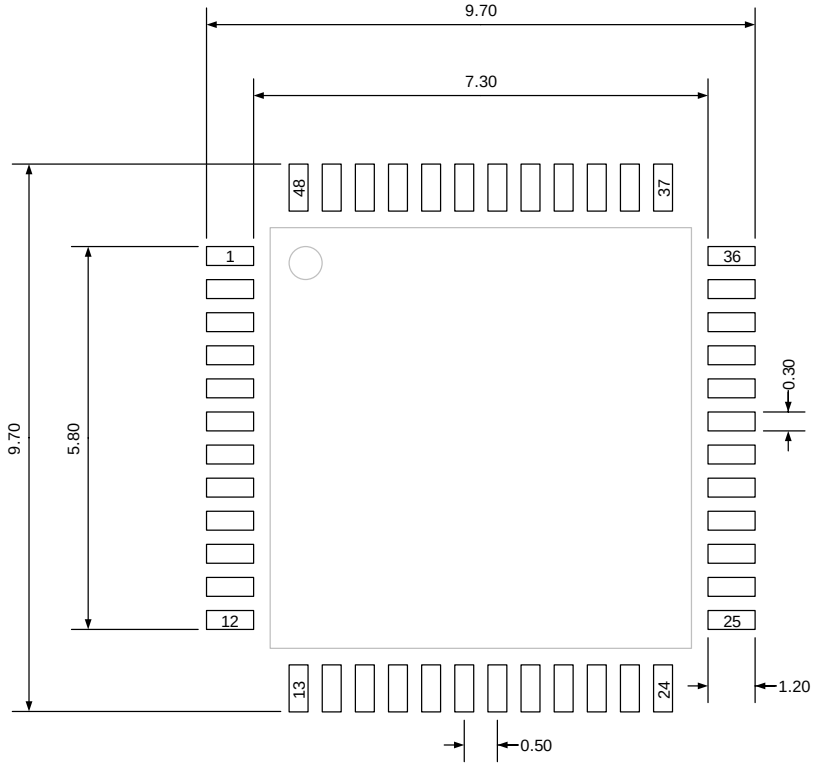
Table 5-6. LQFP48 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.27
b1	0.17	0.20	0.23
c	0.13	—	0.18
c1	0.117	0.127	0.137
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.40	0.50	0.60
H	8.14	8.17	8.20
L	0.50	—	0.70

Symbol	Min	Typ	Max
L1	—	1.00	—
R1	0.08	—	—
R2	0.08	—	0.20
S	0.20	—	—
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°
aaa	—	0.08	—
bbb	—	0.08	—

(Original dimensions are in millimeters)

Figure 5-12. LQFP48 recommended footprint



(Original dimensions are in millimeters)

5.7. QFN48 package outline dimensions

Figure 5-13. QFN48 package outline

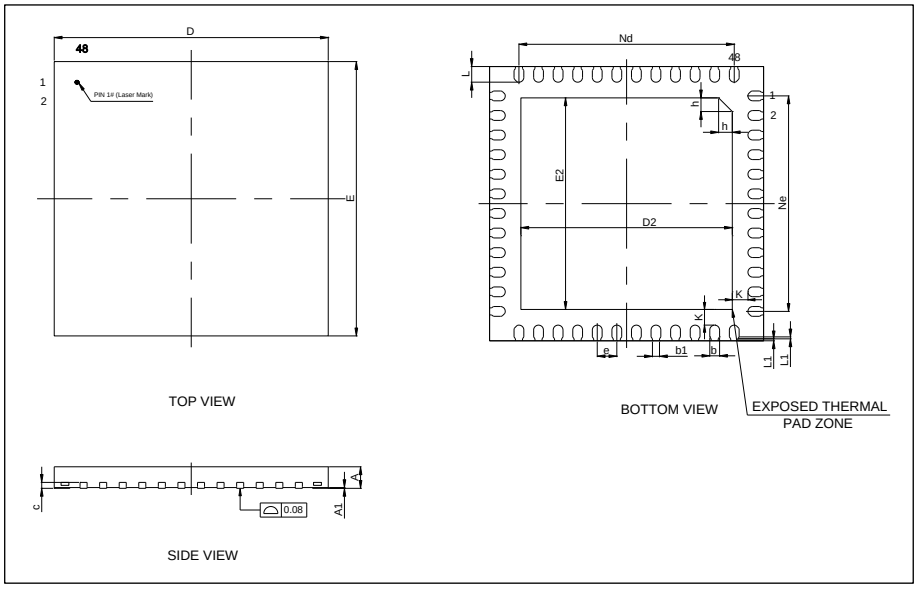
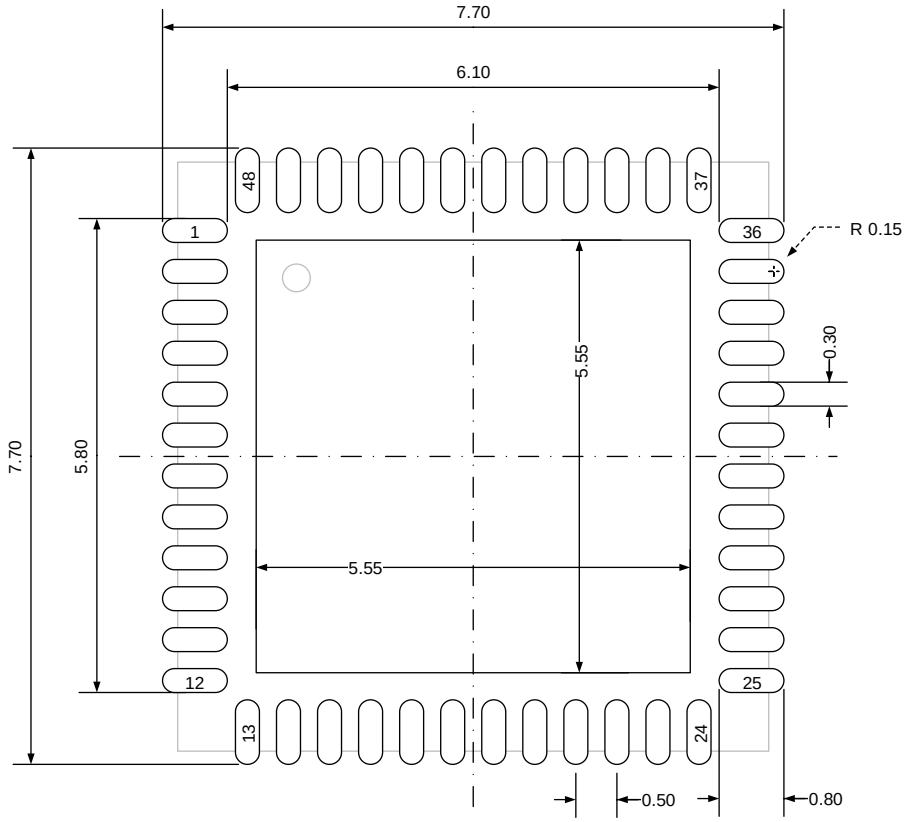


Table 5-7. QFN48 package dimensions

Symbol	Min	Typ	Max
A	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1	—	0.18	—
c	—	0.152	—
D	6.90	7.00	7.10
D2	5.50	5.60	5.70
E	6.90	7.00	7.10
E2	5.50	5.60	5.70
e	—	0.50	—
K	—	0.30	—
L	0.35	0.40	0.45
L1	0	0.05	0.10
h	0.30	0.35	0.40
Nd	—	5.50	—
Ne	—	5.50	—

(Original dimensions are in millimeters)

Figure 5-14. QFN48 recommended footprint



(Original dimensions are in millimeters)

5.8. Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter “θ”. For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

θ_{JA}: Thermal resistance, junction-to-ambient.

θ_{JB}: Thermal resistance, junction-to-board.

θ_{JC}: Thermal resistance, junction-to-case.

Ψ_{JB}: Thermal characterization parameter, junction-to-board.

Ψ_{JT}: Thermal characterization parameter, junction-to-top center.

$$\theta_{JA}=(T_J-T_A)/P_D \quad (5\text{-}1)$$

$$\theta_{JB}=(T_J-T_B)/P_D \quad (5\text{-}2)$$

$$\theta_{JC}=(T_J-T_C)/P_D \quad (5\text{-}3)$$

Where, T_J = Junction temperature.

T_A = Ambient temperature

T_B = Board temperature

T_C = Case temperature which is monitoring on package surface

P_D = Total power dissipation

θ_{JA} represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower θ_{JA} can be considerate as better overall thermal performance.

θ_{JB} is used to measure the heat flow resistance between the chip surface and the PCB board.

θ_{JC} represents the thermal resistance between the chip surface and the package top case. θ_{JC} is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

The maximum chip-junction temperature, T_J max, may be calculated using the following equation: T_J max = T_A max + (P_D max x θ_{JA}) Where:

• T_A max is the maximum ambient temperature in °C,

• θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,

• P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$ max), • P_{INT} max is the product of I_{DD} and V_{DD}. $P_{I/O}$ max represents the maximum power dissipation on output pins expressed in Watts.

Table 5-8. Package thermal characteristics(1)

Symbol	Condition	Package	Value	Unit
θ_{JA}	Natural convection, 2S2P PCB	LQFP128	47.84	°C/W
		LQFP100	49.18	
		WLCSP81	44.90	
		LQFP80	51.81	
		LQFP64	54.57	
		LQFP48	69.64	
		QFN48	28.60	
θ_{JB}	Cold plate, 2S2P PCB	LQFP128	33.88	°C/W
		LQFP100	22.70	
		WLCSP81	9.20	
		LQFP80	33.36	
		LQFP64	35.08	
		LQFP48	43.16	
		QFN48	6.10	
θ_{JC}	Cold plate, 2S2P PCB	LQFP128	7.43	°C/W
		LQFP100	12.52	
		WLCSP81	8.70	
		LQFP80	11.25	
		LQFP64	18.11	
		LQFP48	25.36	
		QFN48	5.62	
Ψ_{JB}	Natural convection, 2S2P PCB	LQFP128	34.06	°C/W
		LQFP100	32.85	
		WLCSP81	7.30	
		LQFP80	33.53	
		LQFP64	35.41	
		LQFP48	47.75	
		QFN48	5.95	
Ψ_{JT}	Natural convection, 2S2P PCB	LQFP128	0.33	°C/W
		LQFP100	0.53	
		WLCSP81	5.70	
		LQFP80	0.49	
		LQFP64	1.10	
		LQFP48	2.45	
		QFN48	0.17	

(1) Thermal characteristics are based on simulation, and meet JEDEC specification.

6. Ordering information

Table 6-1. Part ordering code for GD32G553xx devices

Ordering code	Flash (KB)	Package	Package type	Temperature operating range
GD32G553QET7	512	LQFP128	Green	Industrial -40°C to +105°C
GD32G553QET3	512	LQFP128	Green	Industrial -40°C to +125°C
GD32G553VET7	512	LQFP100	Green	Industrial -40°C to +105°C
GD32G553VET3	512	LQFP100	Green	Industrial -40°C to +125°C
GD32G553MEY7TR	512	WLCSP81	Green	Industrial -40°C to +105°C
GD32G553MET7	512	LQFP80	Green	Industrial -40°C to +105°C
GD32G553MET3	512	LQFP80	Green	Industrial -40°C to +125°C
GD32G553RET7	512	LQFP64	Green	Industrial -40°C to +105°C
GD32G553RET3	512	LQFP64	Green	Industrial -40°C to +125°C
GD32G553CET7	512	LQFP48	Green	Industrial -40°C to +105°C
GD32G553CET3	512	LQFP48	Green	Industrial -40°C to +125°C
GD32G553CEU7	512	QFN48	Green	Industrial -40°C to +105°C
GD32G553CEU3	512	QFN48	Green	Industrial -40°C to +125°C

7. Revision history

Table 7-1. Revision history

Revision No.	Description	Date
1.0	1. Initial Release	Nov.07, 2024
1.1	1. Table number modification, refers to ***Table 2-1. GD32G553xx devices features and peripheral list***.	Nov.19, 2024
1.2	1. Modify PG10-NRST pin name to NRST-PG10, and add notice to this pin, refers to ***Pin definitions*** and ***Pinouts and pin assignment*** chapter. 2. Modify EXMC_NL pin function to EXMC_NL/EXMC_NADV, refers to ***Pin definitions***. 3. Pin name update, please refer to ***Pin definitions***.	Jan.20, 2025
1.3	1. Add five part number: GD32G553VET3, GD32G553MET3, GD32G553RET3, GD32G553CET3, and GD32G553CEU3. 2. Add the difference descriptions among T3 and T7 devices.	Apr.18, 2025
1.4	1. Correct GPIO pin numbers, refers to ***Table 2-1. GD32G553xx devices features and peripheral list***.	May.06, 2025
1.5	1. ***Boot modes*** chapter description modification. 2. Descriptions modification in ***Table 4-17. Voltage reference buffer characteristics(1)***, ***Table 4-22. High speed internal clock (IRC8M) characteristics(1)***, and ***Table 4-43. 1MSPS DAC accuracy(1)***. 3. Parameter value update in ***Table 4-41. Temperature monitoring characteristics***. 4. ***External clock characteristics*** description update. 5. ***High-Resolution Timer (HRTIMER)*** description update. 6. Part number modification, please refer to ***Device information*** and ***Ordering information***. 7. Descriptions modification in ***Table 4-38. 12-bit ADC accuracy(1)***, ***Table 4-29. Output voltage characteristics for all I/Os except PC13, PC14, PC15 (1)(2)***, ***Table 4-5. Start-up timings of Operating conditions(1)(2)(3)***, ***Table 4-10. Power consumption in Deep-sleep mode (1)(2)***, ***Table 4-12. Power consumption in BKP_ONLY mode***, ***Table 4-23. Low speed internal clock (IRC32K)***	Aug.27, 2025

Revision No.	Description	Date
	characteristics, ***Table 4-28. I/O static characteristics***, and ***Table 4-29. Output voltage characteristics for all I/Os except PC13, PC14, PC15*** [1][2].	
1.6	1. Add information of maximum sampling rate of DACs in ***Digital to analog converter (DAC)***. 2. Add USART0 alternate functions to PC0, PC1, and PF10 pins, refer to ***Pin definitions***. 3. Add a new part number: GD32G553QET3.	Nov.26, 2025
1.7	1. ADC descriptions modification, delete VREFN related descriptions, refer to ***Analog to digital converter (ADC)***. 2. Delete VREFN and add notice “VREFN internally connected to VSSA” to ***Table 4-35. ADC characteristics***, ***Table 4-42. 1MSPS DAC characteristics***, and ***Table 4-44. 15MSPS DAC characteristics***.	Jan.15, 2026
2.0	1. Parameters are updated in chapter ***High-precision temperature sensor characteristics*** and ***Temperature sensor characteristics***. 2. By char parameters are updated.	Mar.24, 2026

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