GigaDevice Semiconductor Inc.

GD32F5HCxx
Arm® Cortex®-M33 32-bit MCU

Datasheet

Revision 1.0

(Apr. 2026)

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1. General description

The GD32F5HCxx is a highly integrated IC or SoC that includes an ARM® Cortex®-M33 processor with Trustzone. It is an optimized SoC designed for a broad range of smart devices for Internet of Things (IoT) applications. The Cortex®-M33 processor is a 32-bit processor that possesses low interrupt latency and low-cost debug. The characteristics of integrated and advanced make the Cortex®-M33 processor suitable for market products that require microcontrollers with high performance and low power consumption. The Cortex®-M33 processor is based on the ARMv8 architecture and supports a powerful and scalable instruction set including general data processing I/O control tasks, advanced data processing bit field manipulations and DSP.

The GD32F5HCxx device incorporates the Arm® Cortex®-M33 32-bit processor core operating at up to 200 MHz frequency to obtain maximum efficiency. It provides up to 2048 KB on-chip Flash memory and up to 320 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer a 12-bit ADC, up to four general 16-bit timers, two general 32-bit timers, one basic timer, one PWM advanced timer, as well as standard and advanced communication interfaces: up to two SPIs, a SQPI, two I2Cs, three USARTs, one I2S and an USBFS. Additional peripherals as TrustZone protection controller union (TZPCU), quad-SPI interface (QSPI) are included.

The device operates from a 2.7 to 3.63 V power supply and is available within a –40 to +85 °C temperature range. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make the GD32F5HCxx devices suitable for a wide range of applications, especially in areas such as industrial control, motor drives, user interface, power monitor and alarm systems, consumer and handheld equipment, gaming and GPS, E-bike, optical module and so on.

2. Device overview

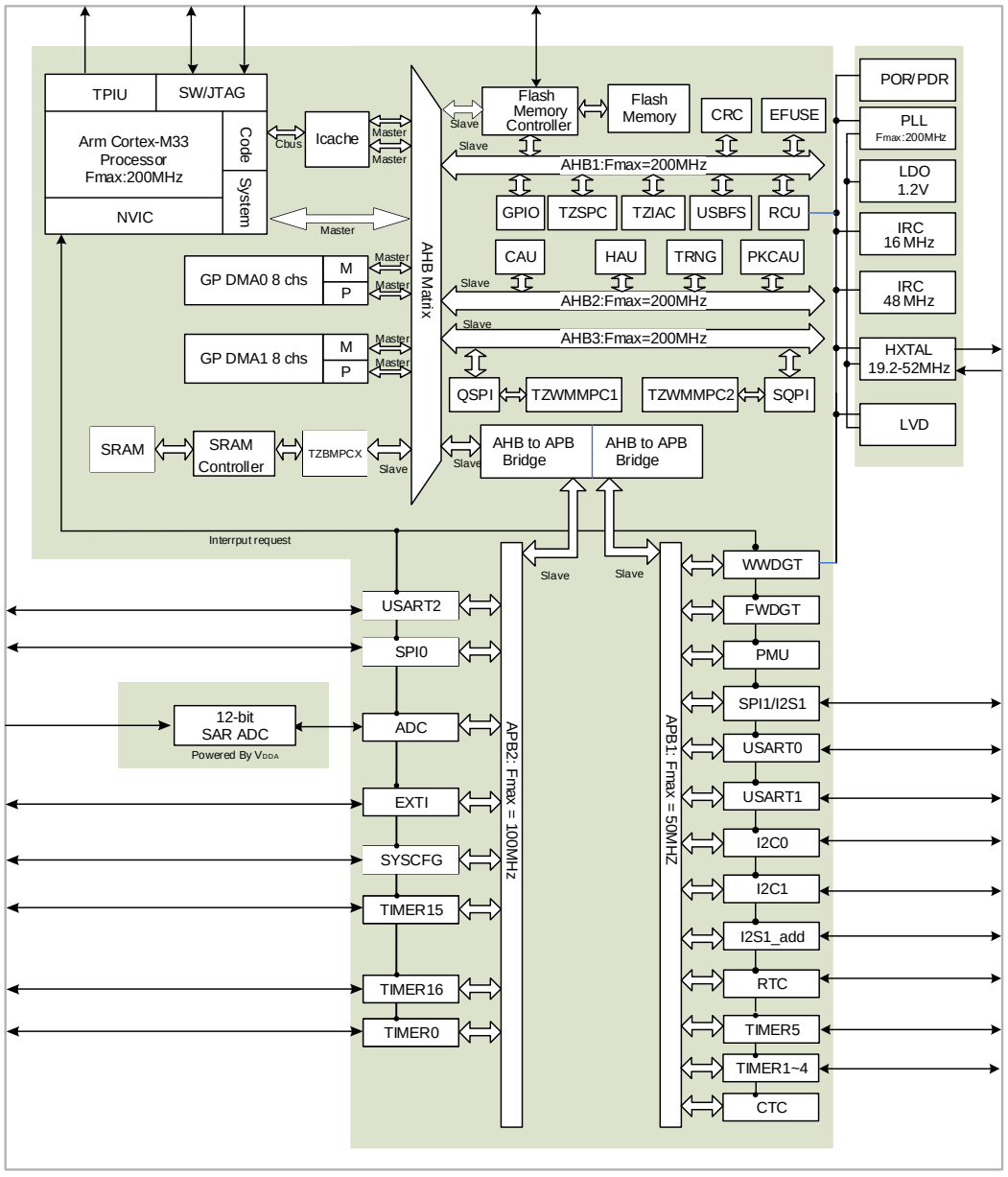
2.1. Device information

Table 2-1. GD32F5HCxx devices features and peripheral list

Part Number		GD32F5HCxx		
		RIL6	PIQ6	PIQ7
FLASH (KB)		2048	2048	2048
SRAM (KB)		320	320	320
Timers	General timer(16-bit)	4 (3-4,15-16)	4 (3-4,15-16)	4 (3-4,15-16)
	General timer(32-bit)	2 (1-2)	2 (1-2)	2 (1-2)
	Advanced timer(16-bit)	1 (0)	1 (0)	1 (0)
	SysTick	1	1	1
	Basic timer(16-bit)	1 (5)	1 (5)	1 (5)
	Watchdog	2	2	2
	RTC	1	1	1
Connectivity	USART	3 (0-2)	3 (0-2)	3 (0-2)
	I2C	2 (0-1)	2 (0-1)	2 (0-1)
	SPI/I2S	2/1 (0-1)/(1)	2/1 (0-1)/(1)	2/1 (0-1)/(1)
	QSPI	1	1	1
	SQPI	1	1	1
	USBFS	1	1	1
GPIO		54	50	50
TZPCU		1	1	1
ADC	Units	1	1	1
	Channels	12	11	11
Package		BGA64		QFN56

2.2. Block diagram

Figure 2-1. GD32F5HCxx block diagram



2.3. Pinouts and pin assignment

Figure 2-2. GD32F5HCRIx6 BGA64 pinouts

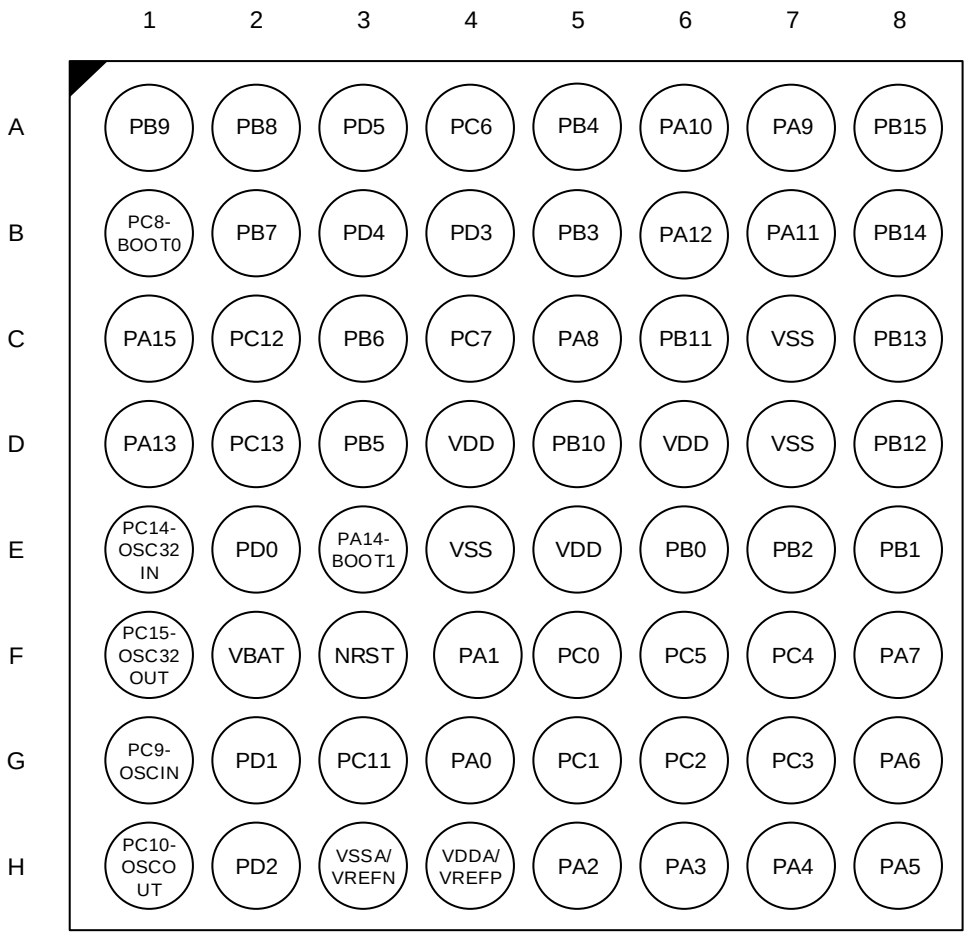
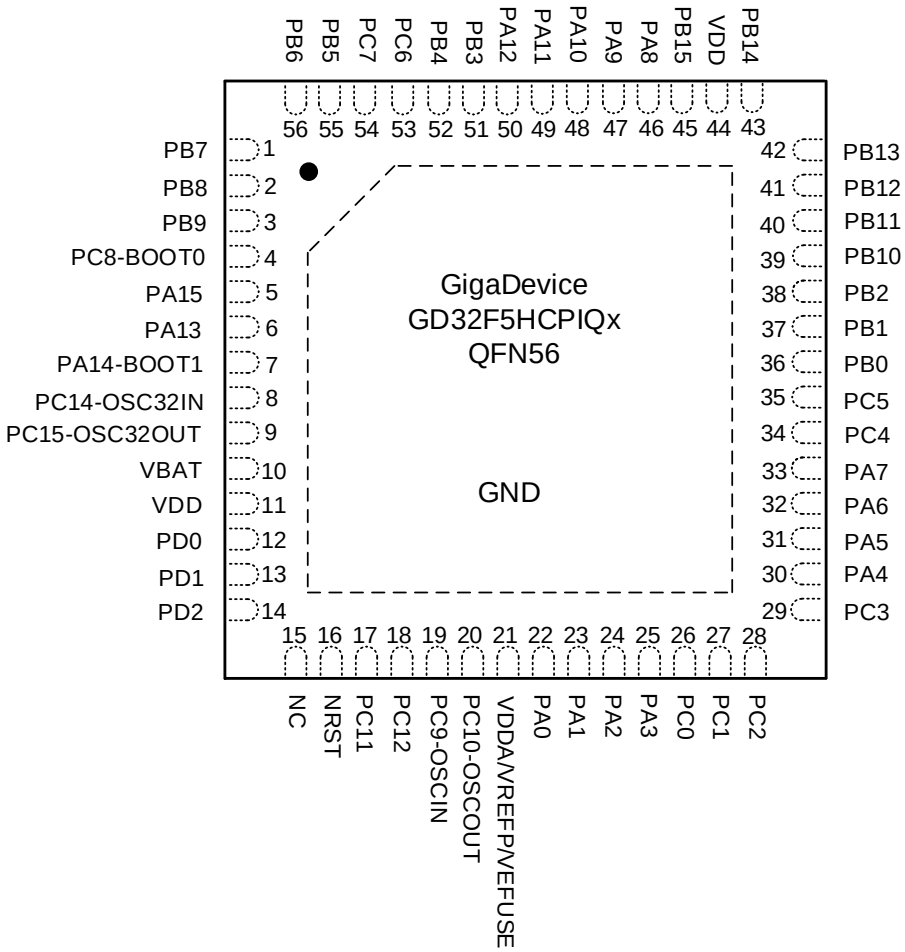


Figure 2-3. GD32F5HCPIQx QFN56 pinouts



2.4. Memory map

Table 2-2. GD32F5HCxx memory map

Pre-defined Regions	Bus	Secure boundary address	Non-Secure boundary address	Peripherals
Cortex M33	-	-	0xE000 1000 - 0xE00F FFFF	Cortex M33 internal peripherals
External device	AHB3	-	0x9800 0000 - 0xDFFF FFFF	Reserved
		-	0x9000 0000 - 0x97FF FFFF	QSPI_FLASH(MEM)
		-	0x7000 0000 - 0x8FFF FFFF	Reserved
		-	0x6000 0000 - 0x6FFF FFFF	SQPI_PSRAM(MEM)
Peripheral	AHB2	0x5C06 3000 - 0x5FFF FFFF	0x4C06 3000 - 0x4FFF FFFF	Reserved
		0x5C06 1000 - 0x5C06 2FFF	0x4C06 1000 - 0x4C06 2FFF	PKCAU
		0x5C06 0C00 - 0x5C06 0FFF	0x4C06 0C00 - 0x4C06 0FFF	Reserved
		0x5C06 0800 - 0x5C06 0BFF	0x4C06 0800 - 0x4C06 0BFF	TRNG
		0x5C06 0400 - 0x5C06 07FF	0x4C06 0400 - 0x4C06 07FF	HAU
		0x5C06 0000 - 0x5C06 03FF	0x4C06 0000 - 0x4C06 03FF	CAU
		0x5C05 0400 - 0x5C05 FFFF	0x4C05 0400 - 0x4C05 FFFF	Reserved
		0x5C05 0000 - 0x5C05 03FF	0x4C05 0000 - 0x4C05 03FF	Reserved
		0x5C04 0000 - 0x5C04 FFFF	0x4C04 0000 - 0x4C04 FFFF	Reserved
		0x5C00 0000 - 0x5C03 FFFF	0x4C00 0000 - 0x4C03 FFFF	Reserved
	AHB1	0x5904 0000 - 0x5BFF FFFF	0x4904 0000 - 0x4BFF FFFF	Reserved
		0x5900 0000 - 0x5903 FFFF	0x4900 0000 - 0x4903 FFFF	USBFS
		0x500B 1000 - 0x58FF FFFF	0x400B 1000 - 0x48FF FFFF	Reserved
		0x500B 0800 - 0x500B 0FFF	0x400B 0800 - 0x400B 0FFF	Reserved
		0x500B 0400 - 0x500B 07FF	0x400B 0400 - 0x400B 07FF	TZBMPC3
		0x500B 0000 - 0x500B 03FF	0x400B 0000 - 0x400B 03FF	TZBMPC2
		0x500A 1000 - 0x500A FFFF	0x400A 1000 - 0x400A FFFF	Reserved
		0x500A 0C00 - 0x500A 0FFF	0x400A 0C00 - 0x400A 0FFF	TZBMPC1
		0x500A 0800 - 0x500A 0BFF	0x400A 0800 - 0x400A 0BFF	TZBMPC0
		0x500A 0400 - 0x500A 07FF	0x400A 0400 - 0x400A 07FF	TZIAC
		0x500A 0000 - 0x500A 03FF	0x400A 0000 - 0x400A 03FF	TZSPC
		0x5008 0400 - 0x5009 FFFF	0x4008 0400 - 0x4009 FFFF	Reserved
		0x5008 0000 - 0x5008 03FF	0x4008 0000 - 0x4008 03FF	ICACHE
		0x5003 3000 - 0x5007 FFFF	0x4003 3000 - 0x4007 FFFF	Reserved
		0x5003 0000 - 0x5003 2FFF	0x4003 0000 - 0x4003 2FFF	Reserved
		0x5002 BC00 - 0x5002 FFFF	0x4002 BC00 - 0x4002 FFFF	Reserved
		0x5002 B000 - 0x5002 BBFF	0x4002 B000 - 0x4002 BBFF	Reserved
		0x5002 A000 - 0x5002 AFFF	0x4002 A000 - 0x4002 AFFF	Reserved
		0x5002 8000 - 0x5002 9FFF	0x4002 8000 - 0x4002 9FFF	Reserved
		0x5002 6800 - 0x5002 7FFF	0x4002 6800 - 0x4002 7FFF	Reserved
		0x5002 6400 - 0x5002 67FF	0x4002 6400 - 0x4002 67FF	DMA1

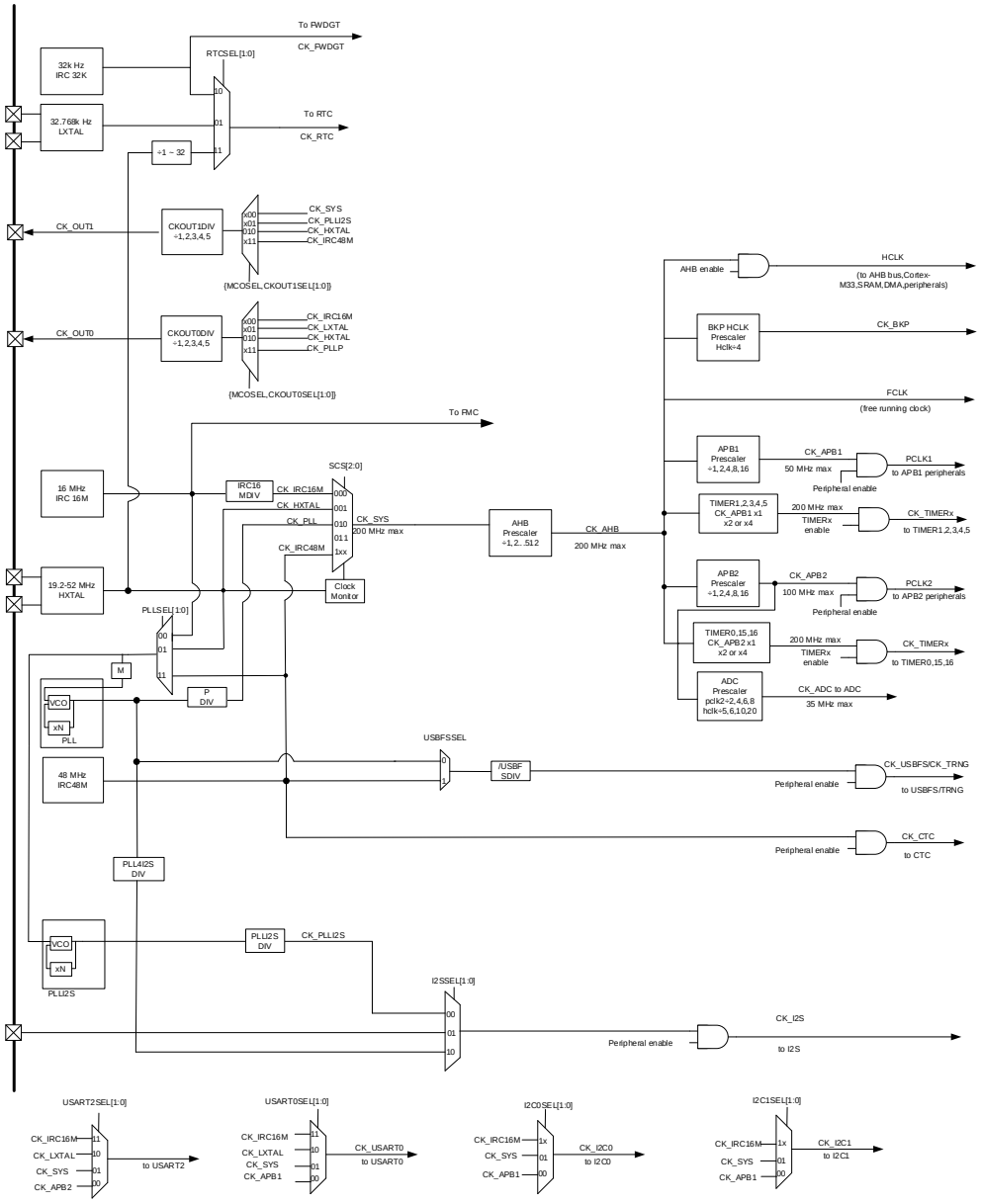
Pre-defined Regions	Bus	Secure boundary address	Non-Secure boundary address	Peripherals
		0x5002 6000 - 0x5002 63FF	0x4002 6000 - 0x4002 63FF	DMA0
		0x5002 5C00 - 0x5002 5FFF	0x4002 5C00 - 0x4002 5FFF	Reserved
		0x5002 5800 - 0x5002 5BFF	0x4002 5800 - 0x4002 5BFF	QSPI_FLASH(REG)
		0x5002 5400 - 0x5002 57FF	0x4002 5400 - 0x4002 57FF	SQPI_PSRAM(REG)
		0x5002 5000 - 0x5002 53FF	0x4002 5000 - 0x4002 53FF	Reserved
		0x5002 4000 - 0x5002 4FFF	0x4002 4000 - 0x4002 4FFF	Reserved
		0x5002 3C00 - 0x5002 3FFF	0x4002 3C00 - 0x4002 3FFF	Reserved
		0x5002 3800 - 0x5002 3BFF	0x4002 3800 - 0x4002 3BFF	RCU
		0x5002 3400 - 0x5002 37FF	0x4002 3400 - 0x4002 37FF	Reserved
		0x5002 3000 - 0x5002 33FF	0x4002 3000 - 0x4002 33FF	CRC
		0x5002 2C00 - 0x5002 2FFF	0x4002 2C00 - 0x4002 2FFF	Reserved
		0x5002 2800 - 0x5002 2BFF	0x4002 2800 - 0x4002 2BFF	EFUSE
		0x5002 2400 - 0x5002 27FF	0x4002 2400 - 0x4002 27FF	Reserved
		0x5002 2000 - 0x5002 23FF	0x4002 2000 - 0x4002 23FF	FMC
		0x5002 1C00 - 0x5002 1FFF	0x4002 1C00 - 0x4002 1FFF	Reserved
		0x5002 1800 - 0x5002 1BFF	0x4002 1800 - 0x4002 1BFF	Reserved
		0x5002 1400 - 0x5002 17FF	0x4002 1400 - 0x4002 17FF	Reserved
		0x5002 1000 - 0x5002 13FF	0x4002 1000 - 0x4002 13FF	Reserved
		0x5002 0C00 - 0x5002 0FFF	0x4002 0C00 - 0x4002 0FFF	GPIOD
		0x5002 0800 - 0x5002 0BFF	0x4002 0800 - 0x4002 0BFF	GPIOC
		0x5002 0400 - 0x5002 07FF	0x4002 0400 - 0x4002 07FF	GPIOB
		0x5002 0000 - 0x5002 03FF	0x4002 0000 - 0x4002 03FF	GPIOA
	APB2	0x5001 8800 - 0x5001 FFFF	0x4001 8800 - 0x4001 FFFF	Reserved
		0x5001 8400 - 0x5001 87FF	0x4001 8400 - 0x4001 87FF	TIMER16
		0x5001 8000 - 0x5001 83FF	0x4001 8000 - 0x4001 83FF	TIMER15
		0x5001 7C00 - 0x5001 7FFF	0x4001 7C00 - 0x4001 7FFF	Reserved
		0x5001 7800 - 0x5001 7BFF	0x4001 7800 - 0x4001 7BFF	Reserved
		0x5001 6800 - 0x5001 77FF	0x4001 6800 - 0x4001 77FF	Reserved
		0x5001 6000 - 0x5001 67FF	0x4001 6000 - 0x4001 67FF	Reserved
		0x5001 5800 - 0x5001 5FFF	0x4001 5800 - 0x4001 5FFF	Reserved
		0x5001 5400 - 0x5001 57FF	0x4001 5400 - 0x4001 57FF	Reserved
		0x5001 4C00 - 0x5001 53FF	0x4001 4C00 - 0x4001 53FF	Reserved
		0x5001 4800 - 0x5001 4BFF	0x4001 4800 - 0x4001 4BFF	Reserved
		0x5001 4400 - 0x5001 47FF	0x4001 4400 - 0x4001 47FF	Reserved
		0x5001 4000 - 0x5001 43FF	0x4001 4000 - 0x4001 43FF	Reserved
		0x5001 3C00 - 0x5001 3FFF	0x4001 3C00 - 0x4001 3FFF	EXTI
		0x5001 3800 - 0x5001 3BFF	0x4001 3800 - 0x4001 3BFF	SYSCFG
		0x5001 3400 - 0x5001 37FF	0x4001 3400 - 0x4001 37FF	Reserved
		0x5001 3000 - 0x5001 33FF	0x4001 3000 - 0x4001 33FF	SPI0
		0x5001 2C00 - 0x5001 2FFF	0x4001 2C00 - 0x4001 2FFF	Reserved

Pre-defined Regions	Bus	Secure boundary address	Non-Secure boundary address	Peripherals
		0x5001 2400 - 0x5001 2BFF	0x4001 2400 - 0x4001 2BFF	Reserved
		0x5001 2000 - 0x5001 23FF	0x4001 2000 - 0x4001 23FF	ADC
		0x5001 1400 - 0x5001 1FFF	0x4001 1400 - 0x4001 1FFF	Reserved
		0x5001 1000 - 0x5001 13FF	0x4001 1000 - 0x4001 13FF	USART2
		0x5001 0800 - 0x5001 0FFF	0x4001 0800 - 0x4001 0FFF	Reserved
		0x5001 0400 - 0x5001 07FF	0x4001 0400 - 0x4001 07FF	Reserved
		0x5001 0000 - 0x5001 03FF	0x4001 0000 - 0x4001 03FF	TIMER0
	APB1	0x5000 7400 - 0x5000 FFFF	0x4000 D000 - 0x4000 FFFF	Reserved
		0x5000 CC00 - 0x5000 CFFF	0x4000 CC00 - 0x4000 CFFF	Reserved
		0x5000 7400 - 0x5000 CBFF	0x4000 7400 - 0x4000 CBFF	Reserved
		0x5000 7000 - 0x5000 73FF	0x4000 7000 - 0x4000 73FF	PMU
		0x5000 6C00 - 0x5000 6FFF	0x4000 6C00 - 0x4000 6FFF	CTC
		0x5000 5C00 - 0x5000 6BFF	0x4000 5C00 - 0x4000 6BFF	Reserved
		0x5000 5800 - 0x5000 5BFF	0x4000 5800 - 0x4000 5BFF	I2C1
		0x5000 5400 - 0x5000 57FF	0x4000 5400 - 0x4000 57FF	I2C0
		0x5000 4C00 - 0x5000 53FF	0x4000 4C00 - 0x4000 53FF	Reserved
		0x5000 4800 - 0x5000 4BFF	0x4000 4800 - 0x4000 4BFF	USART0
		0x5000 4400 - 0x5000 47FF	0x4000 4400 - 0x4000 47FF	USART1
		0x5000 4000 - 0x5000 43FF	0x4000 4000 - 0x4000 43FF	Reserved
		0x5000 3C00 - 0x5000 3FFF	0x4000 3C00 - 0x4000 3FFF	Reserved
		0x5000 3800 - 0x5000 3BFF	0x4000 3800 - 0x4000 3BFF	SPI1/I2S1
		0x5000 3400 - 0x5000 37FF	0x4000 3400 - 0x4000 37FF	I2S1_add
		0x5000 3000 - 0x5000 33FF	0x4000 3000 - 0x4000 33FF	FWDGT
		0x5000 2C00 - 0x5000 2FFF	0x4000 2C00 - 0x4000 2FFF	WWDGT
		0x5000 2800 - 0x5000 2BFF	0x4000 2800 - 0x4000 2BFF	RTC
		0x5000 2400 - 0x5000 27FF	0x4000 2400 - 0x4000 27FF	Reserved
		0x5000 2000 - 0x5000 23FF	0x4000 2000 - 0x4000 23FF	Reserved
		0x5000 1C00 - 0x5000 1FFF	0x4000 1C00 - 0x4000 1FFF	Reserved
		0x5000 1800 - 0x5000 1BFF	0x4000 1800 - 0x4000 1BFF	Reserved
		0x5000 1400 - 0x5000 17FF	0x4000 1400 - 0x4000 17FF	Reserved
		0x5000 1000 - 0x5000 13FF	0x4000 1000 - 0x4000 13FF	TIMER5
		0x5000 0C00 - 0x5000 0FFF	0x4000 0C00 - 0x4000 0FFF	TIMER4
		0x5000 0800 - 0x5000 0BFF	0x4000 0800 - 0x4000 0BFF	TIMER3
		0x5000 0400 - 0x5000 07FF	0x4000 0400 - 0x4000 07FF	TIMER2
		0x5000 0000 - 0x5000 03FF	0x4000 0000 - 0x4000 03FF	TIMER1
SRAM	AHB	0x3005 0000 - 0x3FFF FFFF	0x2005 0000 - 0x2FFF FFFF	Reserved
		0x3003 0000 - 0x3004 FFFF	0x2003 0000 - 0x2004 FFFF	SRAM3 (128KB)
		0x3002 0000 - 0x3002 FFFF	0x2002 0000 - 0x2002 FFFF	SRAM2 (64KB)
		0x3001 0000 - 0x3001 FFFF	0x2001 0000 - 0x2001 FFFF	SRAM1 (64KB)
		0x3000 0000 - 0x3000 FFFF	0x2000 0000 - 0x2000 FFFF	SRAM0 (64KB)

Pre-defined Regions	Bus	Secure boundary address	Non-Secure boundary address	Peripherals
Code	AHB	-	0x1000 0000 - 0x1FFF FFFF	External memories remap
		0x0FFC 0100 - 0x0FFF FFFF	0x0BFC 0000 - 0x0BFF FFFF	Reserved
		0x0FFC 0000 - 0x0FFC 00FF	-	EFUSE (256B)
		0x0FF8 8000 - 0x0FFB FFFF	0x0BF8 8000 – 0x0BFB FFFF	Reserved
		0x0FF8 4000 – 0x0FF8 7FFF	-	ROM(16KB)
		0x0FF8 0000 – 0x0FF8 3FFF	-	GSSA(16KB)
		0x0FF4 E000 – 0x0FF7 FFFF	-	ROM(200KB)
		-	0x0BF4 6000 –0x0BF8 7FFF	Reserved
		-	0x0BF4 0000 - 0x0BF4 5FFF	ROM(24KB)
		0x0E05 0000 - 0x0FF4 DFFF	0x0A05 0000 - 0x0BF3 FFFF	Reserved
		0x0E03 0000 - 0x0E04 FFFF	0x0A03 0000 - 0x0A04 FFFF	SRAM3 (128KB)
		0x0E02 0000 - 0x0E02 FFFF	0x0A02 0000 - 0x0A02 FFFF	SRAM2 (64KB)
		0x0E01 0000 - 0x0E01 FFFF	0x0A01 0000 - 0x0A01 FFFF	SRAM1 (64KB)
		0x0E00 0000 - 0x0E00 FFFF	0x0A00 0000 - 0x0A00 FFFF	SRAM0 (64KB)
		0x0C20 0000 - 0x0DFF FFFF	0x0820 0000 - 0x09FF FFFF	Reserved
		0x0C00 0000 - 0x0C1F FFFF	0x0800 0000 - 0x081F FFFF	Flash memory (2048KB)
		-	0x0000 0000 - 0x07FF FFFF	External memories remap

2.5. Clock tree

Figure 2-4. GD32F5HCxx clock tree



Legend:

HXTAL: High speed crystal oscillator

LXTAL: Low speed crystal oscillator

IRC48M: Internal 48M RC oscillator

IRC16M: Internal 16M RC oscillator

IRC32K: Internal 32K RC oscillator

2.6. Pin definitions

2.6.1. GD32F5HCRIx6 BGA64 pin definitions

Table 2-3. GD32F5HCRIx6 BGA64 pin definitions

GD32F5HCRIx6 BGA64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PB7	B2	I/O	5VT	Default: PB7 Alternate: I2S1_WS, SPI1_NSS, EVENTOUT, TRACED1, TIMER3_CH1, I2C0_SDA, USART0_RX
PB8	A2	I/O	5VT	Default: PB8 Alternate: SPI1_SCK, EVENTOUT, TRACED2, TIMER3_CH2
PB9	A1	I/O	5VT	Default: PB9 Alternate: I2S1_SD, SPI1_MOSI, EVENTOUT, TRACED3, TIMER1_CH1, TIMER3_CH3
PC8-BOOT0	B1	I/O	5VT	Default: PC8 Alternate: I2C0_SDA, USART0_TX, I2C1_SDA, EVENTOUT, TIMER2_CH2, USBFS_SOF, TIMER3_ETI Additional: BOOT0
PA15-WKUP1	C1	I/O	5VT	Default: JTDI, PA15 Alternate: I2C0_SCL, USART0_RX, I2C1_SCL, EVENTOUT, SPI0_NSS, TIMER3_CH0 Additional: WKUP1
PA13	D1	I/O	5VT	Default: JTMS, SWDIO, PA13 Alternate: USART0_CTS, USART1_CTS, I2C0_SMBA, EVENTOUT
PA14-BOOT1	E3	I/O	5VT	Default: JTCK, SWCLK, PA14 Alternate: USART0_RTS, USART1_RTS, I2C1_SMBA, EVENTOUT, I2C0_SDA Additional: BOOT1
PC14-OSC32IN	E1	I/O	5VT	Default: PC14 Alternate: USART0_CK, USART1_CK, EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	F1	I/O	5VT	Default: PC15 Alternate: IFRP_OUT, EVENTOUT Additional: RTC_TAMP0, RTC_OUT, RTC_TS, OSC32OUT
VBAT	F2	P	-	Default: VBAT
VDD	D4	P	-	Default: VDD
PD0	E2	I/O	5VT	Default: PD0

GD32F5HCRIx6 BGA64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: QSPI_IO1, SPI0_MOSI, I2C0_SMBA, USART1_TX, SQPI_D1, SPI1_MOSI, I2S1_SD, TIMER2_CH0, TIMER16_BRKIN, EVENTOUT
PD1	G2	I/O	5VT	Default: PD1 Alternate: QSPI_IO2, SPI0_IO2, I2C0_SDA, I2S1_MCK, USART1_RX, SQPI_D2, SPI1_NSS, I2S1_WS, TIMER2_CH1, TIMER16_CH0, EVENTOUT
PD2	H2	I/O	5VT	Default: PD2 Alternate: IFRP_OUT, QSPI_IO3, SPI0_IO3, I2C0_SCL, RTC_OUT, SQPI_D3, SPI1_SCK, TIMER2_CH2, CTC_SYNC, TIMER16_CH0_ON, EVENTOUT
PC9-OSCIN	G1	I/O	5VT	Default: PC9 Alternate: EVENTOUT Additional: OSCIN
PC10-OSCOUT	H1	I/O	5VT	Default: PC10 Alternate: EVENTOUT Additional: OSCOUT
VDD	E5	P	-	Default: VDD
VSS	E4	P	-	Default: VSS
NRST	F3	I/O	-	Default: NRST
PC11	G3	I/O	5VT	Default: PC11 Alternate: QSPI_SCK, SPI0_SCK, I2S1_CKIN, USART1_CK, SQPI_SCK, SPI1_SCK, EVENTOUT Additional: ADC_IN12
PC12	C2	I/O	5VT	Default: PC12 Alternate: QSPI_CSN, SPI0_NSS, USART1_RTS, SQPI_CSN, SPI1_NSS, I2S1_WS, EVENTOUT Additional: ADC_IN13
PC13	D2	I/O	5VT	Default: PC13 Alternate: QSPI_IO0, SPI0_MISO, I2S1_ADD_SD, USART1_CTS, SQPI_D0, SPI1_MISO, EVENTOUT Additional: ADC_IN14
VSSA /VREFN	H3	P	-	Default: VSSA/VREFN
VDDA/ VREFP/ VEFUSE	H4	P	-	Default: VDDA/VREFP/VEFUSE
PA0	G4	I/O	5VT	Default: PA0 Alternate: USART0_TX, USART1_CTS, EVENTOUT, TIMER1_CH0, TIMER1_ETI, TIMER4_CH0

GD32F5HCRIx6 BGA64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Additional: ADC_IN0
PA1	F4	I/O	5VT	Default: PA1 Alternate: USART0_RX, USART1_RTS, EVENTOUT, TIMER1_CH1, TIMER4_CH1 Additional: ADC_IN1
PA2-WKUP0	H5	I/O	5VT	Default: PA2 Alternate: USART0_CK, TIMER0_CH0, EVENTOUT, TIMER1_CH2, TIMER4_CH2, I2S1_CKIN, USART1_TX Additional: ADC_IN2, WKUP0, RTC_TAMP1
PA3	H6	I/O	5VT	Default: PA3 Alternate: USART1_CK, TIMER0_CH0_ON, EVENTOUT, TIMER1_CH3, TIMER4_CH3, I2S1_MCK, USART1_RX, RTC_OUT Additional: ADC_IN3
PC0	F5	I/O	5VT	Default: PC0 Alternate: USART1_TX, TIMER0_CH3, TIMER4_CH2, I2C0_SMBA, EVENTOUT Additional: ADC_IN4
PC1	G5	I/O	5VT	Default: PC1 Alternate: USART1_RX, TIMER0_BRKIN, I2C1_SMBA, EVENTOUT, SPI1_MOSI, I2S1_SD, TIMER4_CH3 Additional: ADC_IN5
PC2	G6	I/O	5VT	Default: PC2 Alternate: I2C1_SDA, I2C0_SCL, TIMER4_CH0, TIMER0_CH0, TIMER0_ETI, EVENTOUT, SPI1_MISO, I2S1_ADD_SD, USART1_CTS Additional: ADC_IN6
PC3	G7	I/O	5VT	Default: PC3 Alternate: I2S1_SD, I2C1_SCL, I2C0_SDA, TIMER4_CH1, TIMER0_CH0_ON, TIMER1_CH0, TIMER1_ETI, TIMER15_BRKIN, EVENTOUT, SPI1_MOSI, USART1_RTS Additional: ADC_IN7
VSS	D7	P		Default: VSS
PA4	H7	I/O	5VT	Default: PA4 Alternate: I2S1_ADD_SD, SPI1_MOSI, I2S1_SD, SPI0_MOSI, QSPI_SCK, TIMER4_CH2, USART1_TX, TIMER0_CH1, TIMER15_CH0, EVENTOUT, SPI0_NSS, USART1_CK

GD32F5HCRIx6 BGA64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Additional: ADC_IN8
PA5	H8	I/O	5VT	Default: PA5 Alternate: I2S1_MCK, SPI0_MISO, QSPI_CSN, TIMER4_CH3, USART1_RX, TIMER0_CH1_ON, EVENTOUT, SPI0_SCK, TIMER15_CH0_ON
PA6	G8	I/O	5VT	Default: PA6 Alternate: I2S1_CKIN, SPI0_SCK, QSPI_IO0, TIMER2_CH0, USART2_TX, TIMER0_CH1, TIMER1_CH1, TIMER15_BRKIN, EVENTOUT, SPI0_MISO, I2S1_MCK
PA7	F8	I/O	5VT	Default: PA7 Alternate: SPI1_NSS, I2S1_WS, SPI0_NSS, QSPI_IO1, TIMER2_CH1, USART2_RX, TIMER0_CH1_ON, TIMER1_CH2, EVENTOUT, TIMER0_CH0_ON, SPI0_MOSI
PC4	F7	I/O	5VT	Default: PC4 Alternate: I2S1_ADD_SD, SPI0_IO2, QSPI_IO2, TIMER2_CH2, EVENTOUT, SQPI_CLK, CK_OUT1
PC5	F6	I/O	5VT	Default: PC5 Alternate: SPI0_IO3, QSPI_IO3, TIMER2_CH3, TIMER2_CH0, TIMER16_CH0_ON, EVENTOUT, USART2_RX, SQPI_CSN, CK_OUT1
PB0-WKUP6	E6	I/O	5VT	Default: PB0 Alternate: TIMER3_CH0, TIMER2_CH1, EVENTOUT, TIMER0_CH1_ON Additional: WKUP6
PB1	E8	I/O	5VT	Default: PB1 Alternate: TIMER3_CH1, TIMER2_CH2, EVENTOUT, TIMER0_CH2_ON
PB2-WKUP2	E7	I/O	5VT	Default: PB2 Alternate: TIMER3_CH2, TIMER2_CH3, EVENTOUT, TIMER1_CH3 Additional: WKUP2
PB10	D5	I/O	5VT	Default: PB10 Alternate: TIMER3_CH3, TIMER0_CH1, IFRP_OUT, EVENTOUT, TIMER1_CH2, TIMER3_ETI, USART2_TX, USART0_TX
PB11	C6	I/O	5VT	Default: PB11 Alternate: USBFS_ID, TIMER0_CH1_ON, EVENTOUT, I2S1_CKIN, USART2_RX, USART0_RX
PB12	D8	I/O	5VT	Default: PB12

GD32F5HCRIx6 BGA64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: I2S1_WS, USBFS_DP, TIMER0_CH3, EVENTOUT, TIMER0_BRKIN, SPI1_NSS, USART2_CK, USART0_CK
PB13	C8	I/O	5VT	Default: PB13 Alternate: USBFS_DM, EVENTOUT, TIMER15_CH0, TIMER0_CH0_ON, SPI1_SCK, USART2_CTS, USART0_CTS
PB14	B8	I/O	5VT	Default: PB14 Alternate: EVENTOUT, TIMER15_BRKIN, TIMER0_CH1_ON, SPI1_MISO, I2S1_ADD_SD, USART2_RTS, USART0_RTS Additional: USBFS_VBUS
VDD	D6	P		Default: VDD
VSS	C7	P		Default: VSS
PB15	A8	I/O	5VT	Default: PB15 Alternate: I2S1_SD, USART1_TX, USART0_TX, I2C0_SCL, I2C1_SCL, IFRP_OUT, EVENTOUT, RTC_REFIN, TIMER0_CH2_ON, SPI1_MOSI
PA8	C5	I/O	5VT	Default: PA8 Alternate: CK_OUT0, USART1_RX, USART0_RX, I2C0_SDA, I2C1_SDA, EVENTOUT, TIMER15_CH0, TIMER0_CH0, USART0_CK, USBFS_SOF, RTC_OUT, CTC_SYNC
PA9	A7	I/O	5VT	Default: PA9 Alternate: SPI0_MOSI, SQPI_CLK, QSPI_SCK, EVENTOUT, TIMER15_CH0_ON, TIMER0_CH1, SPI1_SCK, USART0_TX
PA10	A6	I/O	5VT	Default: PA10 Alternate: SPI0_MISO, SQPI_CSN, QSPI_CSN, EVENTOUT, TIMER16_CH0, TIMER0_CH2
PA11	B7	I/O	5VT	Default: PA11 Alternate: SPI0_SCK, SQPI_D0, QSPI_IO0, EVENTOUT, TIMER16_BRKIN, TIMER0_CH3
PA12-WKUP3	B6	I/O	5VT	Default: PA12 Alternate: SPI0_NSS, SQPI_D1, QSPI_IO1, EVENTOUT, TIMER16_CH0_ON, TIMER0_ETI, USART0_RTS Additional: WKUP3
PB3	B5	I/O	5VT	Default: JTDO, TRACESWO, PB3

GD32F5HCRIx6 BGA64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: USART2_CTS, SPI0_IO2, SQPI_D2, QSPI_IO2, EVENTOUT, TIMER15_BRKIN, TIMER1_CH1, SPI0_SCK, USART0_RX, SPI1_SCK
PB4	A5	I/O	5VT	Default: NJTRST, PB4 Alternate: USART2_RTS, SPI0_IO3, SQPI_D3, QSPI_IO3, TIMER1_CH0, TIMER1_ETI, EVENTOUT, SPI0_MISO, SPI1_MISO
PC6	A4	I/O	5VT	Default: PC6 Alternate: USART2_TX, TIMER1_CH1, TIMER0_CH1, TIMER0_BRKIN, TRACECK, TIMER16_BRKIN, TIMER2_CH0, I2S1_MCK, SPI0_IO2, SQPI_D0, EVENTOUT
PC7	C4	I/O	5VT	Default: PC7 Alternate: USART2_RX, TIMER1_CH2, TIMER0_CH1_ON, TIMER0_ETI, TIMER16_CH0, TIMER2_CH1, SPI1_SCK, SPI0_IO3, SQPI_D1, EVENTOUT
PB5	D3	I/O	5VT	Default: PB5 Alternate: USART2_CK, TIMER1_CH3, IFRP_OUT, EVENTOUT, SPI0_MOSI, SQPI_SCK, SPI1_MOSI, I2S1_SD
PB6	C3	I/O	5VT	Default: PB6 Alternate: SPI1_MISO, EVENTOUT, TRACED0, SQPI_CSN, SPI1_NSS, I2S1_WS
PD3-WKUP7	B4	I/O	5VT	Default: PD3 Alternate: I2C1_SCL, TIMER15_CH0, USART0_TX, SPI1_MOSI, I2S1_SD, SPI1_MISO, USBFS_ID, TIMER3_CH0, EVENTOUT Additional: WKUP7
PD4-WKUP5	B3	I/O	5VT	Default: PD4 Alternate: I2C1_SDA, TIMER15_CH0_ON, USART0_RX, SPI1_NSS, I2S1_WS, EVENTOUT Additional: WKUP5
PD5-WKUP4	A3	I/O	5VT	Default: PD5 Alternate: I2C1_SMBA, I2C1_SCL, TIMER15_BRKIN, USART0_TX, SPI1_SCK, TIMER3_CH0, EVENTOUT Additional: WKUP4

Note:

(1) Type: I = input, O = output, A = analog, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

2.6.2. GD32F5HCPIQx QFN56 pin definitions

Table 2-4. GD32F5HCPIQx QFN56 pin definitions

GD32F5HCPIQx QFN56				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PB7	1	I/O	5VT	Default: PB7 Alternate: I2S1_WS, SPI1_NSS, EVENTOUT, TRACED1, TIMER3_CH1, I2C0_SDA, USART0_RX
PB8	2	I/O	5VT	Default: PB8 Alternate: SPI1_SCK, EVENTOUT, TRACED2, TIMER3_CH2
PB9	3	I/O	5VT	Default: PB9 Alternate: I2S1_SD, SPI1_MOSI, EVENTOUT, TRACED3, TIMER1_CH1, TIMER3_CH3
PC8-BOOT0	4	I/O	5VT	Default: PC8 Alternate: I2C0_SDA, USART0_TX, I2C1_SDA, EVENTOUT, TIMER2_CH2, USBFS_SOF, TIMER3_ETI Additional: BOOT0
PA15-WKUP1	5	I/O	5VT	Default: JTDI, PA15 Alternate: I2C0_SCL, USART0_RX, I2C1_SCL, EVENTOUT, SPI0_NSS, TIMER3_CH0 Additional: WKUP1
PA13	6	I/O	5VT	Default: JTMS, SWDIO, PA13 Alternate: USART0_CTS, USART1_CTS, I2C0_SMBA, EVENTOUT
PA14-BOOT1	7	I/O	5VT	Default: JTCK, SWCLK, PA14 Alternate: USART0_RTS, USART1_RTS, I2C1_SMBA, EVENTOUT, I2C0_SDA Additional: BOOT1
PC14-OSC32IN	8	I/O	5VT	Default: PC14 Alternate: USART0_CK, USART1_CK, EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	9	I/O	5VT	Default: PC15 Alternate: IFRP_OUT, EVENTOUT Additional: RTC_TAMP0, RTC_OUT, RTC_TS, OSC32OUT
VBAT	10	P	-	Default: VBAT
VDD	11	P	-	Default: VDD
PD0	12	I/O	5VT	Default: PD0 Alternate: QSPI_IO1, SPI0_MOSI, I2C0_SMBA, USART1_TX, SQPI_D1, SPI1_MOSI, I2S1_SD, TIMER2_CH0, TIMER16_BRKIN, EVENTOUT

GD32F5HCPIQx QFN56				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PD1	13	I/O	5VT	Default: PD1 Alternate: QSPI_IO2, SPI0_IO2, I2C0_SDA, I2S1_MCK, USART1_RX, SQPI_D2, SPI1_NSS, I2S1_WS, TIMER2_CH1, TIMER16_CH0, EVENTOUT
PD2	14	I/O	5VT	Default: PD2 Alternate: IFRP_OUT, QSPI_IO3, SPI0_IO3, I2C0_SCL, RTC_OUT, SQPI_D3, SPI1_SCK, TIMER2_CH2, CTC_SYNC, TIMER16_CH0_ON, EVENTOUT
NC	15	-	-	-
NRST	16	I/O	-	Default: NRST
PC11	17	I/O	5VT	Default: PC11 Alternate: QSPI_SCK, SPI0_SCK, I2S1_CKIN, USART1_CK, SQPI_SCK, SPI1_SCK, EVENTOUT Additional: ADC_IN12
PC12	18	I/O	5VT	Default: PC12 Alternate: QSPI_CSN, SPI0_NSS, USART1_RTS, SQPI_CSN, SPI1_NSS, I2S1_WS, EVENTOUT Additional: ADC_IN13
PC9-OSCIN	19	I/O	5VT	Default: PC9 Alternate: EVENTOUT Additional: OSCIN
PC10-OSCOUT	20	I/O	5VT	Default: PC10 Alternate: EVENTOUT Additional: OSCOUT
VDDA /VREFP/ VEFUSE	21	P	-	Default: VDDA/VREFP/VEFUSE
PA0	22	I/O	5VT	Default: PA0 Alternate: USART0_TX, USART1_CTS, EVENTOUT, TIMER1_CH0, TIMER1_ETI, TIMER4_CH0 Additional: ADC_IN0
PA1	23	I/O	5VT	Default: PA1 Alternate: USART0_RX, USART1_RTS, EVENTOUT, TIMER1_CH1, TIMER4_CH1 Additional: ADC_IN1
PA2-WKUP0	24	I/O	5VT	Default: PA2 Alternate: USART0_CK, TIMER0_CH0, EVENTOUT, TIMER1_CH2, TIMER4_CH2, I2S1_CKIN, USART1_TX Additional: ADC_IN2, WKUP0, RTC_TAMP1

GD32F5HCPIQx QFN56				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PA3	25	I/O	5VT	Default: PA3 Alternate: USART1_CK, TIMER0_CH0_ON, EVENTOUT, TIMER1_CH3, TIMER4_CH3, I2S1_MCK, USART1_RX, RTC_OUT Additional: ADC_IN3
PC0	26	I/O	5VT	Default: PC0 Alternate: USART1_TX, TIMER0_CH3, TIMER4_CH2, I2C0_SMBA, EVENTOUT Additional: ADC_IN4
PC1	27	I/O	5VT	Default: PC1 Alternate: USART1_RX, TIMER0_BRKIN, I2C1_SMBA, EVENTOUT, SPI1_MOSI, I2S1_SD, TIMER4_CH3 Additional: ADC_IN5
PC2	28	I/O	5VT	Default: PC2 Alternate: I2C1_SDA, I2C0_SCL, TIMER4_CH0, TIMER0_CH0, TIMER0_ETI, EVENTOUT, SPI1_MISO, I2S1_ADD_SD, USART1_CTS Additional: ADC_IN6
PC3	29	I/O	5VT	Default: PC3 Alternate: I2S1_SD, I2C1_SCL, I2C0_SDA, TIMER4_CH1, TIMER0_CH0_ON, TIMER1_CH0, TIMER1_ETI, TIMER15_BRKIN, EVENTOUT, SPI1_MOSI, USART1_RTS Additional: ADC_IN7
PA4	30	I/O	5VT	Default: PA4 Alternate: I2S1_ADD_SD, SPI1_MOSI, I2S1_SD, SPI0_MOSI, QSPI_SCK, TIMER4_CH2, USART1_TX, TIMER0_CH1, TIMER15_CH0, EVENTOUT, SPI0_NSS, USART1_CK Additional: ADC_IN8
PA5	31	I/O	5VT	Default: PA5 Alternate: I2S1_MCK, SPI0_MISO, QSPI_CSN, TIMER4_CH3, USART1_RX, TIMER0_CH1_ON, EVENTOUT, SPI0_SCK, TIMER15_CH0_ON
PA6	32	I/O	5VT	Default: PA6 Alternate: I2S1_CKIN, SPI0_SCK, QSPI_IO0, TIMER2_CH0, USART2_TX, TIMER0_CH1, TIMER1_CH1, TIMER15_BRKIN, EVENTOUT, SPI0_MISO, I2S1_MCK
PA7	33	I/O	5VT	Default: PA7 Alternate: SPI1_NSS, I2S1_WS, SPI0_NSS,

GD32F5HCPIQx QFN56				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				QSPI_IO1, TIMER2_CH1, USART2_RX, TIMER0_CH1_ON, TIMER1_CH2, EVENTOUT, TIMER0_CH0_ON, SPI0_MOSI
PC4	34	I/O	5VT	Default: PC4 Alternate: I2S1_ADD_SD, SPI0_IO2, QSPI_IO2, TIMER2_CH2, EVENTOUT, SQPI_CLK, CK_OUT1
PC5	35	I/O	5VT	Default: PC5 Alternate: SPI0_IO3, QSPI_IO3, TIMER2_CH3, TIMER2_CH0, TIMER16_CH0_ON, EVENTOUT, USART2_RX, SQPI_CSN, CK_OUT1
PB0-WKUP6	36	I/O	5VT	Default: PB0 Alternate: TIMER3_CH0, TIMER2_CH1, EVENTOUT, TIMER0_CH1_ON Additional: WKUP6
PB1	37	I/O	5VT	Default: PB1 Alternate: TIMER3_CH1, TIMER2_CH2, EVENTOUT, TIMER0_CH2_ON
PB2-WKUP2	38	I/O	5VT	Default: PB2 Alternate: TIMER3_CH2, TIMER2_CH3, EVENTOUT, TIMER1_CH3 Additional: WKUP2
PB10	39	I/O	5VT	Default: PB10 Alternate: TIMER3_CH3, TIMER0_CH1, IFRP_OUT, EVENTOUT, TIMER1_CH2, TIMER3_ETI, USART2_TX, USART0_TX
PB11	40	I/O	5VT	Default: PB11 Alternate: USBFS_ID, TIMER0_CH1_ON, EVENTOUT, I2S1_CKIN, USART2_RX, USART0_RX
PB12	41	I/O	5VT	Default: PB12 Alternate: I2S1_WS, USBFS_DP, TIMER0_CH3, EVENTOUT, TIMER0_BRKIN, SPI1_NSS, USART2_CK, USART0_CK
PB13	42	I/O	5VT	Default: PB13 Alternate: USBFS_DM, EVENTOUT, TIMER15_CH0, TIMER0_CH0_ON, SPI1_SCK, USART2_CTS, USART0_CTS
PB14	43	I/O	5VT	Default: PB14 Alternate: EVENTOUT, TIMER15_BRKIN, TIMER0_CH1_ON, SPI1_MISO, I2S1_ADD_SD, USART2_RTS, USART0_RTS Additional: USBFS_VBUS

GD32F5HCPIQx QFN56				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
VDD	44	P		Default: VDD
PB15	45	I/O	5VT	Default: PB15 Alternate: I2S1_SD, USART1_TX, USART0_TX, I2C0_SCL, I2C1_SCL, IFRP_OUT, EVENTOUT, RTC_REFIN, TIMER0_CH2_ON, SPI1_MOSI
PA8	46	I/O	5VT	Default: PA8 Alternate: CK_OUT0, USART1_RX, USART0_RX, I2C0_SDA, I2C1_SDA, EVENTOUT, TIMER15_CH0, TIMER0_CH0, USART0_CK, USBFS_SOF, RTC_OUT, CTC_SYNC
PA9	47	I/O	5VT	Default: PA9 Alternate: SPI0_MOSI, SQPI_CLK, QSPI_SCK, EVENTOUT, TIMER15_CH0_ON, TIMER0_CH1, SPI1_SCK, USART0_TX
PA10	48	I/O	5VT	Default: PA10 Alternate: SPI0_MISO, SQPI_CSN, QSPI_CSN, EVENTOUT, TIMER16_CH0, TIMER0_CH2
PA11	49	I/O	5VT	Default: PA11 Alternate: SPI0_SCK, SQPI_D0, QSPI_IO0, EVENTOUT, TIMER16_BRKIN, TIMER0_CH3
PA12-WKUP3	50	I/O	5VT	Default: PA12 Alternate: SPI0_NSS, SQPI_D1, QSPI_IO1, EVENTOUT, TIMER16_CH0_ON, TIMER0_ETI, USART0_RTS Additional: WKUP3
PB3	51	I/O	5VT	Default: JTDO, TRACESWO, PB3 Alternate: USART2_CTS, SPI0_IO2, SQPI_D2, QSPI_IO2, EVENTOUT, TIMER15_BRKIN, TIMER1_CH1, SPI0_SCK, USART0_RX, SPI1_SCK
PB4	52	I/O	5VT	Default: NJTRST, PB4 Alternate: USART2_RTS, SPI0_IO3, SQPI_D3, QSPI_IO3, TIMER1_CH0, TIMER1_ETI, EVENTOUT, SPI0_MISO, SPI1_MISO
PC6	53	I/O	5VT	Default: PC6 Alternate: USART2_TX, TIMER1_CH1, TIMER0_CH1, TIMER0_BRKIN, TRACECK, TIMER16_BRKIN, TIMER2_CH0, I2S1_MCK, SPI0_IO2, SQPI_D0, EVENTOUT
PC7	54	I/O	5VT	Default: PC7 Alternate: USART2_RX, TIMER1_CH2, TIMER0_CH1_ON, TIMER0_ETI, TIMER16_CH0,

GD32F5HCPIQx QFN56				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				TIMER2_CH1, SPI1_SCK, SPI0_IO3, SQPI_D1, EVENTOUT
PB5	55	I/O	5VT	Default: PB5 Alternate: USART2_CK, TIMER1_CH3, IFRP_OUT, EVENTOUT, SPI0_MOSI, SQPI_SCK, SPI1_MOSI, I2S1_SD
PB6	56	I/O	5VT	Default: PB6 Alternate: SPI1_MISO, EVENTOUT, TRACED0, SQPI_CSN, SPI1_NSS, I2S1_WS

Note:

(1) Type: I = input, O = output, A = analog, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

2.6.3. GD32F5HCxx pin alternate functions

Table 2-5. Port A alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0	USART0_TX	TIMER1_CH0/TIMER1_ETI	TIMER4_CH0					USART1_CTS								EVENTOUT
PA1	USART0_RX	TIMER1_CH1	TIMER4_CH1					USART1_RTS								EVENTOUT
PA2	USART0_CK	TIMER1_CH2	TIMER4_CH2			I2S1_CKIN	TIMER0_CH0	USART1_TX								EVENTOUT
PA3	USART1_CK	TIMER1_CH3	TIMER4_CH3			I2S1_MCK		USART1_RX	TIMER0_CH0_ON	RTC_OUT						EVENTOUT
PA4	USART1_TX	I2S1_ADD_SD	SPI0_MOSI	QSPI_SCK	TIMER4_CH2	SPI0_NSS	SPI1_MOSI/I2S1_SD	USART1_CK	TIMER0_CH1				TIMER15_CH0			EVENTOUT
PA5	USART1_RX		I2S1_MCK	QSPI_CSN	SPI0_MISO	SPI0_SCK		TIMER4_CH3	TIMER0_CH1_ON				TIMER15_CH0_ON			EVENTOUT
PA6			TIMER2_CH0	QSPI_IO0	I2S1_CKIN	SPI0_MISO	I2S1_MCK	SPI0_SCK	TIMER0_CH1	TIMER1_CH1	USART2_TX		TIMER15_BRKIN			EVENTOUT
PA7	SPI1_NSS/I2S1_WS	TIMER0_CH0_ON	TIMER2_CH1	QSPI_IO1	SPI0_NSS	SPI0_MOSI	TIMER0_CH1_ON		USART2_RX	TIMER1_CH2						EVENTOUT
PA8	CK_OUT0	TIMER0_CH0	USART0_RX	USART1_RX		I2C0_SDA	I2C1_SDA	USART0_CK	TIMER15_CH0	RTC_OUT	USBFS_SOF	CTC_SYNC				EVENTOUT
PA9	SPI0_MOSI	TIMER0_CH1		SQPI_CLK	QSPI_SCK	SPI1_SCK		USART0_TX	TIMER15_CH0_ON							EVENTOUT
PA10	SPI0_MISO	TIMER0_CH2		SQPI_CSN	QSPI_CSN			TIMER16_CH0								EVENTOUT
PA11	SPI0_SCK	TIMER0_CH3		SQPI_D0	QSPI_IO0			TIMER16_BRKIN								EVENTOUT
PA12		TIMER0_ETI			QSPI_IO1		SPI0_NSS	USART0_RTS	SQPI_D1		TIMER16_CH0_ON					EVENTOUT
PA13	JTMS/SWDIO				I2C0_SMBA			USART0_CTS	USART1_CTS							EVENTOUT
PA14	JTCK/SWCLK				I2C1_SMBA			USART0_RTS	USART1_RTS				I2C0_SDA			EVENTOUT
PA15	JTDI				I2C0_SCL	SPI0_NSS	I2C1_SCL	USART0_RX					TIMER3_CH0			EVENTOUT

Table 2-6. Port B alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB0		TIMER0_CH1_ON	TIMER2_CH1	TIMER3_CH0												EVENTOUT

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB1		TIMER0_CH2_ON	TIMER3_CH1	TIMER2_CH2												EVENTOUT
PB2		TIMER1_CH3	TIMER3_CH2	TIMER2_CH3												EVENTOUT
PB3	JTDO/TRACESWO	TIMER1_CH1		QSPI_IO2		SPI0_SCK	SPI0_IO2	USART0_RX	SQPI_D2		USART2_CTS	TIMER15_BRKIN		SPI1_SCK		EVENTOUT
PB4	NJTRST	TIMER1_CH0/TIMER1_ETI		QSPI_IO3		SPI0_MISO	SPI0_IO3	USART2_RTS	SQPI_D3					SPI1_MISO		EVENTOUT
PB5	IFRP_OUT	TIMER1_CH3				SPI0_MOSI		USART2_CK					SQPI_SCK	SPI1_MOSI/I2S1_SD		EVENTOUT
PB6	TRACED0					SPI1_MISO							SQPI_CSN	SPI1_NSS/I2S1_WS		EVENTOUT
PB7	TRACED1		TIMER3_CH1		I2C0_SDA	SPI1_NSS/I2S1_WS		USART0_RX								EVENTOUT
PB8	TRACED2		TIMER3_CH2			SPI1_SCK										EVENTOUT
PB9	TRACED3	TIMER1_CH1	TIMER3_CH3			SPI1_MOSI/I2S1_SD										EVENTOUT
PB10		TIMER1_CH2	TIMER3_ETI	TIMER3_CH3				USART2_TX	TIMER0_CH1	IFRP_OUT			USART0_TX			EVENTOUT
PB11			TIMER0_CH1_ON			I2S1_CKIN		USART2_RX			USBFS_ID		USART0_RX			EVENTOUT
PB12		TIMER0_BRKIN	TIMER0_CH3			SPI1_NSS/I2S1_WS		USART2_CK			USBFS_DP		USART0_CK			EVENTOUT
PB13		TIMER0_CH0_ON				SPI1_SCK		USART2_CTS	TIMER15_CH0		USBFS_DM		USART0_CTS			EVENTOUT
PB14		TIMER0_CH1_ON				SPI1_MISO	I2S1_ADD_SD	USART2_RTS	TIMER15_BRKIN				USART0_RTS			EVENTOUT
PB15	RTC_REFIN	TIMER0_CH2_ON			I2C0_SCL	SPI1_MOSI/I2S1_SD	I2C1_SCL	USART1_TX	USART0_TX	IFRP_OUT						EVENTOUT

Table 2-7. Port C alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC0	USART1_TX		TIMER0_CH3		I2C0_SMBA								TIMER4_CH2			EVENTOUT
PC1	USART1_RX	TIMER0_BRKIN			I2C1_SMBA			SPI1_MOSI/I2S1_SD					TIMER4_CH3			EVENTOUT
PC2	TIMER0_ETI	TIMER0_CH0	TIMER4_CH0		I2C0_SCL	SPI1_MISO	I2S1_ADD_SD			I2C1_SDA				USART1_CTS		EVENTOUT
PC3		TIMER1_CH0/TIMER1_ETI	TIMER4_CH1		I2C0_SDA	SPI1_MOSI/I2S1_SD	I2C1_SCL		TIMER0_CH0_ON				TIMER15_BRKIN	USART1_RTS		EVENTOUT
PC4	CK_OUT1	I2S1_ADD_SD	TIMER2_CH2	QSPI_IO2			SPI0_IO2		SQPI_CLK							EVENTOUT
PC5	CK_OUT1	TIMER2_CH0	TIMER2_CH3	QSPI_IO3			SPI0_IO3	USART2_RX	SQPI_CSN				TIMER16_CH0_ON			EVENTOUT
PC6	TRACECK	TIMER0_BRKIN	TIMER2_CH0			I2S1_MCK		TIMER16_BRKIN	TIMER0_CH1	TIMER1_CH1	USART2_TX		SPI0_IO2	SQPI_D0		EVENTOUT
PC7	TIMER0_ETI		TIMER2_CH1	TIMER0_CH1_ON		SPI1_SCK		TIMER16_CH0	USART2_RX	TIMER1_CH2			SPI0_IO3	SQPI_D1		EVENTOUT
PC8			TIMER2_CH2			I2C0_SDA	I2C1_SDA	USART0_TX			USBFS_SOF		TIMER3_ETI			EVENTOUT
PC9																EVENTOUT
PC10																EVENTOUT
PC11				QSPI_SCK	SPI0_SCK		I2S1_CKIN	USART1_CK	SQPI_SCK	SPI1_SCK						EVENTOUT
PC12				QSPI_CSN	SPI0_NSS			USART1_RTS	SQPI_CSN	SPI1_NSS/I2S1_WS						EVENTOUT
PC13				QSPI_IO0	SPI0_MISO		I2S1_ADD_SD	USART1_CTS	SQPI_D0	SPI1_MISO						EVENTOUT
PC14	USART0_CK	USART1_CK														EVENTOUT
PC15	IFRP_OUT															EVENTOUT

Table 2-8. Port D alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PD0				QSPI_IO1	SPI0_MOSI	I2C0_SMBA		USART1_TX	SQPI_D1	SPI1_MOSI/I2S1_SD	TIMER2_CH0		TIMER16_BRKIN			EVENTOUT

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PD1				QSPI_IO2	SPI0_IO2	I2C0_SDA	I2S1_MCK	USART1_RX	SQPI_D2	SPI1_NSS/I2S1_WS	TIMER2_CH1		TIMER16_CH0			EVENTOUT
PD2	IFRP_OUT			QSPI_IO3	SPI0_IO3	I2C0_SCL	RTC_OUT		SQPI_D3	SPI1_SCK	TIMER2_CH2	CTC_SYNC	TIMER16_CH0_ON			EVENTOUT
PD3				I2C1_SCL		TIMER15_CH0		USART0_TX	SPI1_MOSI/I2S1_SD	SPI1_MISO	USBFS_ID		TIMER3_CH0			EVENTOUT
PD4				I2C1_SDA		TIMER15_CH0_ON		USART0_RX		SPI1_NSS/I2S1_WS						EVENTOUT
PD5				I2C1_SMBA	I2C1_SCL	TIMER15_BRKIN		USART0_TX		SPI1_SCK			TIMER3_CH0			EVENTOUT

3. Functional description

3.1. Arm® Cortex®-M33 core

The Cortex®-M33 processor is a 32-bit processor that possesses low interrupt latency and low-cost debug. The characteristics of integrated and advanced make the Cortex®-M33 processor suitable for market products that require microcontrollers with high performance and low power consumption.

32-bit Arm® Cortex®-M33 processor core:

- Up to 200 MHz operation frequency
- Ultra-low power, energy-efficient operation
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M33 processor is based on the ARMv8 architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M33:

- Internal Bus Matrix connected with Code bus, System bus, and Private Peripheral Bus (PPB) and debug accesses
- Nested Vectored Interrupt Controller (NVIC)
- Breakpoint Unit (BPU)
- Data Watchpoint and Trace (DWT)
- Instrumentation Trace Macrocell (ITM)
- Serial Wire JTAG Debug Port (SWJ-DP)
- Trace Port Interface Unit (TPIU)
- Arm® TrustZone® technology, using the ARMv8-M main extension supporting secure and non-secure states
- Memory Protection Unit (MPU), supporting 8 regions for secure and 8 regions for non-secure.
- Configurable secure attribute unit (SAU) supporting up to 8 memory regions
- Floating Point Unit (FPU)
- DSP Extension (DSP)

3.2. On-chip memory

- Up to 2048 Kbytes of SIP Flash memory
- Up to 320 Kbytes of SRAM

2048 Kbytes of Main Flash, and 320 Kbytes of inner SRAM at most is available for storing programs and data. ***Table 2-2. GD32F5HCxx memory map*** shows the memory map of the GD32F5HCxx series of devices, including code, SRAM, peripheral, and other pre-

defined regions.

3.3. Clock, reset and supply management

- Internal 16 MHz and 48 MHz factory-trimmed RC and external 19.2 to 52 MHz crystal oscillator
- Internal 32 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator
- Integrated system clock PLL
- 2.7 to 3.63 V application supply and I/Os
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD)

The Clock Control Unit (CCTL) provides a range of oscillator and clock functions, including high-speed internal RC oscillators, external crystal oscillators, and two types of oscillators: high-speed and low-speed. Several prescalers allow the frequency configuration of the AHB and two APB domains. The maximum operating frequencies for the AHB, APB2, and APB1 domains are 200 MHz, 100 MHz, and 50 MHz, respectively. See ***Figure 2-4. GD32F5HCxx clock tree*** for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: System reset (resets the processor core and peripheral IP components); Power-on reset (POR) and power-down reset (PDR), are always active, and ensures the proper operation of the chip. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold, and generates an interrupt as a warning message to lead the MCU into a secure state.

Power supply schemes:

- V_{DD} range: 2.7 to 3.63 V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}: 0 V.
- V_{DDA} range: 2.7 to 3.63 V, external analog power supplies for ADC, reset blocks, RCs and PLL.
- V_{BAT} range: 1.62 to 3.63 V, power supply for RTC unit, LXTAL oscillator, BPOR, and two pads, including PC14 to PC15 when V_{DD} is not present.
- V_{DD} <= V_{DDA}.

3.4. Boot modes

At startup, a BOOT0 pin, and a BOOT1 pin are used to select the boot memory address.

The BOOT0 value may come from the BOOT0 pin or from the value of SWBOOT0 bit in the EFUSE_CTL register to free the GPIO pad if needed.

The BOOT1 value may come from the PA14 pin or from the value of SWBOOT1 bit in the EFUSE_CTL register to free the GPIO pad if needed.

Table 3-1. BOOT0 modes

EFUSE_CTL		FMC_OBR1		BOOT0 PC8 pin	BOOT0
SWBOOT0	EFBOOT0	SWBOOT0	nBOOT0		
0	-	1	-	0	0
0	-	1	-	1	1
0	-	0	1	-	0
0	-	0	0	-	1
1	0	-	-	-	0
1	1	-	-	-	1

Table 3-2. BOOT1 modes

EFUSE_CTL		FMC_OBR1		BOOT1 PA14 pin	BOOT1
SWBOOT1	EFBOOT1	SWBOOT1	nBOOT1		
0	-	1	-	0	0
0	-	1	-	1	1
0	-	0	1	-	0
0	-	0	0	-	1
1	0	-	-	-	0
1	1	-	-	-	1

Refer to ***Table 3-3. Boot address modes when TrustZone is disabled (TZEN=0)*** and ***Table 3-4. Boot modes when TrustZone is enabled (TZEN=1)*** for boot address when TrustZone is disabled and enabled respectively. When the EFBOOTLK bit in the EFUSE_CTL register is set, the boot memory address is selected based on boot1 and boot0.

Table 3-3. Boot address modes when TrustZone is disabled (TZEN=0)

EFBOOTLK	BOOT0	BOOT1	Boot address	Boot area
0	0	-	0x08000000	SIP Flash
0	1	0	0x0BF40000	Bootloader / ROM
0	1	1	0x0A000000	SRAM0
1	0	-	0x08000000	SIP Flash
1	1	-	0x0BF40000	Bootloader / ROM

When TrustZone is enabled by setting the TZEN option bit, the boot space must be in secure area.

Table 3-4. Boot modes when TrustZone is enabled (TZEN=1)

GSSACMD == 8'hc(1)	EFBOOTLK	BOOT0	BOOT1	EFSB	Boot address	Boot area
0	0	0	-	0	0x0C000000	SPI Flash
0	0	0	-	1	0X0FF84000	secure boot
0	0	1	0	-	0x0FF80000	GSSA
0	0	1	1	-	0x0E000000	SRAM0
-	1	0	-	0	0x0C000000	SPI Flash

GSSACMD == 8'hc(1)	EFBOOTLK	BOOT0	BOOT1	EFSB	Boot address	Boot area
-	1	0	-	1	0X0FF84000	secure boot
-	1	1	-	-	0x0FF80000	GSSA
1	0	-	-	-	0x0FF80000	GSSA

Note: (1) When the GSSACMD bit field is 0x0C, it means 1, otherwise it means 0.

The BOOTx (x=0/1) value (either coming from the pin or the EFBOOTx bit) is latched upon reset release. It is up to the user to set BOOTx values to select the required boot mode. The BOOTx pin or EFBOOTx bit (depending on the EFBOOTLK and SWBOOTx bit value in the EFUSE_CTL register) is also re-sampled when exiting from Standby mode. Consequently, they must be kept in the required Boot mode configuration in Standby mode. After startup delay, the selection of the boot area is done before releasing the processor reset.

The embedded boot loader is located in the System memory, which is used to reprogram the Flash memory. The boot loader can be activated through one of the following serial interfaces: USART0 (PA8, PB15), USART1 (PA2, PA3), USART2 (PB10, PB11) and USBFS (PB12, PB13).

To ensure system reliability and stability, it is recommended not to connect peripherals that may generate interference signals (such as sensor outputs, watchdog chips, buttons, etc.) to the above-mentioned pins during the hardware design stage, in order to avoid affecting the normal function of the Bootloader and causing abnormal outputs to the connected peripherals.

Note: After the MCU starts from the system memory, the USART interface and the USB interface are in the detection state. Therefore, the unused USART RX pins (PA8, PA3, PB11) need to be maintained at a stable logic level. Unused USB DP pin (PB12) is prohibited from being pulled down and recommended to pull up. This design is made to prevent false triggering during the connection process.

3.5. Power saving modes

The MCU supports four kinds of power saving modes to achieve even lower power consumption. They are Sleep, Deep-sleep, Standby and SRAM_sleep. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep mode**

  In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt/event can wake up the system.

- **Deep-sleep mode**

The Deep-sleep mode is based on the SLEEPDEEP mode of the Cortex®-M33. In Deep-sleep mode, all clocks in the V_{CORE} domain are off, and all of IRC16M, IRC48M, HXTAL and PLLs are disabled. The contents of SRAM0 and registers are preserved. The LDO can operate normally or in low power mode depending on the LDOLP bit in the PMU_CTL0 register. Before entering the Deep-sleep mode, it is necessary to set the SLEEPDEEP bit in the Cortex®-M33 System Control Register, and clear the STBMOD bit in the PMU_CTL0 register. Then, the device enters the Deep-sleep mode after a WFI or WFE instruction is executed. If the Deep-sleep mode is entered by executing a WFI instruction, any interrupt from EXTI lines can wake up the system. If it is entered by executing a WFE instruction, any wakeup event from EXTI lines can wake up the system (If SEVONPEND is 1, any interrupt from EXTI lines can wake up the system, refer to Cortex®-M33 Technical Reference Manual). When exiting the Deep-sleep mode, the IRC16M is selected as the system clock. Notice that an additional wakeup delay will be incurred if the LDO operates in low power mode.

The low-driver mode in Deep-sleep mode can be entered by configuring the LDEN, LDNP, LDLP, LDOLP bits in the PMU_CTL0 register. The low-driver mode provides lower drive capability, and the low-power mode take lower power.

- **Standby mode**

The Standby mode is based on the SLEEPDEEP mode of the Cortex®-M33, as well. In Standby mode, the whole V_{CORE} domain is powered off, the LDO is shut down, and all of IRC16M, IRC48M, HXTAL and PLLs are disabled. Before entering the Standby mode, it is necessary to set the SLEEPDEEP bit in the Cortex®-M33 System Control Register, and set the STBMOD bit in the PMU_CTL0 register, and clear WUF bit in the PMU_CS0 register. Then, the device enters the Standby mode after a WFI or WFE instruction is executed, and the STBF status flag in the PMU_CS0 register indicates that the MCU has been in Standby mode. There are four wakeup sources for the Standby mode, including the external reset from NRST pin, the RTC alarm / time stamp / tamper / auto wakeup events, the FWDGT reset, and the rising edge on WKUP pins. The Standby mode achieves the lowest power consumption, but requires the longest time to wake up. Besides, the contents of SRAM0 / SRAM1 / SRAM2 / SRAM3 and registers in 1.2V power domain are lost in Standby mode. When exiting from the Standby mode, a power-on reset occurs and the Cortex®-M33 will execute instruction code from the 0x00000000 address.

- **SRAM_sleep mode**

If at least one of SRAM1 / SRAM2 / SRAM3 is powered off, the SRAM enters SRAM_sleep mode. When the SRAMxPSLEEP (x = 1/2/3) bit in PMU_CTL1 register is set, the SRAMx (x = 1/2/3) will be powered off, the contents of SRAMx (x = 1/2/3) are lost. When the SRAMxPWAKE (x = 1/2/3) bit in PMU_CTL1 register is set, the SRAMx (x = 1/2/3) will be powered on.

SRAM1 / SRAM2 / SRAM3 can be configured powered on or powered off when in run / sleep / deep_sleep mode.

SRAM1 / SRAM2 / SRAM3 are powered off when in standby mode / BKP_ONLY mode.

3.6. Electronic fuse (EFUSE)

- One-time programmable nonvolatile EFUSE storage cells organized as 256*8 bit.
- All bits in the EFUSE cannot be rollback from 1 to 0.
- Can only be accessed through corresponding registers.

The EFUSE controller has an efuse macro that store system parameters. As a non-volatile unit of storage, the bit of efuse macro cannot be restored to 0 once it is programmed to 1. According to the software operation, the EFUSE controller can program all the bits in the system parameters.

3.7. Instruction cache (ICACHE)

- Support 32KB cache with 2 ways, 1024 cache lines per way and 16B per cache line.
- Support fetch address without any wait state if cache hit.
- Support two performance counters: 32-bit hit monitor counter and16-bit miss monitor counter.
- Support TrustZone security and configure registers to be protected at system level.

The instruction cache (ICACHE) is based on CBUS code bus of Cortex-M33 processor. It is necessary to improve performance in fetching instruction and data from both internal and external memories.

3.8. Clock trim controller (CTC)

- Two external reference signal sources: GPIO(CTC_SYNC) and LXTAL clock.
- Provide software reference sync pulse.
- Automatically trimmed by hardware without any software action.
- 16 bits trim counter with reference signal source capture and reload.
- 8 bits clock trim base value to frequency evaluation and automatically trim.
- Enough flag or interrupt to indicate the clock is OK (CKOKIF), warning (CKWARNIF) or error (ERRIF).

The Clock Trim Controller (CTC) is used to trim the internal 48MHz RC oscillator (IRC48M) automatically by hardware. The CTC unit trim the frequency of the IRC48M based on an external accurate reference signal source. It can automatically adjust the trim value to provide a precise IRC48M clock.

3.9. General-purpose inputs / outputs (GPIOs)

- Up to 54 fast GPIOs, all mappable on 16 external interrupt lines
- Analog input/output configurable
- Alternate function input/output configurable

There are up to 54 general purpose I/O pins (GPIO) in GD32F5HCxx, named PA0 ~ PA15, PB0 ~ PB15, PC0 ~ PC15, and PD0 ~ PD5 to implement logic input/output functions. Each GPIO port has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt/Event Controller Unit (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins.

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), input, peripheral alternate function or analog mode. Most of the GPIO pins are shared with digital or analog alternate functions.

3.10. TrustZone protection controller union (TZPCU)

- TZSPC, TZBMPC and TZIAC have independent 32-bit AHB interface.
- For TZSPC, whether non-secure/non-privilege access is supported is defined by secure/privilege configuration registers.
- For TZBMPC and TZIAC, only secure access is supported.
- For securable slave/master peripherals, secure/privilege state is defined in TZSPC registers.
- For off-chip memories, the size of non-secure area is defined in TZSPC registers.
- For on-chip RAM, the secure states of all blocks is defined in TZBMPC registers.

This section describes the TrustZone® protection controller union. Three different sub-blocks, TrustZone® security privilege controller (TZSPC), TrustZone® block-based memory protection controller (TZBMPC) and TrustZone® illegal access controller (TZIAC), are used to configure system security or privilege in a product with programmable-security and privileged attributes. TZSPC is used to define the secure/privilege state for securable slave/master peripherals. TrustZone® mark memory protection controller (TZMMPC) does the security checking of off-chip memories based on the size of non-secure area which is defined in TZSPC. For the on-chip RAM, the security checking is done based on block level which is configured by the TZBMPC through an AHB interface. TZIAC is used to enable all illegal access events for slave/master peripherals in system. If an interrupt is enabled, a dedicated interrupt signal is asserted and generates a secure interrupt towards NVIC whenever a security violation is detected. The interrupt is cleared by writing 1 to the appropriate register of TZIAC.

3.11. CRC calculation unit (CRC)

- 32-bit data input and 32-bit data output. Calculation period is 4 AHB clock cycles for 32-bit input data size from data entered to the calculation result available.
- Free 8-bit register is unrelated to calculation and can be used for any other goals by any other peripheral devices.
- Fixed polynomial: 0x4C11DB7
  $X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^{8}+X^{7}+X^{5}+X^{4}+X^{2}+X+1$

A cyclic redundancy check (CRC) is an error-detecting code commonly used in digital networks and storage devices to detect accidental changes to raw data. This CRC calculation unit can be used to calculate 32 bit CRC code with fixed polynomial.

3.12. True Random number generator (TRNG)

- About 40 periods of TRNG_CLK are needed between two consecutive random numbers
- 32-bit random value seed is generated from analog noise, so the random number is a true random number.

The true random number generator (TRNG) module can generate a 32-bit random value by using continuous analog noise.

3.13. Direct memory access controller (DMA)

- 8 channels for DMA0 controller and 8 channels for DMA1 controller.
- Peripherals supported: Timers, ADC, SPIs, I2S, QSPI, I2Cs, USARTs, CAU, HAU.

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby increasing system performance by off-loading the MCU from copying large amounts of data and avoiding frequent interrupts to serve peripherals needing more data or having available data. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory.

Each channel is connected to fixed hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

3.14. Analog to digital converter (ADC)

- 12-bit SAR ADC's conversion rate is up to 2.5 MSPS
- Hardware oversampling ratio adjustable from 2x to 256x improves resolution to 16-

bit

- Input voltage range: 0 to V_{DDA}
- Temperature sensor

A 12-bit 2.5 MSPS multi-channel ADC is integrated in the device. It has a total of 15 multiplexed channels: up to 12 external channels, 1 channel for internal temperature sensor (V_{SENSE}), 1 channel for internal reference voltage (V_{REFINT}) and one channel for external battery power supply (V_{BAT}) channel. The input voltage range is between 0 and V_{DDA}. An on-chip hardware oversampling scheme improves performance while off-loading the related computational burden from the CPU. The analog watchdog allows the application to detect whether the input voltage goes outside the user-defined higher or lower thresholds. A configurable channel management block can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced use.

The ADC can be triggered from the events generated by the general level 0 timers (TIMERx, x=1, 2, 3, 4) and the advanced timers (TIMER0) with internal connection. The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally connected to the ADC_IN9 input channel which is used to convert the sensor output voltage in a digital value.

To ensure a high accuracy on ADC, the independent power supply V_{DDA} is implemented to achieve better performance of analog circuits. V_{DDA} can be externally connected to V_{DD} through the external filtering circuit that avoids noise on V_{DDA}, and V_{SSA} should be connected to V_{SS} through the specific circuit independently.

3.15. Real time clock (RTC)

- Independent binary-coded decimal (BCD) format timer / counter with twenty 32-bit backup registers.
- Calendar with sub-second, second, minute, hour, week day, day, month and year automatically correction.
- Alarm function with wake up from deep-sleep and standby mode capability.
- On-the-fly correction for synchronization with master clock. Digital calibration with 0.95 ppm resolution for compensation of quartz crystal inaccuracy.

The real time clock is an independent timer which provides a set of continuously running counters in backup registers to provide a real calendar function, and provides an alarm interrupt or an expected interrupt. It is not reset by a system or power reset, or when the device wakes up from standby mode. In the RTC unit, there are two prescalers used for implementing the calendar and other functions. One prescaler is a 7-bit asynchronous prescaler and the other is a 15-bit synchronous prescaler.

3.16. Timers and PWM generation (TIMER)

- One 16-bit advanced timer (TIMER0), two 32-bit general timer (TIMER1, TIMER2), up to four 16-bit general timers (TIMER3, TIMER4, TIMER15, TIMER16), and one 16-bit basic timer (TIMER5)
- Up to 4 independent channels of PWM, output compare or input capture for each general timer and external trigger input
- 16-bit, motor control PWM advanced timer with programmable dead-time generation for output match
- Encoder interface controller with two inputs using quadrature decoder
- 24-bit SysTick timer down counter
- 2 watchdog timers (free watchdog timer and window watchdog timer)

The advanced timer (TIMER0) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general timer. The 4 independent channels can be used for input capture, output compare, PWM generation (edge- or center- aligned counting modes) and single pulse mode output. If configured as a general 16-bit timer, it has the same functions as the TIMERx. It can be synchronized with external signals or to interconnect with other general timers together which have the same architecture and features.

The general timer can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TIMER1 and TIMER2 are based on a 32-bit auto-reload up/down counter and a 16-bit prescaler. TIMER3 and TIMER4 is based on a 16-bit auto-reload up/down counter and a 16-bit prescaler. TIMER15 ~ TIMER16 are based on a 16-bit auto-reload up counter and a 16-bit prescaler. The general timer also supports an encoder interface with two inputs using quadrature decoder.

The basic timer TIMER5, is mainly used as a simple 16-bit time base.

The GD32F5HCxx devices have two watchdog peripherals, free watchdog timer and window watchdog timer. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-stage prescaler. It is clocked from an independent 32 KHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wakeup interrupt capability and the counter can be

frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. The features are shown below:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.17. Universal synchronous asynchronous receiver transmitter (USART)

- Automatic baud rate detection (USART0 and USART2)
- Maximum speed up to 25 MBits/s for USART0 and USART2
- Maximum speed up to 6.25 MBits/s for USART1
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- ISO 7816-3 compliant smart card interface
- Dual clock domain
- Wake up from Deep-sleep mode

The USART (USART0, USART1, USART2) are used to translate data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. The USART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART transmitter and receiver. The USART also supports DMA function for high speed data communication.

3.18. Inter-integrated circuit (I2C)

- Support both master and slave mode with a frequency up to 1 MHz (Fast mode plus)
- Provide arbitration function, optional PEC (packet error checking) generation and checking
- Supports 7-bit and 10-bit addressing mode and general call addressing mode
- SMBus 3.0 and PMBus 1.3 compatible
- Wakeup from Deep-sleep mode on I2C0 and I2C1 address match

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two-line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides different data transfer rates: up to 100 KHz in standard mode, up to 400 KHz in the fast mode and up to 1 MHz in the fast mode

plus. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

3.19. Serial peripheral interface (SPI)

- Support both master and slave mode
- Hardware CRC calculation and transmit automatic CRC error checking
- Quad-SPI configuration available in master mode (only in SPI0)

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). All SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking. Quad-SPI master mode is also supported in SPI0.

3.20. Inter-IC sound (I2S)

- Sampling frequency from 8 KHz to 192 KHz
- Support either master or slave mode

The Inter-IC sound (I2S) bus provides a standard communication interface for digital audio applications by 4-wire serial lines. GD32F5HCxx contain an I2S-bus interface that can be operated with 16/32-bit resolution in master or slave mode, pin multiplexed with SPI1. The audio sampling frequency from 8 KHz to 192 KHz is supported.

3.21. Serial / Quad parallel interface (SQPI)

- SQPI controller supports configuring output clock frequency which is divided by HCLK.
- SQPI controller supports no address phase and data phase operation which is named special command by the controller.
- SQPI controller supports 256MB external memory space.
  Logic memory address range: 0x6000 0000 - 0x6FFF FFFF.
- SQPI controller supports 6 types mode for different combination of command, address, wait cycle, and data phase.

Serial/Quad Parallel Interface (SQPI) is a controller for external serial/dual/quad parallel interface memory peripheral. For example: SQPI-PSRAM and SQPI-FLASH. With this controller, users can use external SQPI interface memory as SRAM simply.

3.22. Quad-SPI interface (QSPI)

- Three functional modes: indirect (address extend), status-polling and memory-mapped
- Command formats for both indirect and memory mapped mode
- Integrated FIFO for transmission/reception
- 8, 16, or 32-bit data accesses
- DMA channel for indirect mode

The QSPI is a specialized interface that communicate with Flash memories. This interface support single, dual or quad SPI FLASH.

3.23. Universal serial bus full-speed interface (USBFS)

- One USB device/host/OTG full-speed Interface with frequency up to 12 Mbps
- Internal main PLL for USB Clock compliantly
- Internal USBFS PHY support

The Universal Serial Bus (USB) is a 4-wire bus with 4 bidirectional endpoints. The device controller enables 12 Mbps data exchange with integrated transceivers. Transaction formatting is performed by the hardware, including CRC generation and checking. It supports both host and device modes, as well as OTG mode with Host Negotiation Protocol (HNP) and Session Request Protocol (SRP). The controller contains an internal full-speed USB PHY. For full-speed or low-speed operation, no external PHY chip is required. It supports all four types of transfer (control, bulk, Interrupt and isochronous) as defined in USB 2.0 protocol. The required precise 48 MHz clock which can be generated from the internal main PLL or by the internal 48 MHz oscillator in automatic trimming mode.

3.24. Cryptographic acceleration unit (CAU)

- Supports DES, TDES or AES (128, 192, or 256) algorithms.
- DES/TDES supports Electronic codebook (ECB) or Cipher block chaining (CBC) mode
- AES supports 128bits-key, 192bits-key or 256 bits-key
- AES supports Electronic codebook (ECB), Cipher block chaining (CBC) mode, Counter mode (CTR) mode, Galois/counter mode (GCM), Galois message authentication code mode (GMAC), Counter with CBC-MAC (CCM) Cipher Feedback mode (CFB) and Output Feedback mode (OFB).
- DMA transfer for incoming and outgoing data is supported

The Cryptographic Acceleration Unit supports acceleration of DES, TDES or AES (128, 192, or 256) algorithms. The DES/TDES supports Electronic codebook (ECB) or Cipher

block chaining (CBC) mode. The AES supports Electronic codebook (ECB), Cipher block chaining (CBC) mode, Counter mode (CTR) mode, Galois/counter mode (GCM), Galois message authentication code mode (GMAC), Counter with CBC-MAC (CCM), Cipher Feedback mode (CFB) and Output Feedback mode (OFB).

3.25. Hash acceleration unit (HAU)

- Supports SHA-1, SHA-224 and SHA-256 algorithms, compliant with FIPS PUB 180-2 (Federal Information Processing Standards Publication 180-2)
- Supports MD5 compliant with IETF RFC 1321 (Internet Engineering Task Force Request for Comments number 1321)
- Supports HMAC (keyed-hash message authentication code) algorithm
- Automatic swapping to comply with the big-endian or little-endian for MD5, SHA-1, SHA-224 and SHA-256 algorithms
- Automatic data padding to fill the 512-bit message block for digest computation
- Support DMA mode for input data flow

The HAU supports acceleration of SHA-1, SHA-224, SHA-256, MD5 algorithms and the HMAC (keyed-hash message authentication code) algorithm, which calls the SHA-1, SHA-224, SHA-256 or MD5 hash function to calculate the key, message, digest twice.

3.26. Public Key Cryptographic Acceleration Unit (PKCAU)

- Support RSA/DH algorithms with up to 3136 bits of operands
- Support ECC algorithm with up to 640 bits of operands
- Embedded RAM of 3584 bytes
- Conversion between the Montgomery domain and the natural domain
- only 32-bit access is supported

Public key encryption is also called asymmetric encryption, asymmetric encryption algorithms use different keys for encryption and decryption. The Public Key Cryptographic Acceleration Unit (PKCAU) can accelerate RSA (Rivest, Shamir and Adleman), Diffie-Hellmann (DH key exchange) and ECC (elliptic curve cryptography) in GF(p) (Galois domain). These operations are performed in the Montgomery domain to improve computational efficiency.

3.27. Infrared ray port (IFRP)

- The IFRP output signal is decided by TIMER15_CH0 and TIMER16_CH0.
- To get correct infrared ray signal, TIMER15 should generate low frequency modulation envelope signal, and TIMER16 should generate high frequency carrier signal.

Infrared ray port (IFRP) is used to control infrared light LED, and send out infrared data to implement infrared ray remote control.

There is no register in this module, which is controlled by TIMER15 and TIMER16. The IFRP_OUT pin can be configured by GPIO alternate function selected register.

3.28. Debug mode (DBG)

- Serial wire JTAG debug port (SWJ-DP)

The Arm® SWJ-DP Interface is embedded and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

3.29. Package and operation temperature

- BGA64 (GD32F5HCRIx6), QFN56 (GD32F5HCPIQx).
- Operation temperature range: -40°C to +85°C (industrial level).

4. Electrical characteristics

4.1. Parameter introduction

- Parameter conditions: Unless otherwise specified, all values given for V_{DD} = V_{DDA} = 3.3 V, T_A = 25°C, and all voltages are referenced to Vss.
- Value guaranteed by design, not 100% tested in production indicates that the value is derived from design or simulation and/or process characteristics.
- Value guaranteed by characterization, not 100% tested in production indicates that the value is derived from random test.
- Value guaranteed by sample, not 100% tested in production indicates that the value is derived from testing parameters with a small sample size.
- If the value is not specially indicated, it means the value guaranteed by 100% tested in production.

See the following table for some abbreviation terms and their descriptions in this chapter.

Table 4-1. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
GPIO	General Purpose Input / Output
PLL	Phase-Locked Loop
USBFS	Universal serial bus full-speed interface
SPI/I2S	Serial peripheral interface/Inter-IC sound (SPI/I2S)
SQPI	Serial / Quad Parallel Interface
QSPI	Quad-SPI interface
WWDGT	Window Watchdog Timer
FWDGT	Free Watchdog Timer
USART	Universal Synchronous / Asynchronous Receiver / Transmitter
I2C	Inter-Integrated Circuit Interface

4.2. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly beyond the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-2. Absolute maximum ratings (1)

Symbol	Description	Min	Max	Unit
V_{DD}	External voltage range(2)	V_{SS} - 0.3	V_{SS} + 4.0	V
V_{DDA}	External analog supply voltage(2)	V_{SSA} - 0.3	V_{SSA} + 4.0	V
V_{BAT}	External battery supply voltage(2)	V_{SS} - 0.3	V_{SS} + 4.0	V
V_{IN}	Input voltage on GPIO pin	V_{SS} - 0.3	V_{DD} + 4.0(3)	V
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	—	50	mV
$\lvert\Delta V_{SSx}\rvert$	Variations between V_{SS} ground pins	—	50	mV
I_{IO}	Maximum current for GPIO pin	—	20	mA
ΣI_{IO}	Maximum current sunk/sourced by all GPIO pin	—	100	
I_{DD}	Maximum current into each V_{DD} pin	—	100	
I_{SS}	Maximum current into each Vss pin	—	100	
ΣI_{DD}	Total current into all V_{DD} pins	—	200	
ΣI_{SS}	Total current into all V_{SS} pins	—	200	
I_{INJ}	Injected current on each GPIO pin(4)	—	-5/+0	
ΣI_{INJ}	Total injected current on all GPIO pins(5)	—	±25	
T_{STG}	Storage temperature range	-65	+150	°C
T_J	Maximum junction temperature(6)	—	125	°C

(1) Value guaranteed by design, not 100% tested in production.

(2) All power supply pins must be connected to the correct voltage range.

(3) V_{IN} maximum value cannot exceed 5.5 V.

(4) The device junction temperature must be kept below maximum T_J, otherwise it may cause permanent damage to the device.

(5) When several inputs are submitted to a current injection, the maximum ΣI_{INJ} is the absolute sum of the positive and negative injected currents (instantaneous values).

(6) The device junction temperature must be kept below maximum T_J, otherwise it may cause permanent damage to the device.

4.3. Operating conditions characteristics

Table 4-3. General operating conditions (1)

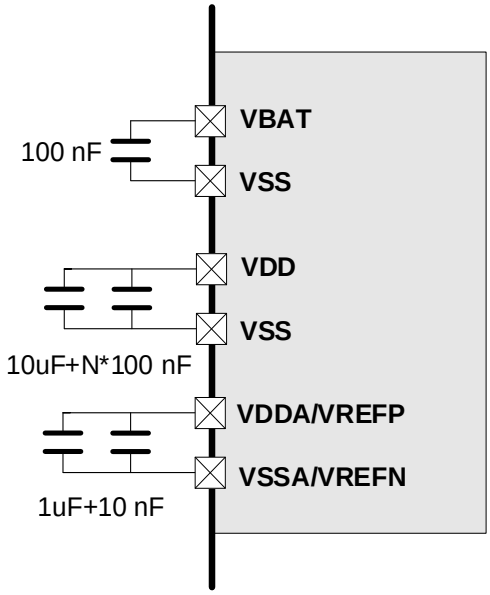
Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage	—	2.7	3.3	3.63	V
V_{DDA}	Analog supply voltage	—	2.7	3.3	3.63	
V_{BAT}(2)	Battery supply voltage	—	1.62	3.3	3.63	
V_{CORE}	Core logic supply voltage	LDOVS[1:0] = 0x	—	1.2	—	V

Symbol	Description	Conditions	Min	Typ	Max	Unit
	powered by internal voltage regulator	LDOVS[1:0] = 1x	—	1.1	—	V
f_{HCLK1}	AHB1 clock frequency	—	—	—	200	MHz
f_{APB1}	APB1 clock frequency	—	—	—	50	
f_{APB2}	APB2 clock frequency	—	—	—	100	
T_A	Ambient temperature	Grade 6 device	-40	—	+85	°C
		Grade 7 device	-40	—	+105	
P_D	Power dissipation at T_A = 85°C of BGA64(4x4)	—	—	—	556	mW
	Power dissipation at T_A = 85°C of QFN56	—	—	—	1044	
	Power dissipation at T_A = 105°C of QFN56	—	—	—	522	

(1) Value guaranteed by design, not 100% tested in production.

(2) In the application which V_{BAT} supply the backup domains, if the V_{BAT} voltage drops below the minimum value, when V_{DD} is powered on again, it is necessary to refresh the registers of backup domains and enable LXTAL again.

Figure 4-1. Recommended power supply decoupling capacitors (1)(2)



(1) When using precision internal reference voltage, and a bypass capacitor about 0.1 μF (or 1 μF connected in parallel, which is recommended) to ground is required.

(2) All decoupling capacitors need to be as close as possible to the pins on the PCB board.

4.4. Power supply requirement characteristics

Table 4-4. Power supply requirement characteristics(1)

Symbol	Description	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	—	—	∞	μs/V
	V_{DD} fall time rate	—	20	∞	
t_{VDDA}	V_{DDA} rise time rate	—	—	∞	μs/V
	V_{DDA} fall time rate	—	20	∞	
$f_{R(VDD/VDDA)}$	Allowable ripple frequency	$V_{R(VDD/VDDA)} \leq 0.2\ V_{DD}/V_{DDA}$	—	10	kHz
		$V_{R(VDD/VDDA)} \leq 0.08\ V_{DD}/V_{DDA}$	—	0.1	MHz
		$V_{R(VDD/VDDA)} \leq 0.06\ V_{DD}/V_{DDA}$	—	1	
$\Delta V_{DD}/V_{DDA}$ (2)	Allowable voltage change rising and falling gradient	When V_{DD}/V_{DDA} change exceeds V_{DD}/V_{DDA} ± 10%	1	—	ms/V

(1) Value guaranteed by design, not 100% tested in production.

(2) The ripple voltage must meet the allowable ripple frequency $f_{R(VDD/VDDA)}$ within the range between the V_{DD}/V_{DDA} upper limit (3.63 V) and lower limit (2.7 V). When the V_{DD}/V_{DDA} change exceeds V_{DD}/V_{DDA} ± 10%, the allowable voltage change rising and falling gradient $\Delta V_{DD}/V_{DDA}$ must be met.

4.5. Start-up timings of Operating conditions

Table 4-5. Start-up timings of Operating conditions (1)(2)(3)

Symbol	Description	Conditions	Typ	Unit
t_{ST}	Start-up time	Clock source from IRC16M	269.67	μs

(1) Value guaranteed by sample, not 100% tested in production.

(2) After power-up, the start-up time is the time between the rising edge of NRST high and the first I/O instruction.

(3) PLL is off.

(4) Excluding the time to initialize SRAM during startup.

4.6. Wake-up times from power saving modes

Table 4-6. Power saving mode wakeup timings characteristics (1)(2)

Symbol	Description	Conditions		Typ	Unit
t_{Sleep}	Wakeup from Sleep mode	ICACHE enable		0.75	μs
		ICACHE disable		7.32	
$t_{Deep-sleep}$	Wakeup from Deep-sleep mode	LDO in normal power and normal driver mode	ICACHE enable	2.24	
			ICACHE disable	113.67	
		LDO in low power and normal driver mode	ICACHE enable	2.24	
			ICACHE disable	113.67	
		LDO in normal power and low driver mode		113.67	
		LDO in low power and Low driver mode		113.67	

Symbol	Description	Conditions	Typ	Unit
$t_{Standby}$	Wakeup from Standby mode	—	274.00	

(1) Value guaranteed by sample, not 100% tested in production.

(2) The wakeup time is measured from the wakeup event to the point at which the application code reads the first instruction under the below conditions: $V_{DD} = V_{DDA} = 3.3$ V, IRC16M = System clock = 16 MHz.

4.7. Power consumption

The power consumption is measured as described in ***Figure 4-2. Power consumption measurement diagram*** The current consumption values are derived from the tests powered by VDD = VDDA except BKP_ONLY mode, while the current is ISUM. In BKP_ONLY mode, the RTC unit and LXTAL oscillator are powered by the VBAT, while the current is IBAT. Unless otherwise stated, VDD = VDDA = 3.3 V is applied to supply pins in typical current consumption columns, and VDD = VDDA = 3.63V is applied in maximum current consumption columns.

The MCU is configured under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- When the peripherals are enabled $4*f_{APB1} = 2*f_{APB2} = f_{HCLK}$

Figure 4-2. Power consumption measurement diagram

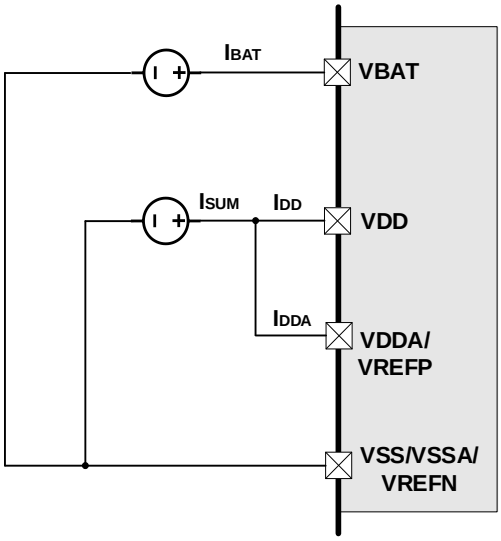


Table 4-7. Power consumption in Run mode (1)(2)

Symbol	Description	Conditions				Typ			Unit
		Execute from	Peripherals	General	f_{HCLK}	25°C	55°C	85°C	
I_{SUM}	Sum of supply current from V_{DD} and V_{DDA} (Run mode)	FLASH	All disabled	HXTAL = 25 MHz, PLL on, System clock = f_{HCLK1}	200MHz	30.56	31.48	33.57	mA
					180 MHz	28.56	29.36	31.40	
					168 MHz	26.88	27.63	29.66	
					120 MHz	20.09	20.81	22.74	
					108 MHz	18.41	19.10	21.01	
					96 MHz	16.72	17.39	19.29	
					72 MHz	13.33	14.00	15.83	
					48 MHz	9.96	10.58	12.36	
					36 MHz	8.26	8.88	10.63	
				IRC16M = 16 MHz, PLL off, System clock = 16 MHz	16 MHz	2.85	3.41	5.09	
					8 MHz	1.69	2.25	3.91	
					4 MHz	1.11	1.67	3.32	
					2 MHz	0.81	1.37	3.02	
			All enabled	HXTAL = 25 MHz, PLL on, System clock = f_{HCLK1}	200 MHz	54.78	55.98	58.46	
					180 MHz	50.29	51.32	53.82	
					168 MHz	47.16	48.16	50.59	
					120 MHz	34.59	35.49	37.69	
					108 MHz	31.46	32.32	34.48	
					96 MHz	28.32	29.14	31.24	
					72 MHz	22.05	22.80	24.81	
					48 MHz	15.77	16.46	18.36	
					36 MHz	12.62	13.29	15.13	

Symbol	Description	Conditions				Typ			Unit
		Execute from	Peripherals	General	f_{HCLK}	25°C	55°C	85°C	
				IRC16M = 16 MHz, PLL off, System clock = 16 MHz	16 MHz	4.78	5.37	7.07	
					8 MHz	2.66	3.23	4.91	
					4 MHz	1.59	2.16	3.83	
					2 MHz	1.05	1.62	3.28	
		SRAM	All disabled	HXTAL = 25 MHz, PLL on, System clock = f_{HCLK1}	200 MHz	19.26	20.07	21.96	
					180 MHz	17.65	18.37	20.32	
					168 MHz	16.68	17.39	19.32	
					120 MHz	12.81	13.48	15.35	
					108 MHz	11.85	12.51	14.36	
					96 MHz	10.89	11.54	13.38	
					72 MHz	8.96	9.59	11.41	
					48 MHz	7.03	7.64	9.43	
					36 MHz	6.07	6.67	8.44	
				IRC16M = 16 MHz, PLL off, System clock = 16 MHz	16 MHz	1.81	2.37	4.082	
					8 MHz	1.16	1.72	3.43	
					4 MHz	0.84	1.40	3.10	
					2 MHz	0.68	1.23	2.94	
			All enabled	HXTAL = 25 MHz, PLL on, System clock = f_{HCLK1}	200 MHz	53.06	54.30	56.82	
					180 MHz	48.76	49.82	52.30	
					168 MHz	45.72	46.75	49.19	
					120 MHz	33.57	34.48	36.70	
					108 MHz	30.54	31.41	33.57	
					96 MHz	27.50	28.34	30.46	
					72 MHz	21.43	22.20	24.21	

Symbol	Description	Conditions				Typ			Unit
		Execute from	Peripherals	General	f_{HCLK}	25°C	55°C	85°C	
					48 MHz	15.35	16.06	17.97	
					36 MHz	12.31	12.99	14.84	
				IRC16M = 16 MHz, PLL off, System clock = 16 MHz	16 MHz	4.64	5.23	6.95	
					8 MHz	2.58	3.17	4.85	
					4 MHz	1.55	2.13	3.81	
					2 MHz	1.03	1.61	3.27	

(1) Value guaranteed by sample, not 100% tested in production.

(2) During power consumption test, GPIO needs to be configure as Analog Input mode.

Table 4-8. Power consumption in Sleep mode (1) (2)

Symbol	Description	Conditions				Typ			Unit
		Execute from	Peripherals	General	f_{HCLK}	25°C	55°C	85°C	
I_{SUM}	Sum of supply current from V_{DD} and V_{DDA} (sleep mode)	FLASH	All disabled(4)	HXTAL = 25 MHz, PLL on, System clock = f_{HCLK1}, CPU clock off	200 MHz	17.47	18.28	20.19	mA
					180 MHz	16.01	16.72	18.59	
					168 MHz	15.15	15.86	17.72	
					120 MHz	11.72	12.39	14.19	
					108 MHz	10.87	11.52	13.31	
					96 MHz	10.01	10.66	12.43	
					72 MHz	8.31	8.94	10.68	
					48 MHz	6.60	7.21	8.92	
					36 MHz	5.74	6.34	8.04	
				IRC16M = 16 MHz, PLL off, System	16 MHz	1.65	2.22	3.86	
					8 MHz	1.09	1.65	3.29	
					4 MHz	0.80	1.36	3.00	

Symbol	Description	Conditions				Typ			Unit
		Execute from	Peripherals	General	f_{HCLK}	25°C	55°C	85°C	
				clock = 16 MHz, CPU clock off	2 MHz	0.66	1.22	2.85	
			All enabled	HXTAL = 25 MHz, PLL on, System clock = f_{HCLK1}, CPU clock off	200 MHz	42.14	43.24	45.58	
					180 MHz	38.24	39.19	41.44	
					168 MHz	35.90	36.83	39.05	
					120 MHz	26.55	27.38	29.44	
					108 MHz	24.22	25.02	27.04	
					96 MHz	21.88	22.66	24.64	
					72 MHz	17.21	17.94	19.84	
					48 MHz	12.53	13.21	15.04	
					36 MHz	10.20	10.85	12.63	
				IRC16M = 16 MHz, PLL off, System clock = 16 MHz, CPU clock off	16 MHz	3.63	4.22	5.89	
					8 MHz	2.08	2.65	4.31	
					4 MHz	1.30	1.87	3.51	
					2 MHz	0.91	1.47	3.11	
		SRAM	All disabled(3)	HXTAL = 25 MHz, PLL on, System clock = f_{HCLK1}, CPU clock off	200 MHz	19.26	20.09	22.02	
					180 MHz	17.64	18.38	20.36	
					168 MHz	16.68	17.40	19.37	
					120 MHz	12.81	13.49	15.39	
					108 MHz	11.85	12.52	14.40	
					96 MHz	10.89	11.54	13.42	
					72 MHz	8.96	9.60	11.44	
					48 MHz	7.03	7.65	9.46	
					36 MHz	6.07	6.67	8.47	

Symbol	Description	Conditions				Typ			Unit
		Execute from	Peripherals	General	f_{HCLK}	25°C	55°C	85°C	
				IRC16M = 16 MHz, PLL off, System clock = 16 MHz, CPU clock off	16 MHz	1.81	2.38	4.11	
					8 MHz	1.16	1.73	3.45	
					4 MHz	0.84	1.40	3.12	
					2 MHz	0.68	1.24	2.96	
			All enabled	HXTAL = 25 MHz, PLL on, System clock = f_{HCLK1}, CPU clock off	200 MHz	42.12	43.23	45.56	
					180 MHz	38.24	39.19	41.46	
					168 MHz	35.90	36.83	39.06	
					120 MHz	26.55	27.38	29.45	
					108 MHz	24.22	25.02	27.04	
					96 MHz	21.88	22.66	24.65	
					72 MHz	17.21	17.94	19.85	
					48 MHz	12.54	13.22	15.04	
					36 MHz	10.20	10.85	12.64	
				IRC16M = 16 MHz, PLL off, System clock = 16 MHz, CPU clock off	16 MHz	3.64	4.22	5.89	
					8 MHz	2.08	2.65	4.31	
					4 MHz	1.30	1.87	3.52	
					2 MHz	0.91	1.48	3.12	

(1) Value guaranteed by sample, not 100% tested in production.

(2) During power consumption test, GPIO needs to be configure as Analog Input mode.

(3) FMC clock on.

Table 4-9. Power consumption in Deep-sleep mode (1)(2)(3)

Symbol	Description	Conditions		Typ			Unit
		General	V_{DD}	25°C	55°C	85°C	
I_{SUM}			2.7V	0.26	0.65	1.79	mA

Symbol	Description	Conditions		Typ			Unit
		General	V_{DD}	25°C	55°C	85°C	
	Sum of supply current from V_{DD} and V_{DDA} (Deep-sleep mode)	LDO in normal power and normal driver mode, IRC32K off, RTC off	3.3V	0.26	0.65	1.80	
			3.63V	0.27	0.65	1.80	
		LDO in normal power and low driver mode, IRC32K off, RTC off	2.7V	0.24	0.63	1.77	
			3.3V	0.24	0.63	1.77	
			3.63V	0.24	0.63	1.77	
		LDO in low power and normal driver mode, IRC32K off, RTC off	2.7V	0.21	0.60	1.75	
			3.3V	0.21	0.60	1.75	
			3.63V	0.21	0.60	1.75	
		LDO in low power and Low driver mode, IRC32K off, RTC off	2.7V	0.19	0.57	1.70	
			3.3V	0.19	0.57	1.71	
			3.63V	0.19	0.57	1.71	

(1) Value guaranteed by sample, not 100% tested in production.
(2) During power consumption test, GPIO needs to be configure as Analog Input mode.
(3) The V_{CORE} in the stop mode of this data is 1.1V.

Table 4-10. Power consumption in Standby mode [(1)(2)]

Symbol	Description	Conditions		Typ			Unit
		General	V_{DD}	25°C	55°C	85°C	
I_{SUM}	Sum of supply current from V_{DD} and V_{DDA} (Standby mode)	LXTAL off, IRC32K on, RTC on	2.7V	3.76	4.07	5.42	μA
			3.3V	4.53	5.09	7.14	
			3.63V	5.10	5.87	8.42	
		LXTAL off, IRC32K on, RTC off	2.7V	3.54	3.84	5.20	
			3.3V	4.25	4.81	6.85	
			3.63V	4.78	5.56	8.09	
		LXTAL off, IRC32K off, RTC off	2.7V	2.99	3.31	4.66	
			3.3V	3.63	4.20	6.25	

Symbol	Description	Conditions		Typ			Unit
		General	V_{DD}	25°C	55°C	85°C	
			3.63V	4.12	4.90	7.44	

(1) Value guaranteed by sample, not 100% tested in production.

(2) During power consumption test, GPIO needs to be configure as Analog Input mode.

Table 4-11. Power consumption in BKP_ONLY mode (1)(2)

Symbol	Description	Conditions		Typ			Unit
		General	V_{BAT}	25°C	55°C	85°C	
I_{BAT}	LXTAL+RTC current from V_{BAT} (BKP_ONLY mode)	V_{DD} off, LXTAL on with external crystal, RTC on, LXTAL High driving	1.62V	1.64	1.81	2.08	µA
			2.7V	1.88	2.07	2.39	
			3.3V	2.01	2.22	2.60	
			3.63V	2.14	2.39	2.85	
		V_{DD} off, LXTAL on with external crystal, RTC on, LXTAL Medium High driving	1.62V	1.27	1.40	1.64	
			2.7V	1.43	1.57	1.85	
			3.3V	1.56	1.73	2.06	
			3.63V	1.68	1.89	2.30	
		V_{DD} off, LXTAL on with external crystal, RTC on, LXTAL Medium Low driving	1.62V	0.84	0.93	1.12	
			2.7V	1.00	1.10	1.32	
			3.3V	1.12	1.24	1.53	
			3.63V	1.24	1.40	1.76	
		V_{DD} off, LXTAL on with external crystal, RTC on, LXTAL Low driving	1.62V	0.69	0.76	0.94	
			2.7V	0.84	0.93	1.14	
			3.3V	0.96	1.07	1.34	
			3.63V	1.08	1.23	1.58	

(1) Value guaranteed by sample, not 100% tested in production.

(2) During power consumption test, GPIO needs to be configure as Analog Input mode.

The current consumption of the on-chip peripherals is given in the following table. To avoid adding the CPU dynamic power consumption to the peripheral power consumption, the MCU needs to enter sleep mode to stop the CPU operation during current measurement. The MCU is configured under the following conditions:

- All I/O pins are in analog input mode
- The given value is in the table calculated by measuring the difference of the current consumptions:
  -- The target peripheral is clocked on and enters sleep mode
  -- All peripherals are clocked off and enter sleep mode

The power consumption of the digital part of the on-chip peripherals is given in the following table. The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

The values in the table are equal to the peripheral current divided by the clock frequency of the corresponding bus.

Table 4-12. Peripheral current consumption characteristics(1)

Bus	Peripherials	Typical consumption	Unit
AHB1	GPIOA	0.49	μA/MHz
	GPIOB	0.50	
	GPIOC	0.50	
	GPIOD	0.41	
	TZPCU	2.87	
	CRC	0.19	
	FMC	30.24	
	SRAM0	1.01	
	SRAM1	0.86	
	SRAM2	0.95	
	SRAM3	1.30	
	DMA0	7.36	
	DMA1	7.52	
	USBFS	18.21	
AHB2	PKCAU	7.80	
	CAU	47.96	
	HAU	2.93	
	TRNG	0.34	
AHB3	SQPI	0.98	
	QSPI	2.39	
APB1	TIMER1	6.94	
	TIMER2	6.86	
	TIMER3	5.57	
	TIMER4	5.43	
	TIMER5	0.83	
	WWDGT	0.28	

Bus	Peripherials	Typical consumption	Unit
	SPI1	1.45	
	USART1	1.57	
	USART0	4.76	
	I2C0	4.02	
	I2C1	4.05	
	CTC	0.29	
	PMU	11.71	
APB2	TIMER0	9.14	
	USART2	4.84	
	ADC	1.55	
	SPI0	0.57	
	SYSCFG	0.81	
	TIMER15	3.04	
	TIMER16	3.08	

(1) Value guaranteed by sample, not 100% tested in production.

4.8. EMC characteristics

System level ESD (Electrostatic discharge, according to IEC 61000-4-2) and EFT (Electrical Fast Transient/burst, according to IEC 61000-4-4) testing result is given in the ***Table 4-13. EMS characteristics*** [(1) (2)]. System level ESD is for end-customer operation, it includes ESD field events on system level occur in an unprotected area (outside EPA). System level ESD protection necessary to satisfy higher ESD levels.

Table 4-13. EMS characteristics [(1) (2)]

Symbol	Description	Conditions	Package	Measurement value	Level
V_{ESD}	Contact / Air mode high voltage stressed on few special I/O pins	V_{DD} = 3.3 V, T_A = 25 °C, f_{HCLK} = 200 MHz IEC 61000-4-2	BGA64	CD 6KV AD 8KV	3A
V_{EFT}	Fast transient high voltage burst stressed on Power and GND	V_{DD} = 3.3 V, T_A = 25 °C, f_{HCLK} = 200 MHz IEC 61000-4-4	BGA64	4KV	4A

(1) Value guaranteed by sample, not 100% tested in production.

(2) The explanation of the evaluation methods for system-level ESD and system-level EFT test methods and test levels can be referred to in AN127 and AN128.

EMI (Electromagnetic Interference) emission test result is given in the ***Table 4-14. EMI characteristics*** [(1)(2)], The electromagnetic field emitted by the device are monitored while an application, executing EEMBC code, is running. The test is compliant with SAE J1752-3 standard which specifies the test board and the pin loading.

Table 4-14. EMI characteristics (1)(2)

Symbol	Description	Conditions	Package	Max vs. [f_{HXTAL}/f_{HCLK}] 40/200 MHz			Unit
				0.1-30MHz	30-130MHz	130MHz-1GHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, f_{HCLK} = 200 MHz, conforms to SAE J1752-3	BGA64	-7.22	4.98	9.35	dBμV

(1) Value guaranteed by sample, not 100% tested in production.

(2) The explanation of the chip-level EMI test methods can be referred to in AN125.

Component level ESD include HBM (Human body model, according to ANSI/ESDA/JEDEC JS-001) and CDM (ANSI/ESDA/JEDEC JS-002), that ESD field events during manufacturing in an ESD protected area, such as PCB assembly/repair, IC assembly/test and Fab environment. The ESD protected area (EPA) has many measures, for instance ESD protective packaging, grounding person wrist strap to ground (or flooring/footwear), grounded work surface and ionizer.

Static latch-up (LU, according to JEDEC78) test is based on the two measurement methods, I/O current injection value (I-test) and power supply over-voltage value.

Table 4-15. Component level ESD characteristics latch-up characteristics (1) (2)

Symbol	Description	Conditions	Package	Max	Unit	Level
V_{HBM}	Human body model electrostatic discharge voltage (Any pin combination)	T_A = 25 °C; JS-001	BGA64	2000	V	2
V_{CDM}	Charge device model electrostatic discharge voltage (All pins)	T_A = 25 °C; JS-002	BGA64	500	V	C2a
LU	I-test	T_A = 125 °C; JESD78	BGA64	±200	mA	Class II Level A
	V_{supply} over voltage			5.4	V	

(1) Value guaranteed by sample, not 100% tested in production.

(2) The levels of system-level ESD and chip-level ESD are not related. The differences between the two can be referred to in AN159.

4.9. Power supply supervisor characteristics

Table 4-16. Power supply supervisor characteristics(1)

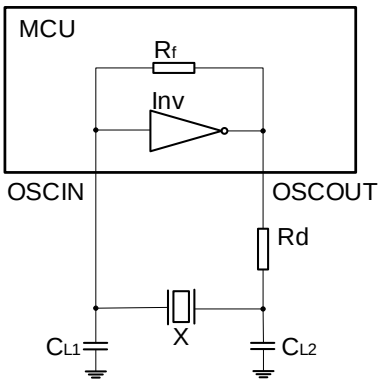
Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{LVD}	Low Voltage Detector Threshold	LVDT[2:0] = 000, rising edge	—	2.14	—	V
		LVDT[2:0] = 000, falling edge	—	2.04	—	V
		LVDT[2:0] = 001, rising edge	—	2.28	—	V

Symbol	Description	Conditions	Min	Typ	Max	Unit
		LVDT[2:0] = 001, falling edge	—	2.18	—	V
		LVDT[2:0] = 010, rising edge	—	2.42	—	V
		LVDT[2:0] = 010, falling edge	—	2.32	—	V
		LVDT[2:0] = 011, rising edge	—	2.56	—	V
		LVDT[2:0] = 011, falling edge	—	2.46	—	V
		LVDT[2:0] = 100, rising edge	—	2.7	—	V
		LVDT[2:0] = 100, falling edge	—	2.6	—	V
		LVDT[2:0] = 101, rising edge	—	2.84	—	V
		LVDT[2:0] = 101, falling edge	—	2.74	—	V
		LVDT[2:0] = 110, rising edge	—	2.98	—	V
		LVDT[2:0] = 110, falling edge	—	2.88	—	V
		LVDT[2:0] = 111, rising edge	—	3.12	—	V
		LVDT[2:0] = 111, falling edge	—	3.02	—	V
$V_{LVDhyst}$	LVD hysteresis	—	—	100	—	mV
V_{VLVD}	V_{DDA} Low Voltage Detector Threshold	Rising edge	—	2.4	—	V
		Falling edge	—	2.28	—	V
$V_{VLVDhyst}$	VLVD hysteresis	—	—	120	—	mV
V_{POR}	Power on reset threshold	—	—	1.536	—	V
V_{PDR}	Power down reset threshold		—	1.5	—	V
$V_{PDRhyst}$	PDR hysteresis		—	36	—	mV
$t_{RSTTEMPO}$	Reset temporization		—	2.3	—	ms

(1) Value guaranteed by design, not 100% tested in production.

4.10. External clock characteristics

Figure 4-3. Internal structure diagram of OSCIN and OSCOUT pin



It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine which load capacitors will best tune their resonator/crystal to the microcontroller device for optimum start-up and operation over temperature/voltage extremes.

Table 4-17. High speed external clock (HXTAL) generated from a crystal/ceramic characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{HXTAL}	Crystal or ceramic frequency	—	19.2	40	52	MHz
R_F	Feedback resistor	V_{DD} = V_{DDA} = 3.3 V	—	400	—	kΩ
C_{HXTAL}(2)	Recommended matching capacitance on OSCIN and OSCOUT	—	—	20	30	pF
$Duty_{HXTAL}$	Crystal or ceramic duty cycle	—	30	-	70	%
g_m (3)	Oscillator transconductance	Startup	—	—	62	mA/V
$I_{DD(HXTAL)}$	Crystal or ceramic operating current	V_{DD} = V_{DDA} = 3.3 V f_{HXTAL} = 52MHz	—	2.5	—	mA
$t_{ST(HXTAL)}$	Crystal or ceramic startup time	V_{DD} = V_{DDA} = 3.3 V f_{HXTAL} = 19.2 MHz	—	1.2	—	ms

(1) Value guaranteed by design, not 100% tested in production.

(2) C_{HXTAL1} = C_{HXTAL2} = 2*(C_{LOAD} - C_S), For C_{HXTAL1} and C_{HXTAL2}, it is recommended matching capacitance on OSCIN and OSCOUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

(3) More details about g_m could be found in ***AN052 GD32 MCU Resonator-Based Clock Circuits.***

Table 4-18. High speed external clock characteristics (HXTAL in bypass mode) (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{HXTAL_ext}	External clock source or oscillator frequency	—	19.2	40	52	MHz
$V_{H(HXTAL)}$	OSCIN input pin high level	V_{DD} = V_{DDA} = 3.3 V	0.7*V_{DDA}	—	V_{DDA}	V

Symbol	Description	Conditions	Min	Typ	Max	Unit
	voltage					
$V_{L(HXTAL)}$	OSCIN input pin low level voltage		V_{SSA}	—	0.3*V_{DDA}	V
C_{IN}	OSCIN input capacitance	—	—	5	—	pF
$Duty_{HXTAL}$	Duty cycle	—	30	—	70	%

(1) Value guaranteed by design, not 100% tested in production.

Table 4-19. Low speed external clock (LXTAL) generated from a crystal/ceramic characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{LXTAL}	Crystal or ceramic frequency	—	—	32.768	—	kHz
C_{LXTAL}(2)	Recommended matching capacitance on OSC32IN and OSC32OUT	—	—	15	—	pF
$Duty_{LXTA}$	Crystal or ceramic duty cycle	—	30	—	70	%
g_m(4)	Oscillator transconductance	Lower driving capability	—	4.5	—	μA/V
		Medium low driving capability	—	6.5	—	
		Medium high driving capability	—	13	—	
		Higher driving capability	—	19	—	
$I_{DD(LXTAL)}$	Crystal or ceramic operating current	Lower driving capability	—	0.5	—	μA
		Medium low driving capability	—	0.6	—	
		Medium high driving capability	—	0.9	—	
		Higher driving capability	—	1.2	—	
$t_{ST(LXTAL)}$(3)	Crystal or ceramic startup time	V_{DD} = V_{DDA} = 3.3 V	—	2	—	s

(1) Value guaranteed by design, not 100% tested in production.

(2) C_{LXTAL1} = C_{LXTAL2} = 2*(C_{LOAD} - C_S), For C_{LXTAL1} and C_{LXTAL2}, it is recommended matching capacitance on OSC32IN and OSC32OUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

(3) $t_{ST(LXTAL)}$ is the startup time measured from the moment it is enabled (by software) to the 32.768 kHz oscillator stabilization flags is SET. This value varies significantly with the crystal manufacturer.

(4) More details about g_m could be found in ***AN052 GD32 MCU Resonator-Based Clock Circuits.***

Table 4-20. Low speed external user clock characteristics (LXTAL in bypass mode) (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{LXTAL_ext}	External clock source or oscillator frequency	V_{DD} = 3.3 V	—	32.768	1000	kHz
$V_{H(LXTAL)}$	OSC32IN input pin high level voltage	V_{DD} = 3.3 V	0.7*V_{DD}	—	V_{DD}	V
$V_{L(LXTAL)}$	OSC32IN input pin low level voltage	V_{DD} = 3.3 V	V_{SS}	—	0.3*V_{DD}	
C_{IN}	OSC32IN input capacitance	—	—	5	—	pF
$Duty_{LXTAL}$	Duty cycle	—	30	—	70	%

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-4. Recommended external OSCIN and OSCOUT pins circuit for crystal

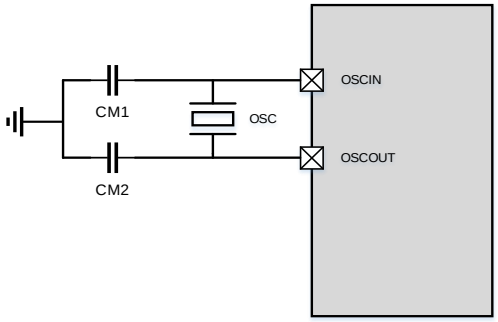
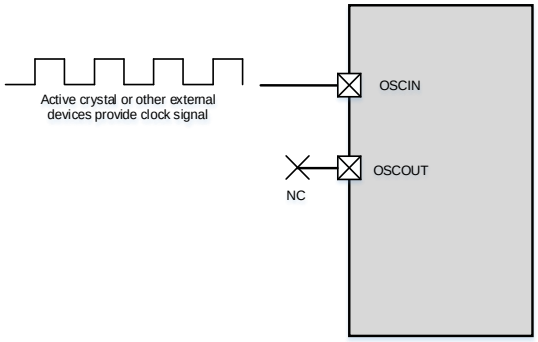


Figure 4-5. Recommended external OSCIN and OSCOUT pins circuit for oscillator



4.11. Internal clock characteristics

Table 4-21. High speed internal clock (IRC16M) characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{IRC16M}	High Speed Internal Oscillator (IRC16M) frequency	V_{DD} = V_{DDA} = 3.3 V	TBD	16	TBD	MHz
$Drift_{IRC16M}$	IRC16M oscillator Frequency drift, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_A = 25°C	TBD	—	TBD	%
		2.7 V≤ V_{DD} = V_{DDA} ≤ 3.63 V, T_A = -40 °C ~ +85 °C(2)	TBD	—	TBD	%
$Trim_{IRC16M}$(1)	IRC16M oscillator user trimming step	—	—	0.5	—	%
$Duty_{IRC16M}$(1)	IRC16M oscillator duty cycle	—	45	50	55	%
$I_{DDA(IRC16M)}$(1)	IRC16M oscillator operating current	V_{DD} = V_{DDA} = 3.3 V	—	90	—	μA
$t_{ST(IRC16M)}$(1)	IRC16M oscillator startup time	V_{DD} = V_{DDA} = 3.3 V	—	1.6	—	μs

(1) Value guaranteed by design, not 100% tested in production.
(2) Value guaranteed by characterization, not 100% tested in production.

Table 4-22. High speed internal clock (IRC48M) characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{IRC48M}	High Speed Internal Oscillator (IRC48M) frequency	V_{DD} = V_{DDA} = 3.3 V	TBD	48	TBD	MHz
$Drift_{IRC48M}$	IRC48M oscillator Frequency drift, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_A = 25°C	TBD	—	TBD	%
		2.7 V≤ V_{DD} = V_{DDA} ≤ 3.63 V, T_A = -40 °C ~ +85 °C(2)	TBD	—	TBD	%
$Trim_{IRC48M}$(1)	IRC48M oscillator user trimming step(1)	—	—	0.13	—	%
$Duty_{IRC48M}$(1)	IRC48M oscillator duty cycle	—	45	50	55	%
$I_{DDA(IRC48M)}$(1)	IRC48M oscillator operating current	V_{DD} = V_{DDA} = 3.3 V	—	340	—	μA
$t_{ST(IRC48M)}$(1)	IRC48M oscillator startup time	V_{DD} = V_{DDA} = 3.3 V	—	1.3	—	μs

(1) Value guaranteed by design, not 100% tested in production.
(2) Value guaranteed by characterization, not 100% tested in production.

Table 4-23. Low speed internal clock (IRC32K) characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{IRC32K}	Low Speed Internal oscillator (IRC32K) frequency	V_{DD} = 3.3 V	TBD	32	TBD	kHz
$Drift_{IRC32K}$	IRC32K oscillator Frequency accuracy, Factory-trimmed	V_{DD} = 3.3 V, T_A = 25°C	TBD	—	TBD	%
		2.7 V ≤ V_{DD} ≤ 3.63 V, T_A = -40 °C ~ +85 °C	TBD	—	TBD	%
$I_{DDA(IRC32K)}$(1)	IRC32K oscillator operating current	V_{DD} = = 3.3 V	—	0.4	—	μA
$t_{ST(IRC32K)}$(1)	IRC32K oscillator startup time	V_{DD} = 3.3 V	—	20	—	μs

(1) Value guaranteed by design, not 100% tested in production.

4.12. PLL characteristics

The parameters given in ***Table 4-24*** are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in ***Table 4-3. General operating conditions***.

Table 4-24. PLL characteristics(1)

Symbol	Description	Conditions		Min	Typ	Max	Unit
$f_{IN(PLL)}$	PLL input clock frequency	—		1	—	2	MHz
$f_{OUT(PLL)}$	PLL output clock frequency	—		64	—	500	MHz
f_{VCO}	PLL VCO output clock frequency	—		64	—	500	MHz
$t_{LK(PLL)}$	PLL lock time	—		—	—	300	μs
$I_{DDA(PLL)}$	Current consumption from V_{DDA}	VCO freq = 500 MHz		—	2.2	—	mA
J_{PLL}(2)	Cycle to cycle Jitter（rms）	f_{PLL_OUT} = f_{VCO_OUT} / 10	f_{VCO_OUT}= 500 MHz	—	30	—	ps
	Cycle to cycle Jitter（peak to peak）			—	210	—	

(1) Value guaranteed by design, not 100% tested in production.

(2) Value given with main PLL running.

Table 4-25. PLLI2S characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
$f_{IN(PLL)}$	PLL input clock frequency	—	2	—	16	MHz
$f_{OUT(PLL)}$	PLL output clock frequency	—	—	—	550	MHz
f_{VCO}	PLL VCO output clock	—	—	—	550	MHz

Symbol	Description	Conditions		Min	Typ	Max	Unit
	frequency						
$t_{LK(PLL)}$	PLL lock time	—		—	—	300	μs
$I_{DDA(PLL)}$	Current consumption from V_{DDA}	VCO freq = 550 MHz		—	1.5	—	mA
J_{PLL}(2)	Cycle to cycle Jitter（rms）	f_{PLL_OUT} = f_{VCO_OUT} / 10	f_{VCO_OUT}= 550 MHz	—	40	—	ps
	Cycle to cycle Jitter（peak to peak）			—	400	—	

(1) Value guaranteed by design, not 100% tested in production.
(2) Value given with main PLL running.

4.13. Memory characteristics

Table 4-26. Flash memory characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
$I_{DD(FLASH)}$(1)	Average supply current from V_{DD} during FLASH operation	Erasing	—	17.8	—	mA
		Programming	—	8.1	—	
PE_{CYC}(2)	Number of guaranteed program /erase cycles before failure (Endurance)	T_A range(5)	100	—	—	kcycles
t_{RET}(3)	Data retention time	T_A = 70 °C after up to 0 kcycle	—	20	—	years
t_{PROG}(2)	Word programming time	T_A range(5)	—	47.5	106	μs
t_{PER}(2)	Page(4) erase time	T_A range(5)	—	45	300	ms
t_{MERASE}(2)	Mass erase time	T_A range(5)	—	6	20	s

(1) Value guaranteed by sample, not 100% tested in production.
(2) Value guaranteed by design, not 100% tested in production.
(3) Value guaranteed by characterization, not 100% tested in production.
(4) 4KB.
(5) For grade 6 devices, T_A range= -40°C ~ +85°C. For grade 7 devices, T_A range= -40°C ~ +105°C.

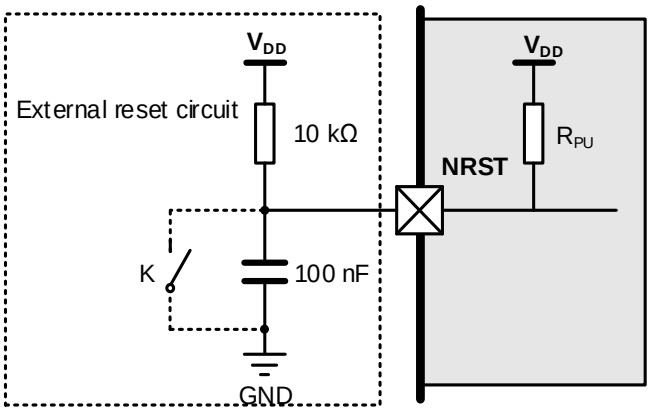
4.14. NRST pin characteristics

Table 4-27. NRST pin characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST Input low level voltage	V_{DD} = V_{DDA} = 3.3 V	—	—	0.35V_{DD}	V
$V_{IH(NRST)}$	NRST Input high level voltage	V_{DD} = V_{DDA} = 3.3 V	0.65V_{DD}	—	—	
V_{HYST}	Schmidt trigger Voltage hysteresis	V_{DD} = V_{DDA} = 3.3 V	270	—	—	mV
R_{PU}	Pull-up equivalent resistor	V_{IN} = V_{SS}	—	40	—	kΩ
t_{NRST}	Generated reset pulse duration	—	20	—	—	us

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-6. Recommended external NRST pin circuit(1)



(1) Unless the voltage on NRST pin go below $V_{IL(NRST)}$ level, the device would not generate a reliable reset.

4.15. GPIO characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures. The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the -5μA/+0μA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Table 4-28. GPIO current injection susceptibility (1)

Symbol	Description		Functional susceptibility		Unit
			Negative injection	Positive injection	
I_{INJ}(1)	Injected current on pin	Input current on GPIO pins	-5	NA(2)	mA

(1) Value guaranteed by design, not 100% tested in production.
(2) NA: Not applicable.

More details about GPIO could be found in ***AN092 GD32 MCU GPIO structure and precautions***.

Table 4-29. I/O static characteristics

Symbol	Description		Conditions	Min	Typ	Max	Unit
V_{IL}(1)	IO low level input voltage		2.7 V < V_{DD} = V_{DDA} < 3.63 V	—	—	0.35V_{DD}	V
V_{IH}(1)	IO high level input voltage		2.7 V < V_{DD} = V_{DDA} < 3.63 V	0.65V_{DD}	—	—	V
V_{HYS}(1)	Input hysteresis		—	—	480	—	mV
I_{LEAK}	IO input leakage current		V_{IN} = 5 V	-2	—	+2	uA
R_{PU}(1)	Weak pull-up equivalent resistor	All Pins	V_{IN} = V_{SS}	—	40	—	kΩ
R_{PD}(1)	Weak pull-down equivalent resistor	All Pins	V_{IN} = V_{DD}	—	40	—	kΩ

(1) Value guaranteed by design, not 100% tested in production.

Table 4-30. Output voltage characteristics for all I/Os except PC13, PC14, PC15 (1)(2)

Symbol	Description	Conditions	Typ	Unit
V_{OL} (IO_speed = 166 MHz)	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 2.7 V	0.09	V
		V_{DD} = 3.3 V	0.09	
		V_{DD} = 3.63 V	0.09	
V_{OL} (IO_speed = 166 MHz)	Low level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 2.7 V	0.24	
		V_{DD} = 3.3 V	0.22	
		V_{DD} = 3.63 V	0.22	
V_{OH} (IO_speed = 166 MHz)	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 2.7 V	2.57	
		V_{DD} = 3.3 V	3.20	
		V_{DD} = 3.63 V	3.50	
V_{OH} (IO_speed = 166 MHz)	High level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 2.7 V	2.37	
		V_{DD} = 3.3 V	3.02	
		V_{DD} = 3.63 V	3.36	
V_{OL} (IO_speed=25MHz)	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 2.7 V	0.12	V
		V_{DD} = 3.3 V	0.12	
		V_{DD} = 3.63 V	0.11	
	Low level output voltage for an IO Pin (I_{IO} = +12 mA)	V_{DD} = 2.7 V	0.19	
		V_{DD} = 3.3 V	0.18	
		V_{DD} = 3.63 V	0.17	
V_{OH} (IO_speed=25MHz)	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 2.7 V	2.52	
		V_{DD} = 3.3 V	3.15	
		V_{DD} = 3.63 V	3.48	

Symbol	Description	Conditions	Typ	Unit
	High level output voltage for an IO Pin (I_{IO} = +12 mA)	V_{DD} = 2.7 V	2.43	
		V_{DD} = 3.3 V	3.06	
		V_{DD} = 3.63 V	3.40	
V_{OL} (IO_speed=10MHz)	Low level output voltage for an IO Pin (I_{IO} = +4 mA)	V_{DD} = 2.7 V	0.10	V
		V_{DD} = 3.3 V	0.09	
		V_{DD} = 3.63 V	0.09	
	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 2.7 V	0.20	
		V_{DD} = 3.3 V	0.18	
		V_{DD} = 3.63 V	0.18	
V_{OH} (IO_speed=10MHz)	High level output voltage for an IO Pin (I_{IO} = +4 mA)	V_{DD} = 2.7 V	2.57	
		V_{DD} = 3.3 V	3.19	
		V_{DD} = 3.63 V	3.53	
	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 2.7 V	2.43	
		V_{DD} = 3.3 V	3.07	
		V_{DD} = 3.63 V	3.42	
V_{OL} (IO_speed=2MHz)	Low level output voltage for an IO Pin (I_{IO} = +1 mA)	V_{DD} = 2.7 V	0.07	V
		V_{DD} = 3.3 V	0.06	
		V_{DD} = 3.63 V	0.06	
	Low level output voltage for an IO Pin (I_{IO} = +4 mA)	V_{DD} = 2.7 V	0.29	
		V_{DD} = 3.3 V	0.26	
		V_{DD} = 3.63 V	0.26	
V_{OH} (IO_speed=2MHz)	High level output voltage for an IO Pin (I_{IO} = +1 mA)	V_{DD} = 2.7 V	2.58	
		V_{DD} = 3.3 V	3.19	
		V_{DD} = 3.63 V	3.54	
	High level output voltage for an IO Pin (I_{IO} = +4 mA)	V_{DD} = 2.7 V	2.18	
		V_{DD} = 3.3 V	2.86	
		V_{DD} = 3.63 V	3.22	

(1) Value guaranteed by sample, not 100% tested in production.

(2) All pins except PC13 / PC14 / PC15. Since PC13 to PC15 are supplied through the Power Switch, which can only be obtained by a small current (typical source capability:3 mA shared between these IOs, but sink capability is same as other IO), the speed of GPIOs PC13 to PC15 should not exceed 2 MHz when they are in output mode (maximum load: 30 pF).

Table 4-31. I/O port AC characteristics(1)(2)(3)(4)

Speed	Symbol	Description	Conditions	Max	Unit
00	t_R/t_F	Output high to low level fall time and output low to high level rise time	2.7 V ≤ V_{DD} ≤ 3.63 V, C_L = 10 pF	8	ns
			2.7 V ≤ V_{DD} ≤ 3.63 V, C_L = 30 pF	17	
			2.7 V ≤ V_{DD} ≤ 3.63 V, C_L = 50 pF	27	
01	t_R/t_F	Output high to low level fall time and output low to high level rise	2.7 V ≤ V_{DD} ≤ 3.63 V, C_L = 10 pF	2.5	ns

Speed	Symbol	Description	Conditions	Max	Unit
		time	2.7 V ≤ V_{DD} ≤ 3.63 V, C_L = 30 pF	5	
			2.7 V ≤ V_{DD} ≤ 3.63 V, C_L = 50 pF	7	
10	t_R/t_F	Output high to low level fall time and output low to high level rise time	2.7 V ≤ V_{DD} ≤ 3.63 V, C_L = 10 pF	2	ns
			2.7 V ≤ V_{DD} ≤ 3.63 V, C_L = 30 pF	3.5	
			2.7 V ≤ V_{DD} ≤ 3.63 V, C_L = 50 pF	5	
11	t_R/t_F	Output high to low level fall time and output low to high level rise time	2.7 V ≤ V_{DD} ≤ 3.63 V, C_L = 10 pF	1	ns
			2.7 V ≤ V_{DD} ≤ 3.63 V, C_L = 30 pF	2.2	
			2.7 V ≤ V_{DD} ≤ 3.63 V, C_L = 50 pF	4	

(1) The maximum frequency is defined with the following conditions: (t_R+t_F) ≤ 2/3 T Skew ≤ 1/20 T 45% < Duty cycle < 55%.

(2) The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.

(3) Value guaranteed by design, not 100% tested in production.

(4) The data is for reference only, and the specific values are related to PCB Layout.

4.16. Internal reference voltage characteristics

Table 4-32. Internal reference voltage characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	T_A = -40°C ~ +85 °C	1.19	1.2	1.21	V
$t_{S\_VREFINT}$	ADC sampling time when reading the internal reference voltage	—	13.7	—	—	μs
$t_{STA\_VREFINT}$	Start time of reference voltage buffer when ADC is enable	—	—	4	6	μs
$I_{DD(VREFINT\_BUF)}$	V_{REFINT} buffer consumption from V_{DD} when converted by ADC	—	—	4.5	5.5	μA
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	—	—	25	70	mV

(1) Value guaranteed by design, not 100% tested in production.

(2) The shortest sampling time can be determined in the application by multiple iterations.

Table 4-33. Internal reference voltage calibration values

Symbol	Test conditions	Memory address (2)
V_{REFINT}(1)	V_{DD} = V_{DDA} = V_{REFP} = 3.3 V (± 10 mV), Temperature = 25 °C (± 5 °C)	Secure boundary address: 0x5002 290A - 0x5002 290B Non-Secure boundary address: 0x4002 290A - 0x4002 290B

(1) V_{REFINT} is internally connected to the ADC_IN10 input channel.

(2) The calibration value is read from EFUSE register, which needs to be read in 32 bits, so the register needs to be read from 0x5002 2908 or 0x4002 2908, and the actual calibration values is stored in register's high 16 bits (0x5002 290A - 0x5002 290B or 0x4002 290A - 0x4002 290B).

4.17. ADC characteristics

Table 4-34. ADC characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage	—	2.7	3.3	3.6	V
V_{REFP}(2)	Positive Reference Voltage	—	—	—	V_{DDA}	V
f_{ADC}	ADC clock	—	0.1	—	35	MHz
V_{AIN}	Analog input voltage	12 external; 3 internal	0	—	V_{REFP}	V
R_{AIN}	External input impedance	See ***Equation 1***	—	—	440.7	kΩ
R_{ADC}	Input sampling switch resistance	—	—	—	0.5	kΩ
C_{ADC}	Input sampling capacitance	No pin/pad capacitance included	—	—	2.9	pF
t_S	Sampling time	f_{ADC} = 35 MHz	0.04	—	13.7	μs
t_{CONV}	Total conversion time(including sampling time)	12-bit	—	14	—	1/ f_{ADC}
f_S	Sampling rate	12-bit	0.007	—	2.5	MSPS
$t_{ST(ADC)}$	Startup time	—	—	—	1	μs

(1) Value guaranteed by design, not 100% tested in production.

(2) V_{REFP}/V_{DDA} should always be equal to or less than V_{DD}, especially during power up.

Equation 1: R_{AIN} max formula $$R_{AIN} < \frac{T_S}{f_{ADC} * C_{ADC} * \ln(2^{N+2})} - R_{ADC}$$

The formula above (Equation 1) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 4-35. ADC $R_{AIN\ max}$ for f_{ADC} = 35 MHz(1)(2)

T_s (cycles)	t_s (μs)	$R_{AIN\ max}$ (kΩ)
1.5	0.04	0.88
14.5	0.41	12.84
27.5	0.79	24.80
55.5	1.59	50.57

T_s (cycles)	t_s (μs)	$R_{AIN\ max}$ (kΩ)
83.5	2.39	76.33
111.5	3.19	102.1
143.5	4.10	131.5
479.5	13.7	440.7

(1) Value guaranteed by design, not 100% tested in production.

(2) The R_{AIN} value was calculated by theory and stray capacitance of actual PCB has not been taken into account.

Table 4-36. ADC accurary characteristics(1)(2)(3)(4)(5)

Symbol	Description	Conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 35 MHz, V_{DDA} = 3.3 V, Input Frequency = 20 kHz, Temperature = 25°C	—	10.7	—	bits
SNDR	Signal-to-noise and distortion ratio		—	66.6	—	dB
SNR	Signal-to-noise ratio		—	67	—	
THD	Total harmonic distortion		—	-77	—	
Offset	Offset error	f_{ADC} = 35 MHz, V_{DDA} = 3.3 V Temperature = 25°C	—	±1	—	LSB
DNL	Differential linearity error		—	±1	—	
INL	Integral linearity error		—	±1.2	—	

(1) Value guaranteed by sample, not 100% tested in production.

(2) Some guidance is provided to improve the sampling accuracy of ADC. Refer to AN059 Methods to improve ADC sampling accuracy.

(3) Results for BGA64 packages. The values for other packages might differ.

(4) V_{DD} = V_{DDA} = V_{REFP} = 3.3V, external V_{REFP} were adopted.

(5) System clock = 140MHz, PCLK2 = 70MHz, System clock from HXTAL, ADC_CLK from PCLK2.

4.18. V_{BAT} monitoring characteristics

Table 4-37. V_{BAT} monitoring characteristics

Symbol	Description	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	—	50	—	kΩ
Q	Ratio on V_{BAT} measurement	—	4	—	—
Er(1)	Error on Q	-10	—	10	%
t_{S_Vbat}(1)	ADC sampling time when reading the V_{BAT}	—	13.7	—	μs

(1) Value guaranteed by design, not 100% tested in production.

4.19. Temperature sensor characteristics

Table 4-38. Temperature sensor characteristics (1)

Symbol	Description	Min	Typ	Max	Unit
T_L	V_{SENSE} linearity with temperature	—	±2	—	°C
Avg_Slope	Average slope	—	4.179	—	mV/°C
V_{25}	Uncalibrated Voltage at 25 °C	—	1.491	—	V
t_{START}	Startup time	—	8	—	μs

Symbol	Description	Min	Typ	Max	Unit
t_{S_temp}(2)	ADC sampling time when reading the temperature	—	13.7	—	µs

(1) Value guaranteed by design, not 100% tested in production.

(2) Shortest sampling time can be determined in the application by multiple iterations.

Table 4-39. Temperature sensor calibration values

Symbol	Description	Memory address (1)
TS_CAL1	Temperature sensor raw data acquired value at 30 °C (± 3 °C), V_{DD} = V_{DDA} = V_{REFP} = 3.3V (± 3.65 mV)	Secure boundary address: 0x5002 2930 - 0x5002 2931 Non-Secure boundary address: 0x4002 2930 - 0x 4002 2931

(1) The calibration value is read from EFUSE register, which needs to be read in 32 bits, so the register needs to be read from 0x5002 2930 or 0x4002 2930, and the actual calibration values is stored in register's low 12bits.

4.20. I2C characteristics

The I2C interface meets the requirements of the standard I2C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not "true" open drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

Refer also to ***Section 4.15 GPIO characteristics*** for more details on the input/output alternate function characteristics (SDA and SCL).

Table 4-40. I2C characteristics(1)(2)

Symbol	Description	Conditions	Standard mode		Fast mode		Fast mode plus		Unit
			Min	Max	Min	Max	Min	Max	
$t_{SCL(H)}$	SCL clock high time	—	4.0	—	0.6	—	0.2	—	µs
$t_{SCL(L)}$	SCL clock low time	—	4.7	—	1.3	—	0.5	—	µs
$t_{su(SDA)}$	SDA setup time	—	250	—	100	—	50	—	ns
$t_{h(SDA)}$	SDA data hold time	—	0(3)	3450	0	900	0	450	ns
$t_{r(SDA/SCL)}$	SDA and SCL rise time	—	—	1000	—	300	—	120	ns
$t_{f(SDA/SCL)}$	SDA and SCL fall time	—	—	300	3(4)(5)	300	3(4)(6)	120	ns
$t_{h(STA)}$	Start condition hold time	—	4.0	—	0.6	—	0.26	—	µs
$t_{su(STA)}$	Repeated Start	—	4.7	—	0.6	—	0.26	—	µs

Symbol	Description	Conditions	Standard mode		Fast mode		Fast mode plus		Unit
			Min	Max	Min	Max	Min	Max	
	condition setup time								
$t_{su(STO)}$	Stop condition setup time	—	4.0	—	0.6	—	0.26	—	μs
t_{BUFF}	Stop to Start condition time (bus free)	—	4.7	—	1.3	—	0.5	—	μs

(1) Value guaranteed by design, not 100% tested in production.

(2) To ensure the standard mode I2C frequency, f_{PCLK1} must be at least 2 MHz. To ensure the fast mode I2C frequency, f_{PCLK1} must be at least 4 MHz. To ensure the fast mode plus I2C frequency, f_{PCLK1} must be at least a multiple of 10 MHz.

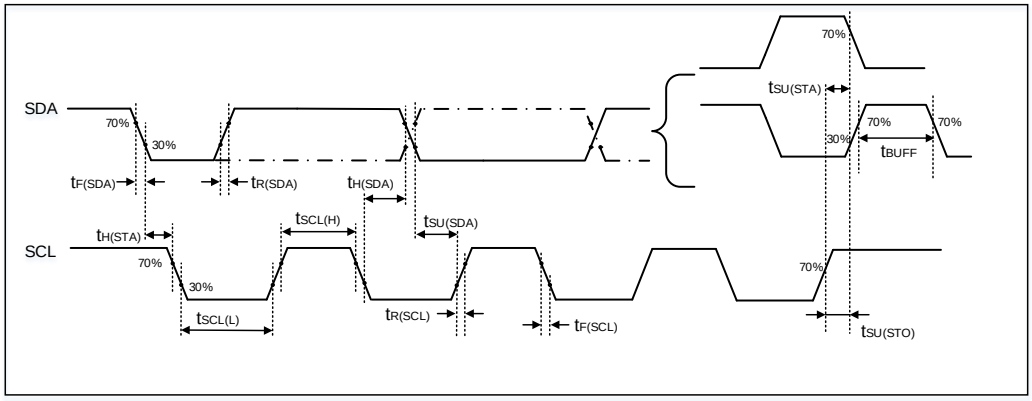
(3) The device should provide a data hold time of 300 ns at least in order to bridge the undefined region of the falling edge of SCL.

(4) Value guaranteed by characterization, not 100% tested in production.

(5) In the condition of I2C frequency = 400 kHz, IO_Speed = 166 MHz and Pull-up resistor = 1 kΩ.

(6) In the condition of I2C frequency = 1 MHz, IO_Speed = 166 MHz and Pull-up resistor = 1 kΩ.

Figure 4-7. I2C bus timing diagram



4.21. SPI characteristics

Refer to ***Section 4.15 GPIO characteristics*** for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 4-41. Standard SPI characteristics(1)(2)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	—	—	—	22.5	MHz
$t_{SCK(H)}$	SCK clock high time	Master mode, f_{SCK} = 22.5 MHz	—	22.22	—	ns
$t_{SCK(L)}$	SCK clock low time	Master mode, f_{SCK} = 22.5 MHz	—	22.22	—	ns
SPI master mode						

Symbol	Description	Conditions	Min	Typ	Max	Unit
$t_{V(MO)}$	Data output valid time	—	—	—	7	ns
$t_{SU(MI)}$	Data input setup time	—	3	—	—	ns
$t_{H(MI)}$	Data input hold time	—	0	—	—	ns
SPI slave mode						
$t_{SU(NSS)}$	NSS enable setup time	—	0	—	—	ns
$t_{H(NSS)}$	NSS enable hold time	—	3	—	—	ns
$t_{A(SO)}$	Data output access time	—	—	6	—	ns
$t_{DIS(SO)}$	Data output disable time	—	—	9	—	ns
$t_{V(SO)}$	Data output valid time	—	—	8	—	ns
$t_{SU(SI)}$	Data input setup time	—	0	—	—	ns
$t_{H(SI)}$	Data input hold time	—	2	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

(2) Output speed is set to OSPDy[1:0] = 10.

Figure 4-8. SPI timing diagram - master mode

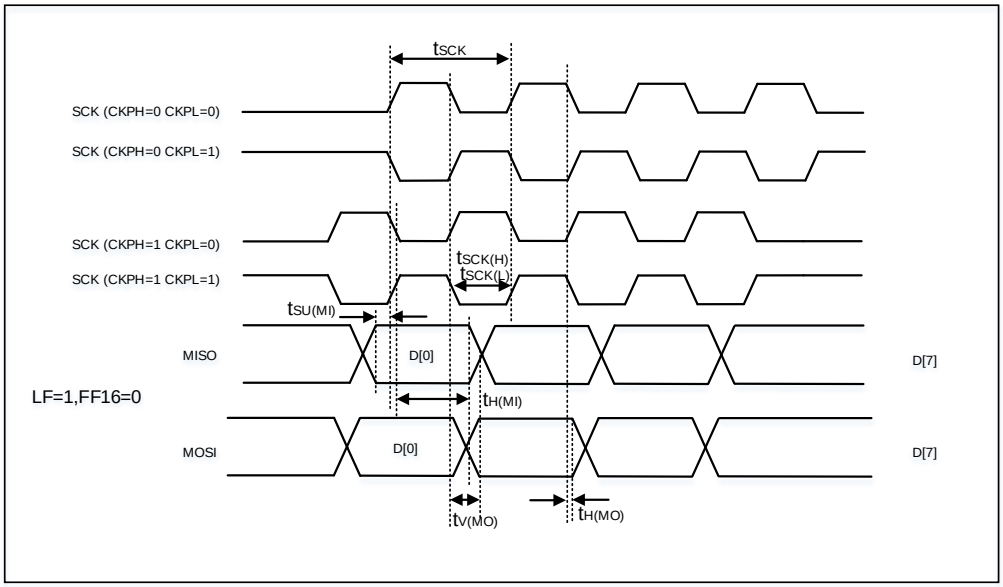


Figure 4-9. SPI timing diagram - slave mode (CKPH=0)

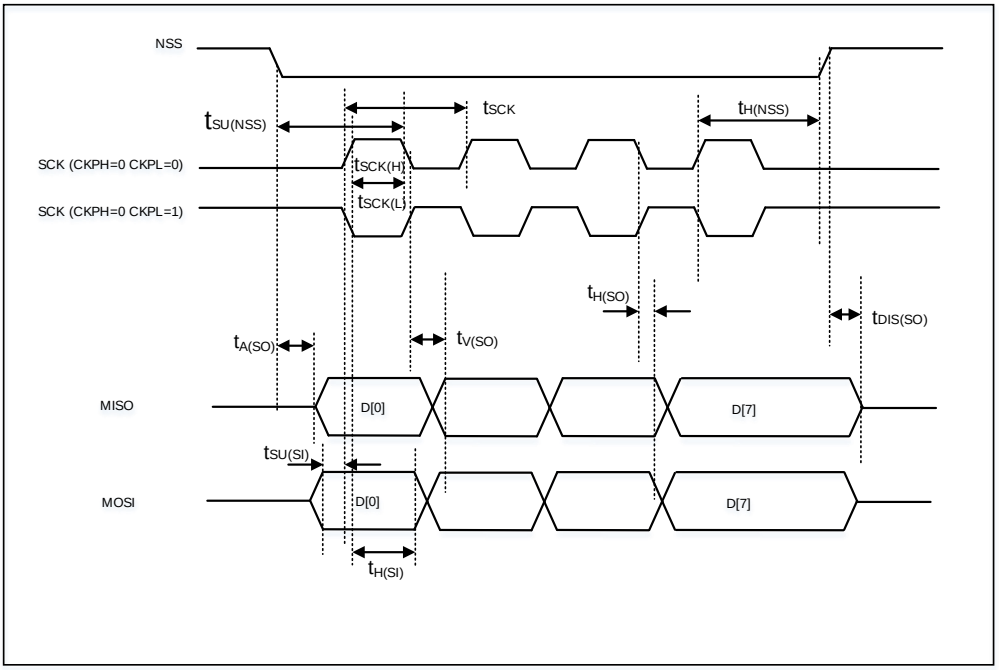
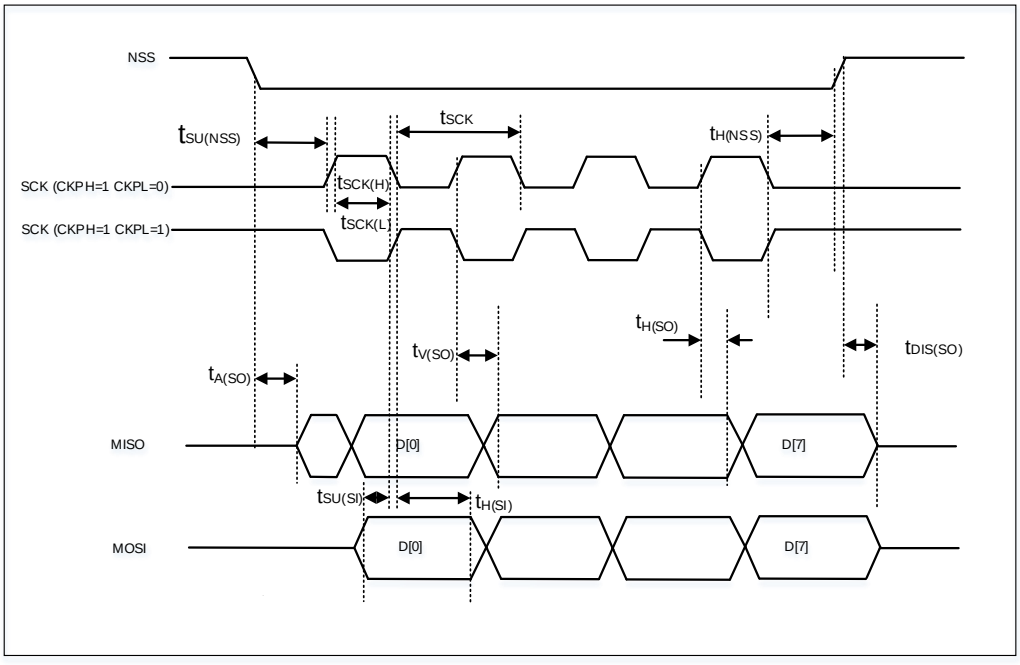


Figure 4-10. SPI timing diagram - slave mode(CKPH=1)



4.22. QSPI characteristics

Table 4-42. Standard QSPI characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	—	—	—	45	MHz
$t_{SCK(H)}$	SCK clock high time, even division	—	$t_{(SCK)}/2$	—	$t_{(SCK)}/2+1$	ns
	SCK clock low time, even division	—	$(n/2)*t_{(SCK)}/(n+1)$	—	$(n/2)*t_{(SCK)}/(n+1)+1$	ns
$t_{SCK(L)}$	SCK clock high time, even division	—	$t_{(SCK)}/2–1$	—	$t_{(SCK)}/2$	ns
	SCK clock low time, even division	—	$(n/2+1)*t_{(SCK)}/(n+1)–1$	—	$(n/2+1)*t_{(SCK)}/(n+1)$	ns
$t_{V(MO)}$	Data output valid time	—	—	4	6	ns
$t_{H(MO)}$	Data output hold time	—	2	—	—	ns
$t_{SU(MI)}$	Data input setup time	—	5	—	—	ns
$t_{H(MI)}$	Data input hold time	—	3	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

4.23. SQPI characteristics

Refer to *Section 4.15 GPIO characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 4-43. SQPI characteristics(1)

Symbol	Description	Min	Typ	Max	Unit
t_{CLK}	CLK period	11.0(3)	—	—	ns
t_{CD}	CLK high level duty for even clock divided	45	50	55	%
	CLK high level duty for odd clock divided	45	—	71	
t_{KHKL}(2)	CLK rise or fall time	—	2.0	—	ns
t_{CPH}	CE# high between subsequent burst operations	22.2	—	—	ns
t_{CEM}	CE# low pulse width	88.8	—	—	ns
t_{CSP}	CE# setup time to CLK rising edge	5.5	—	177.7	ns
t_{CHD}	CE# hold time from CLK rising edge	5.5	—	177.7	ns
t_{SP}	Setup time to active CLK edge	5.5	—	177.7	ns
t_{HD}	Hold time from active CLK edge	5.5	—	177.7	ns
t_{HZ}	CE# rise to data output high-Z	—	0	—	ns
t_{ACLK}	CLK fall to data output valid delay	—	0	—	ns
t_{KOH}	Data hold time from CLK falling edge	—	0	—	ns

(1) Value guaranteed by design, not 100% tested in production.

(2) Output driven mode is 166 MHz. Measured from 10% to 90% of V_{DD}.

(3) This is designed minimal period. The operating minimal clock period is 22.2 ns (45 MHz = 180 MHz / 4).

4.24. I2S characteristics

Refer to *Section 4.15 GPIO characteristics* for more details on the input/output alternate function characteristics (CK, SD, WS).

Table 4-44. I2S characteristics(1)(2)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{CK}	Clock frequency	Master mode (data: 32 bits, Audio frequency = 96 kHz	—	6.25	—	MHz
		Slave mode	—	—	12.5(3)	
t_H	Clock high time	—	—	81	—	ns
t_L	Clock low time		—	81	—	ns
$t_{V(WS)}$	WS valid time	Master mode	—	3	—	ns
$t_{H(WS)}$	WS hold time	Master mode	—	3	—	ns
$t_{SU(WS)}$	WS setup time	Slave mode	0	—	—	ns
$t_{H(WS)}$	WS hold time	Slave mode	3	—	—	ns
$Duty_{SCK}$	I2S slave input clock duty cycle	Slave mode	—	50	—	%
$t_{SU(SD\_MR)}$	Data input setup time	Master mode	3	—	—	ns
$t_{SU(SD\_SR)}$	Data input setup time	Slave mode	0	—	—	ns
$t_{H(SD\_MR)}$	Data input hold time	Master receiver	0	—	—	ns
$t_{H(SD\_SR)}$		Slave receiver	3	—	—	ns
$t_{V(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	—	—	8	ns
$t_{H(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	3	—	—	ns
$t_{V(SD\_MT)}$	Data output valid time	Master transmitter (after enable edge)	—	—	7	ns
$t_{H(SD\_MT)}$	Data output hold time	Master transmitter (after enable edge)	0	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

(2) Output speed is set to OSPDy[1:0] = 10.

(3) In the slave receiving mode, if it is not the Philips standard or CHLEN=1, the maximum audio sampling frequency can reach 192kHz.

Figure 4-11. I2S timing diagram - master mode

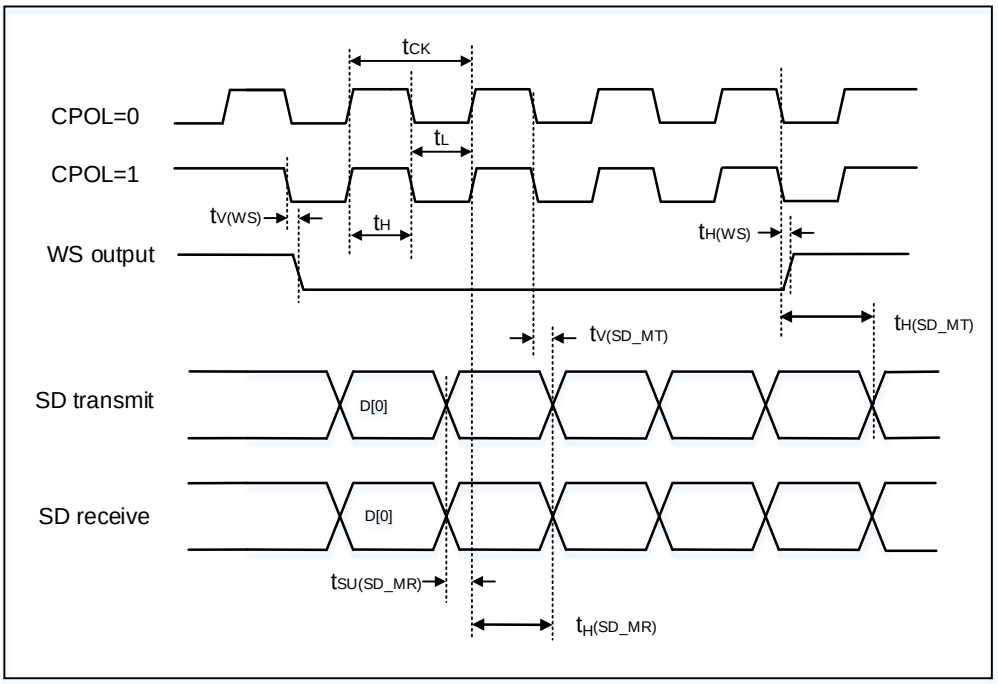
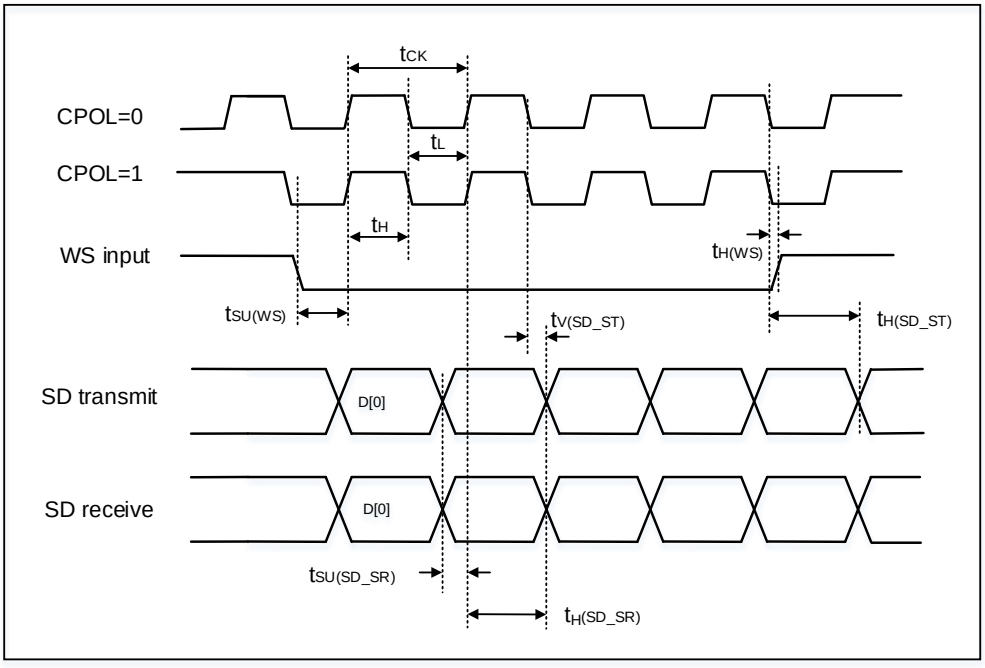


Figure 4-12. I2S timing diagram - slave mode



4.25. USART characteristics

Refer to ***Section 4.15 GPIO characteristics*** for more details on the input/output alternate function characteristics (NSS, CK, TX, and RX for USART).

Table 4-45. USART0/2 characteristics in Synchronous mode (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	CK_SYS= 200 MHz	—	—	25	MHz
$t_{SCK(H)}$	SCK clock high time	CK_SYS = 200 MHz	20	—	—	ns
$t_{SCK(L)}$	SCK clock low time	CK_SYS = 200 MHz	20	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

(2) The clock source can be selected through register configuration, which can be chosen as CK_APB1, CK_SYS, CK_LXTAL or CK_IRC16M.

Table 4-46. USART0/2 characteristics in Smartcard mode (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	CK_SYS = 200 MHz	—	—	100	MHz
$t_{SCK(H)}$	SCK clock high time	CK_SYS = 200 MHz	5	—	—	ns
$t_{SCK(L)}$	SCK clock low time	CK_SYS = 200 MHz	5	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

(2) The clock source can be selected through register configuration, which can be chosen as CK_APB1, CK_SYS, CK_LXTAL or CK_IRC16M

4.26. USBFS characteristics

Table 4-47. USBFS start up time

Symbol	Description	Max	Unit
$t_{STARTUP}$(1)	USBFS startup time	1	μs

(1) Value guaranteed by design, not 100% tested in production.

Table 4-48. USBFS DC electrical characteristics (1)

Symbol		Description	Conditions	Min	Typ	Max	Unit
V_{DD}		USBFS operating voltage	—	3	—	3.6	V
Input levels	V_{DI}	Differential input sensitivity	—	0.2	—	—	
	V_{CM}	Differential common mode range	Includes V_{DI} range	0.8	—	2.5	
	V_{SE}	Single ended receiver threshold	—	0.8	—	2.0	
Output levels	V_{OL}	Static output level low	R_L of 1.5 kΩ to V_{DD}	—	0.031	0.3	V
	V_{OH}	Static output level high	R_L of 21 kΩ to GND	2.8	3.29	3.6	
R_{PD}		PB13, PB12(USBFS_DM/DP)	V_{IN} = V_{DD}	16.36	21	24.19	kΩ
		PB14(USBFS_VBUS)		0.58	—	1.13	
R_{PU}		PB13, PB12(USBFS_DM/DP)	V_{IN} = GND	0.78	1.59	1.85	
		PB14(USBFS_VBUS)		0.3	—	0.43	

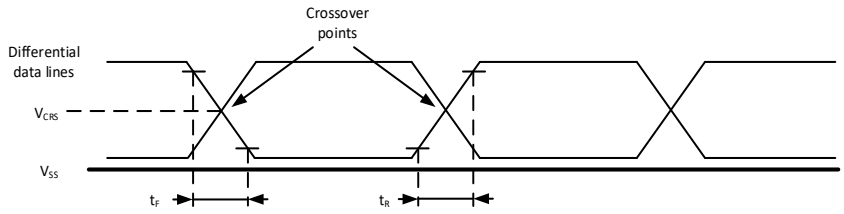
(1) Value guaranteed by design, not 100% tested in production.

Table 4-49. USBFS full speed-electrical characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
t_R	Rise time	CL = 50 pF	4	—	20	ns
t_F	Fall time	CL = 50 pF	4	—	20	ns
t_{RFM}	Rise / fall time matching	t_R / t_F	90	—	110	%
v_{CRS}	Output signal crossover voltage	—	1.3	—	2.0	V

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-13. USBFS timings: definition of data signal rise and fall time



4.27. TIMER characteristics

Table 4-50. TIMER characteristics (1)

Symbol	Description	Conditions	Min	Max	Unit
t_{res}	Timer resolution time	—	1	—	t_{CK_TIMERx}
		f_{CK_TIMERx} = 200 MHz	5	—	ns
f_{EXT}	Timer external clock frequency	—	0	$f_{CK\_TIMERx}/2$	MHz
		f_{CK_TIMERx} = 200 MHz	0	100	MHz
RES	Timer resolution	TIMERx except (TIMER1& TIMER2)	—	16	bit
		TIMER1& TIMER2	—	32	
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	—	1	65536	t_{CK_TIMERx}
		f_{CK_TIMERx} = 200 MHz	0.005	327.68	μs
	32-bit counter clock period when internal clock is selected	—	1	65536x65536	t_{CK_TIMERx}
		f_{CK_TIMERx} = 200 MHz	—	21.47	s
t_{MAX_COUNT}	Maximum possible count (16-bit)	—	—	65536x65536	t_{CK_TIMERx}
		f_{CK_TIMERx} = 200 MHz	—	21.47	s
	Maximum possible count (32-bit)	—	—	65536x65536x65536	t_{CK_TIMERx}
		f_{CK_TIMERx} = 200 MHz	—	1407374.9	s

(1) Value guaranteed by design, not 100% tested in production.

4.28. WDGT characteristics

Table 4-51. FWDGT min/max timeout period at 32 kHz (IRC32K) (1)

Prescaler divider	PSC[2:0] bits	Min timeout RLD[11:0] =0x000	Max timeout RLD[11:0] = 0xFFF	Unit
1/4	000	0.125	512	ms
1/8	001	0.25	1024	

Prescaler divider	PSC[2:0] bits	Min timeout RLD[11:0] =0x000	Max timeout RLD[11:0] = 0xFFF	Unit
1/16	010	0.5	2048	
1/32	011	1.0	4096	
1/64	100	2.0	8192	
1/128	101	4.0	16384	
1/256	110 或 111	8.0	32768	

(1) Value guaranteed by design, not 100% tested in production.

Table 4-52. WWDGT min-max timeout value at 50 MHz (f_{PCLK1}) (1)

Prescaler divider	PSC[2:0]	Min timeout value CNT[6:0] = 0x40	Unit	Max timeout value CNT[6:0] = 0x7F	Unit
1/1	00	81.92	us	5.24	ms
1/2	01	163.84		10.49	
1/4	10	327.68		20.97	
1/8	11	655.36		41.94	

(1) Value guaranteed by design, not 100% tested in production.

5. Package information

5.1. BGA64(4x4) package outline dimensions

Figure 5-1. BGA64(4x4) package outline

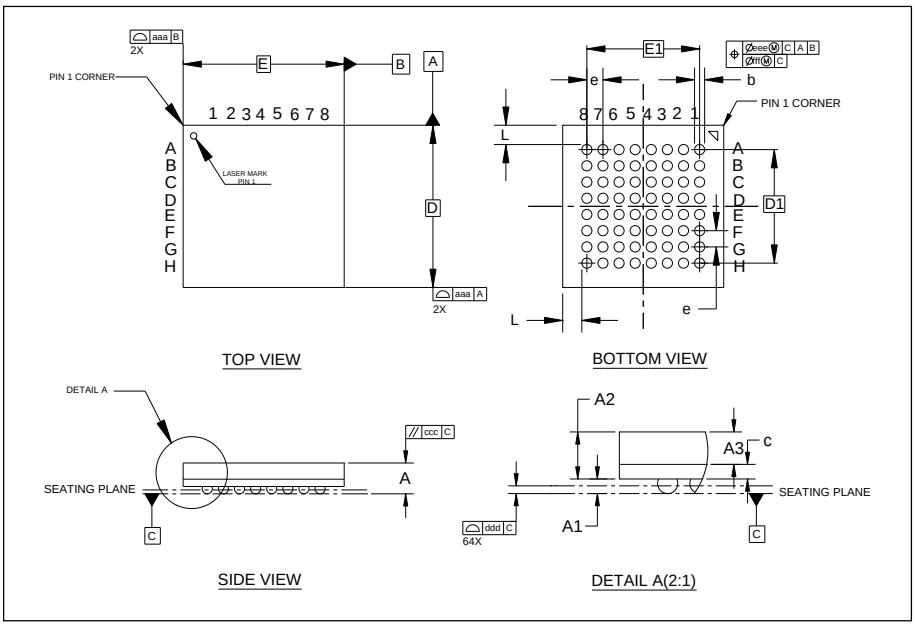
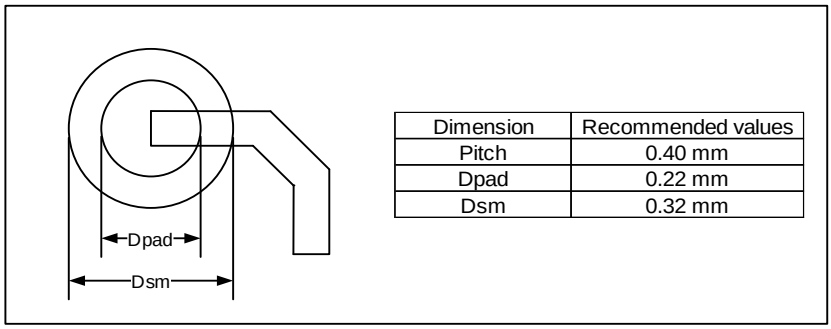


Table 5-1. BGA64(4x4) package dimensions

Symbol	Min	Typ	Max
A	0.68	0.76	0.84
A1	0.13	0.18	0.23
A2	0.53	0.58	0.63
A3	—	0.40	—
b	0.20	0.25	0.30
c	0.15	0.18	0.21
D	3.90	4.00	4.10
D1	—	2.80	—
E	3.90	4.00	4.10
E1	—	2.80	—
e	—	0.40	—
L	—	0.475	—
aaa	—	0.10	—
ccc	—	0.10	—
ddd	—	0.08	—
eee	—	0.15	—
fff	—	0.05	—

(Original dimensions are in millimeters)

Figure 5-2. BGA64(4x4) recommended footprint



Dimension	Recommended values
Pitch	0.40 mm
Dpad	0.22 mm
Dsm	0.32 mm

(Original dimensions are in millimeters)

5.2. QFN56 package outline dimensions

Figure 5-3. QFN56 package outline

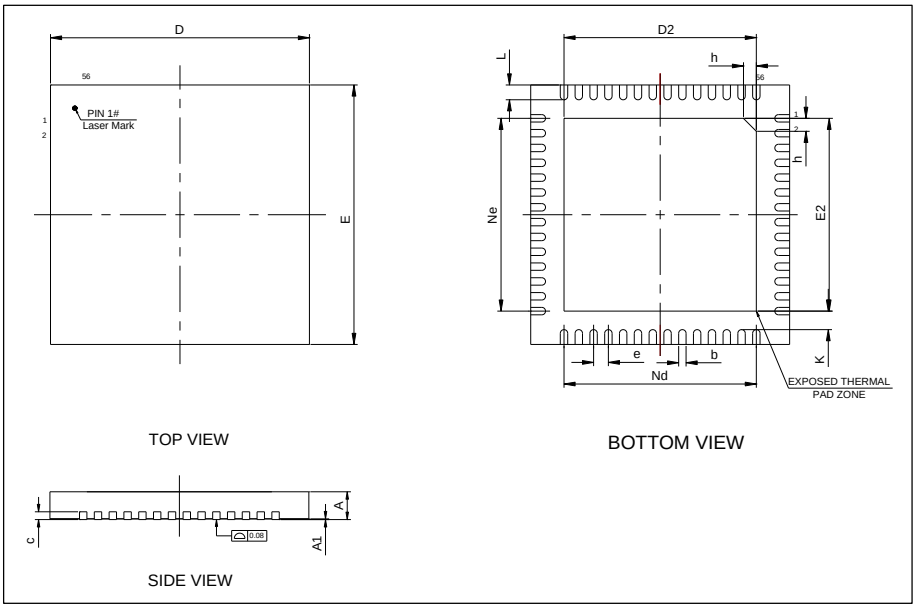
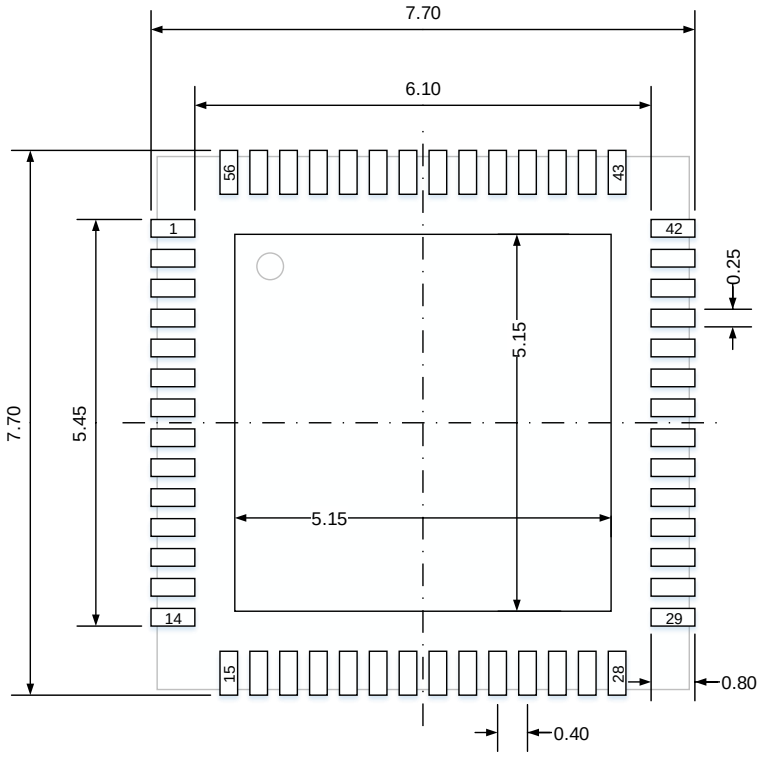


Table 5-2. QFN56 package dimensions

Symbol	Min	Typ	Max
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	—	0.20	—
D	6.90	7.00	7.10
D2	5.10	5.20	5.30
E	6.90	7.00	7.10
E2	5.10	5.20	5.30
e	0.30	0.40	0.50
h	—	0.35	—
K	—	0.50	—
L	0.35	0.40	0.45
Nd	—	5.20	—
Ne	—	5.20	—

(Original dimensions are in millimeters)

Figure 5-4. QFN56 recommended footprint



(Original dimensions are in millimeters)

5.3. Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter "θ". For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

θ_{JA}: Thermal resistance, junction-to-ambient.

θ_{JB}: Thermal resistance, junction-to-board.

θ_{JC}: Thermal resistance, junction-to-case.

Ψ_{JB}: Thermal characterization parameter, junction-to-board.

Ψ_{JT}: Thermal characterization parameter, junction-to-top center.

$$\theta_{JA}=(T_J-T_A)/P_D \quad (5\text{-}1)$$

$$\theta_{JB}=(T_J-T_B)/P_D \quad (5\text{-}2)$$

$$\theta_{JC}=(T_J-T_C)/P_D \quad (5\text{-}3)$$

Where, T_J = Junction temperature.

T_A = Ambient temperature

T_B = Board temperature

T_C = Case temperature which is monitoring on package surface

P_D = Total power dissipation

θ_{JA} represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower θ_{JA} can be considerate as better overall thermal performance.

θ_{JB} is used to measure the heat flow resistance between the chip surface and the PCB board.

θ_{JC} represents the thermal resistance between the chip surface and the package top case. θ_{JC} is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

Table 5-3. Package thermal characteristics(1)

Symbol	Condition	Package	Value	Unit
θ_{JA}	Natural convection, 2S2P PCB	BGA64(4x4)	71.93	°C/W
		QFN56	38.32	
θ_{JB}	Cold plate, 2S2P PCB	BGA64(4x4)	40.82	°C/W
		QFN56	17.23	
θ_{JC}	Cold plate, 2S2P PCB	BGA64(4x4)	19.95	°C/W
		QFN56	13.28	

Symbol	Condition	Package	Value	Unit
Ψ_{JB}	Natural convection, 2S2P PCB	BGA64(4x4)	40.72	°C/W
		QFN56	17.48	
Ψ_{JT}	Natural convection, 2S2P PCB	BGA64(4x4)	1.17	°C/W
		QFN56	2.90	

(1) Thermal characteristics are based on simulation, and meet JEDEC specification.

6. Ordering information

Table 6-1. Part ordering code for GD32F5HCxx devices

Ordering code	Flash (KB)	Package	Package type	Temperature operating range
GD32F5HCRIL6	2048	BGA64(4x4)	Green	Industrial -40 °C to +85 °C
GD32F5HCPIQ6	2048	QFN56	Green	Industrial -40 °C to +85 °C
GD32F5HCPIQ7	2048	QFN56	Green	Industrial -40 °C to +105 °C

7. Revision history

Table 7-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Apr. 15, 2026

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