GigaDevice Semiconductor Inc.

GD32A711,GD32A712
Arm® Cortex®-M7 32-bit MCU

Datasheet

Revision 1.2

(Sep. 2026)

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1. General description

The GD32A711/A712 device belongs to the high performance line of GD32 MCU family. It is a new 32-bit general-purpose microcontroller based on the Arm® Cortex®-M7 core with best cost-performance ratio in terms of enhanced processing capacity, reduced power consumption and peripheral set. The Arm® Cortex®-M7 processor is a highly efficient high-performance, embedded processor that features low interrupt latency, low-cost debug, and has backwards compatibility with existing Cortex-M profile processors. The processor has an in-order super-scalar pipeline that means many instructions can be dual-issued, including load/load and load/store instruction pairs because of multiple memory interfaces. The Cortex-M7 is a high-performance processor, which features a 6-stage superscalar pipeline with branch prediction and an optional FPU capable of single-precision and optionally double-precision operations. The instruction and data buses have been enlarged to 64-bit wide over the previous 32-bit buses. It also provides a Memory Protection Unit (MPU) and powerful trace technology for enhanced application security and advanced debug support.

The GD32A711/A712 device incorporates the Arm® Cortex®-M7 32-bit processor core operating at 160MHz(120MHz) frequency with Flash security protection to prevent illegal code/data access, and additionally, it includes one Cortex®-M7 core and a Cortex®-M23 core HSM module, aligning with ISO26262 ASIL-B functional safety and Evita-full+SM2/3/4 security standards, thereby enhancing frequency, efficiency and security level. It provides up to 2048 KB on-chip main flash memory. The devices offer up to two ADCs, two DAC, two comparators, up to two general 16-bit timers, eight 16-bit advanced timers, and two 32-bit basic timers, as well as standard and advanced communication interfaces: up to six SPIs, two I2Cs, two I2Ss, eight DTM_CANs, six LINFlexDs(support UART mode). Additional peripherals as interrupt requests management (IRM), hardware security module (HSM), self-test control module (STCM), memory test controller (MTC), fault management unit (FMU) are included.

The device operates from a 2.97V to 5.5V power supply and available in -40 to +125 °C temperature range. One power saving mode provides the flexibility for maximum optimization of power consumption, an especially important consideration in low power applications.

The above features make GD32A711/A712 devices suitable for a wide range of interconnection and advanced applications, especially in areas such as Lighting, IVI, T-BOX, BCM, HVAC, BMS and so on.



2. Device overview

2.1. Device information

Table 2-1. GD32A711/A712 devices features and peripheral list (120Mhz)

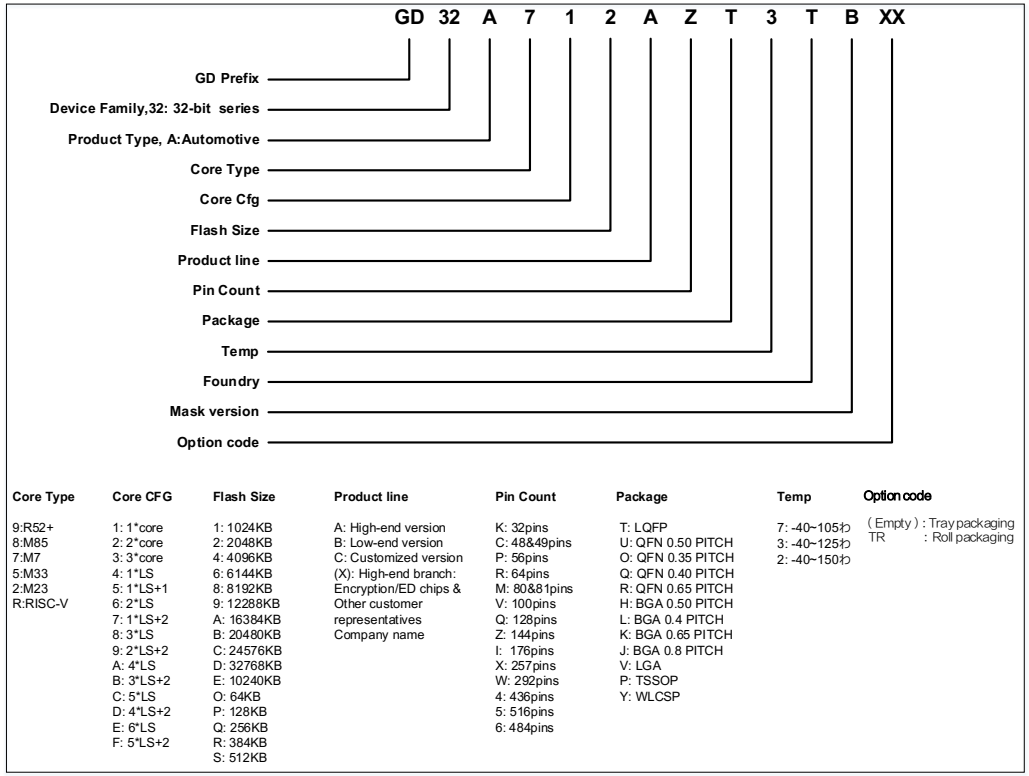
Part Number		GD32A711			GD32A712			
		BRT3TB	BVT3TB	BZT3TB	BPU3TB	BVT3TB	BZT3TB	BIT3TB
Safety-ISO 26262		ASIL-B						
Max Speed (MHz)		120						
Core Type		Cortex-M7						
Main FLASH (KB)		1024			2048			
Data-Flash (KB)		128+96						
SRAM (KB)	ITCM	32						
	DTCM	64						
	SRAM0	32			160			
	Total	128			256			
Timers	General timer	1*4		2*4	1*4		2*4	
	Advanced timer	8*8						
	Basic timer	2						
	SysTick	1						
	Watchdog	2						
	RTC	1						
Connectivity	I2C	2						
	SPI/I2S	4/1	6/2		5/2	6/2		
	QSPI	0	1		0	1		
	LINFlexD	6						
	M_CAN	5	6		5	6		
STCM		1						
MTC		1						
IRM		1						
HSM		1						
FMU		1						
DMA		2 * 8						
12bit ADC		ADC0: 15 ADC1: 12	ADC0: 20 ADC1: 20	ADC0: 20 ADC1: 24	ADC0: 13 ADC1: 9	ADC0: 20 ADC1: 20	ADC0:20 ADC1: 24	ADC0: 24 ADC1: 24
DAC Units		2						
CMP(1)		2						
GPIO		54	83	113	47	83	113	144
Package		LQFP64	LQFP100	LQFP144	QFN56	LQFP100	LQFP144	LQFP176

Table 2-2. GD32A711/A712 devices features and peripheral list (160MHz)

Part Number		GD32A711			GD32A712		
		ART3TB	AVT3TB	AZT3TB	AVT3TB	AZT3TB	AIT3TB
Safety-ISO 26262		ASIL-B					
Max Speed(MHz)		160					
Core Type		Cortex-M7					
Main FLASH (KB)		1024			2048		
Data-Flash(KB)		128+96					
SRAM (KB)	ITCM	32					
	DTCM	64					
	SRAM0	32			160		
	Total	128			256		
Timers	General timer	1 * 4		2 * 4	1 * 4	2 * 4	
	Advanced timer	8* 8					
	Basic timer	2					
	SysTick	1					
	Watchdog	2					
	RTC	1					
Connectivity	I2C	2					
	SPI/I2S	4/1	6/2				
	QSPI	0	1				
	LINFlexD	6					
	M_CAN	7	8				
STCM		1					
MTC		1					
IRM		1					
HSM		1					
FMU		1					
DMA		2 * 8					
12bit Channels		ADC0: 15 ADC1: 12	ADC0: 20 ADC1: 20	ADC0: 20 ADC1: 24	ADC0: 20 ADC1: 20	ADC0:20 ADC1: 24	ADC0: 24 ADC1: 24
DAC Units		2					
CMP[1]		2					
GPIO		54	83	113	83	113	144
Package		LQFP64	LQFP100	LQFP144	LQFP100	LQFP144	LQFP176

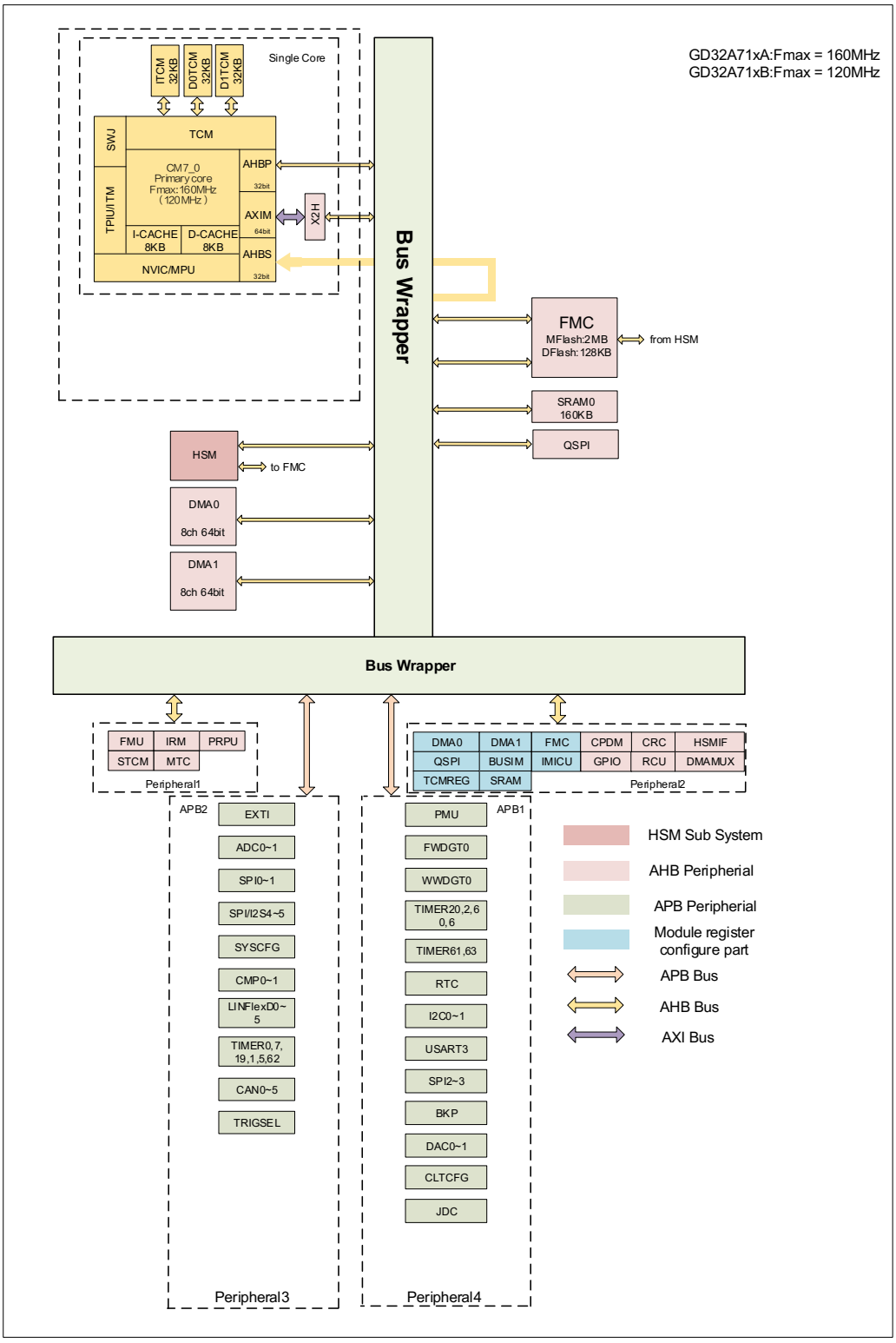
(1) The QFN56 encapsulates the CMP1_OUT pin PA13, which is also the SWD/JTAG pin. If the user configizes this pin as CMP_OUT after power-on, it will result in the inability to debug.For detailed information on pinouts and pin assignments, please refer to 2.3.

Figure 2-1. Part Number information



2.2. Block diagram

Figure 2-2. GD32A711/A712 block diagram



2.3. Pinouts and pin assignment

For detailed information on pinouts and pin assignments, please refer to the attachment "GD32A711_712_PinMux_Matrix" in the LQFP176_Pinouts sheet, LQFP144_Pinouts sheet, LQFP100_Pinouts sheet, LQFP64_Pinouts sheet or QFN56_Pinouts.

2.4. Clock tree

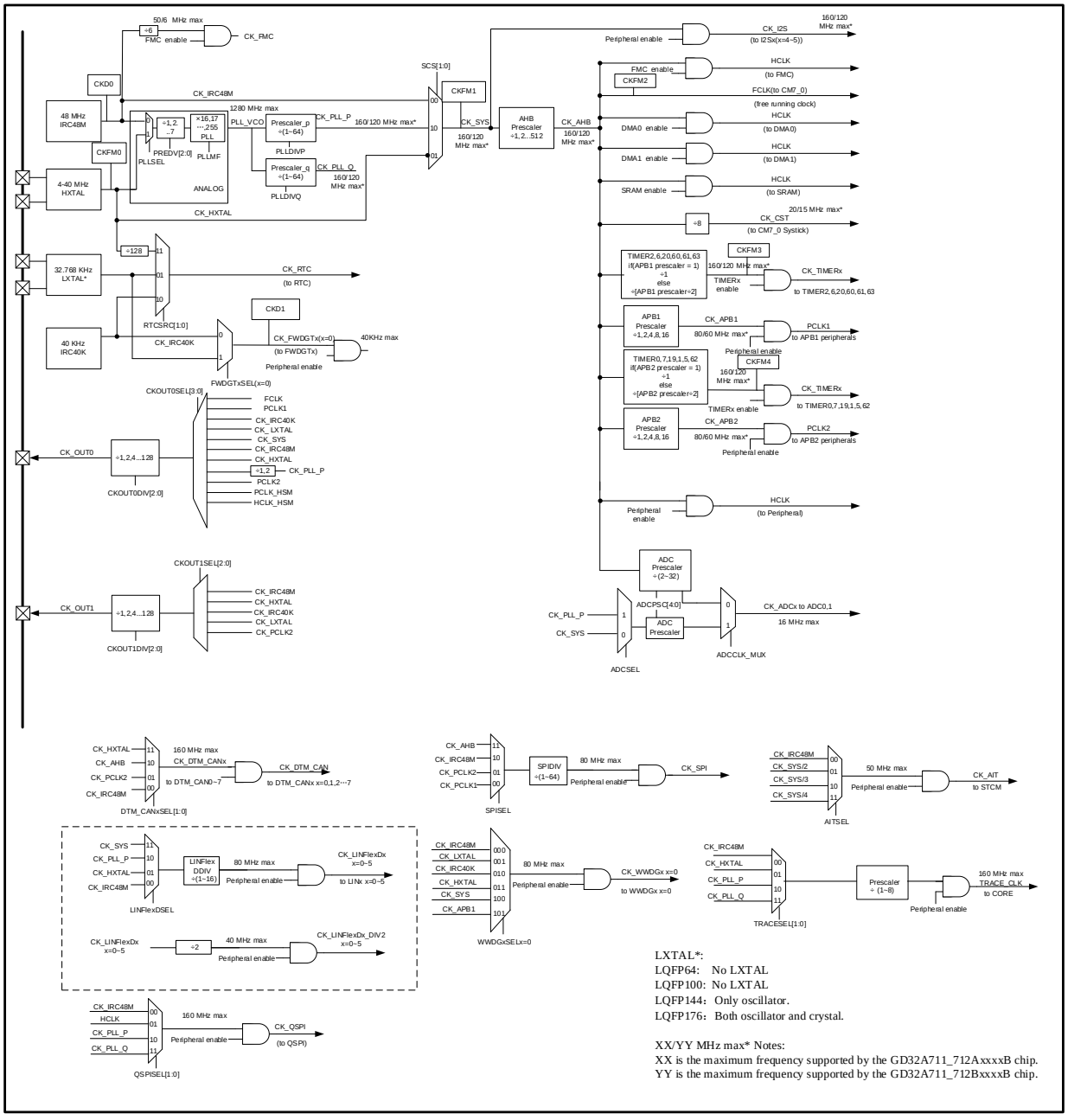


Figure 2-3. GD32A711/A712 clock tree

Notes:

HXTAL: High speed crystal oscillator

LXTAL: Low speed crystal oscillator

IRC40K: Internal 40K RC oscillator

IRC48M: Internal 48M RC oscillator

CK_OUT: By configuring the pin alternate functions, clock frequencies ranging from 32 KHz to 100 MHz can be output through the pins.

2.5. Pin definitions

For the Alternate function or additional functions of the GPIO, please refer to the attachment "GD32A711_712_PinMux_Matrix" in the PinMux sheet.

3. Electrical characteristics

3.1. Parameter introduction

- Parameter conditions: Unless otherwise specified, all values given for V_{DDA} = 5.0 V, T_A = 25°C, and all voltages are referenced to Vss.
- Value guaranteed by design, not 100% tested in production indicates that the value is derived from design or simulation and/or process characteristics.
- Value guaranteed by characterization, not 100% tested in production indicates that the value is derived from random test.
- Value guaranteed by sample, not 100% tested in production indicates that the value is derived from testing parameters with a small sample size.
- If the value is not specially indicated, it means the value guaranteed by 100% tested in production.

See the following table for some abbreviation terms and their descriptions in this chapter.

Table 3-1. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
CAN	Controller Area Network
DAC	Digital-to-Analog Converter
DMA	Direct Memory Access
GPIO	General Purpose Input/Output
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
SPI	Serial Peripheral Interface

3.2. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly over the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 3-2. Absolute maximum ratings (1)

Symbol	Description	Min	Max	Unit
V_{DDA}	Main I/O and analog supply voltage	-0.3	6(2)	V
V_{DD25}	Flash memory supply	-0.3	3.63	V
V_{11_RUN}	Core logic voltage supply	-0.3	1.26	V
V_{IN}	Input voltage on all I/O pins	-0.3	V_{DDA}+0.3	V
I_{IO}	Maximum current for GPIO pins	-	20	mA
$\sum I_{IO}$	Maximum current sink/sourced by all GPIO pin	-	100	
I_{INJ}	Injected current on each GPIO pin	-3	3	
$\sum I_{INJ}$	Total injected current on all GPIO pins	-	30	
T_{STG}	Storage temperature range	-55	150	°C
T_J	Maximum junction temperature	-40	150	°C

(2) Value guaranteed by design, not 100% tested in production.

(3) 6 V maximum for 10 hours over lifetime.

3.3. Operating conditions

Table 3-3. General operating conditions (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DDA}	Main I/O and analog supply voltage	-	2.97	3.3/5.0	5.5	V
V_{DD25}	Flash memory supply	-	-	2.53	-	V
V_{11_RUN}	Core logic voltage supply	-	-	1.14	-	V
f_{CPU}	Core clock frequency	GD32A711B/A712B	-	-	120	MHz
		GD32A711A/A712A	-	-	160	MHz
f_{HCLK}	AHB clock frequency	GD32A711B/A712B	-	-	120	MHz
f_{APB1}	APB1 clock frequency		-	-	60	MHz
f_{APB2}	APB2 clock frequency		-	-	60	MHz
f_{HCLK}	AHB clock frequency	GD32A711A/A712A	-	-	160	MHz
f_{APB1}	APB1 clock frequency		-	-	80	MHz
f_{APB2}	APB2 clock frequency		-	-	80	MHz
Vramp_slow	Supply ramp rate(slow)	-	0.5	-	-	V/min
Vramp_fast	Supply ramp rate(fast)	-	-	-	100	V/ms
T_A	Operating temperature range	-	-40	-	125	°C

(1) Value guaranteed by design, not 100% tested in production.

Table 3-4. TCM & SRAM interface frequency for GD32A711B/A712B (1)

Symbol	Description	Conditions	Min	Max	Unit
f_{TWW}	TCM without wait	-	-	120	MHz
	SRAM without wait		-	106	

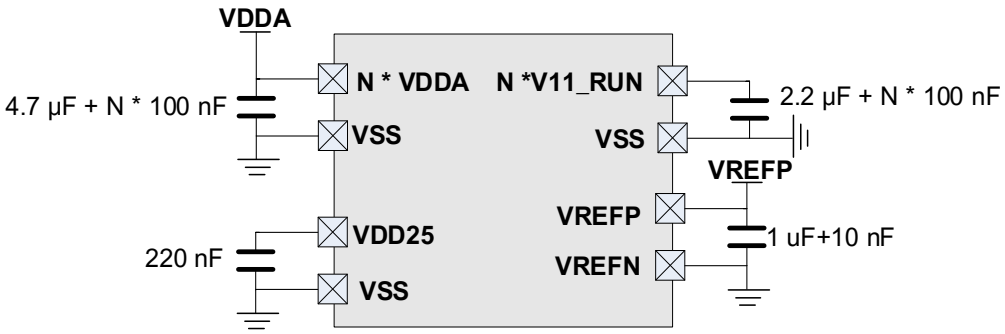
(1) Value guaranteed by design, not 100% tested in production.

Table 3-5. TCM & SRAM interface frequency for GD32A711A/A712A (1)

Symbol	Description	Conditions	Min	Max	Unit
f_{TWW}	TCM without wait	-	-	160	MHz
	SRAM without wait		-	106	

(2) Value guaranteed by design, not 100% tested in production.

Figure 3-1. Recommended power supply decoupling capacitors (1)



(1) VREFP should always be equal to or less than VDDA.

(2) VREFP selects either an independent reference source for power supply or synchronizes with VDDA for power supply based on specific application scenarios.

Table 3-6. Start-up timings of Operating conditions (1)(2)

Symbol	Description	Conditions	Typ	Unit
$t_{start-up}$	Start-up time	Clock source from IRC48M	17.3	us

(1) Value guaranteed by design, not 100% tested in production.

(2) Hardware initialization time, not include SBAF and user code run time

Table 3-7. Power saving mode wakeup timings characteristics (1)(2)

Symbol	Description	Typ	Unit
$t_{Standby}$	Wakeup from Standby mode	20.9	us

(1) Value guaranteed by design, not 100% tested in production.

(2) Hardware initialization time, not include SBAF and user code run time

3.4. Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications. Typical current numbers are typical silicon process and may vary based on the silicon distribution and user configuration.

Table 3-8. Power consumption in Standby mode

Symbol	Description	Conditions	Typ(1)(3)				Max(2)(4)				Unit
		General	25°C	85°C	105°C	125°C	25°C	85°C	105°C	125°C	
I_{VDDA}	Current from VDDA	All clocks and peripherals off	47.00	197.86	374.66	699.55	132.3	837.9	1447.0	2643.8	uA
		IRC40K on	47.76	198.78	376.06	702.20	133.2	839.1	1448.6	2644.2	
		IRC48M on	1080	1230	1410	1740	1608	2323.9	2939	3970.8	

(1) Value guaranteed by sample, not 100% tested in production.
(2) Value guaranteed by characterization, not 100% tested in production.
(3) "typ" is average current numbers at the nominal internally regulated V11 supply voltage, V_{DDA} = V_{DDB} = 5 V, for the typical silicon process.
(4) "max" is the maximum current numbers at the maximum internally regulated V11 supply voltage (1.16 V), V_{DDA} = V_{DDB} = 5.5 V, for the fast silicon process.

Table 3-9. Power consumption in Low run mode for GD32A711B/A712B (4) (5)

Symbol	Description	Conditions		Typ (1)(3)				Unit
		General		25°C	85°C	105°C	125°C	
I_{VDDA}	current from VDDA	Single core@60M HSM core@60M	All peripherals enabled	49.73	55.00	60.90	71.31	mA
			All peripherals disabled	27.45	32.44	38.06	48.04	
		Single core@120M HSM core@60M	All peripherals enabled	78.46	84.12	90.40	101.62	
			All peripherals disabled	37.57	42.69	48.45	58.67	

(1) Value guaranteed by sample, not 100% tested in production.
(2) Value guaranteed by characterization, not 100% tested in production.

(3) "typ" is the average current numbers at the nominal internally regulated V11 supply voltage, V_{DDA} = V_{DDB} = 5 V, for the typical silicon process.

(4) All GPIOs are configured as analog mode.

(5) The GD32A711B/A712B and GD32A711A/A712A share the same family architecture and silicon design, with GD32A711A/A712A operating at a higher maximum clock frequency. The GD32A711A/A712A data can be used as a reference for maximum power consumption at 125°C.

Table 3-10. Power consumption in Low run mode for GD32A711A/A712A (3)(6)

Symbol	Description	Conditions		Typ (1)(4)				Max (2)(5)	Unit
		General		25°C	85°C	105°C	125°C	125°C	
I_{VDDA}	current from VDDA	Single core@80M HSM core@80M	All peripherals enabled	57.79	63.10	69.06	78.82	-	mA
			All peripherals disabled	29.46	34.44	40.04	49.99	-	
		Single core@160M HSM core@80M	All peripherals enabled	98.65	104.87	111.40	122.77	145	
			All peripherals disabled	45.55	50.74	56.59	66.93	-	

(1) Value guaranteed by sample, not 100% tested in production.

(2) Value guaranteed by production.

(3) The junction temperature must be kept below the maximum specification, T_J < 150°C, to avoid self-heating.

(4) "typ" is the average current numbers at the nominal internally regulated V11 supply voltage, VDDA = 5.0V, for the typical silicon process.

(5) "max" is the maximum current numbers at the maximum internally regulated V11 supply voltage (1.16 V), VDDA = 5.5V, for the fast silicon process.

(6) All GPIOs are configured as analog mode.

3.5. EMC

EMI (Electromagnetic Interference) emission test result is given in the *Table 3-11. EMI characteristics for GD32A711B/A712B* , *Table 3-12. EMI characteristics for GD32A711A/A712A* .The electromagnetic field emitted by the device is monitored while an application, executing EEMBC code, is running. The test is compliant with SAE J1752-3:2017 standard which specifies the test board and the pin loading.

Table 3-11. EMI characteristics for GD32A711B/A712B

Symbol	Description	Conditions	Tested frequency band	Max vs. [f_{HXTAL}/f_{CPU}] 8/120 MHz	Unit
S_{EMI}	Peak level	V_{DDA} = 5.5 V, T_A = 23 ± 5 °C, LQFP176, f_{CPU} = 120 MHz, conforms to SAE J1752-3:2017	0.15 MHz to 30 MHz	-8.82	dBμV
			30 MHz to 200 MHz	4.98	
			200 MHz to 1 GHz	9.47	
			1 GHz to 3 GHz	5.88	

Table 3-12. EMI characteristics for GD32A711A/A712A

Symbol	Description	Conditions	Tested frequency band	Max vs. [f_{HXTAL}/f_{CPU}] 8/160 MHz	Unit
S_{EMI}	Peak level	V_{DDA} = 5.5 V, T_A = 23 ± 5 °C, LQFP176, f_{CPU} = 160 MHz, conforms to SAE J1752-3:2017	0.15 MHz to 30 MHz	-7.41	dBμV
			30 MHz to 200 MHz	2.71	
			200 MHz to 1 GHz	10.01	
			1 GHz to 3 GHz	5.11	

3.6. Power supply supervisor

Table 3-13. Power supply supervisor characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DDA_LVR} (2)	LVR on V_{DDA}, assert threshold	-	2.62	2.74	2.86	V
$V_{DDA_LVR_hyst}$ (2)	V_{DDA} LVR, monitor hysteresis	-	-	25	-	mV
V_{DDA_HVD} (1)	HVD on V_{DDA}, assert threshold	-	5.7	5.9	6.1	V
$V_{DDA_HVD_hyst}$ (1)	V_{DDA} HVD monitor hysteresis	-	-	40	-	mV
V_{DDA_LVD} (2)	Low Voltage Interrupt (LVI) on V_{DDA}, assert threshold		4.24	4.39	4.54	V

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DDA_POR} (1)	-	-	1.95	2.1	2.25	V
V_{DDA_PDR} (1)	-	-	1.9	2.05	2.2	V
V_{REF12}	Bandgap reference, trimmed	-	1.16	1.20	1.24	V

(1) Value guaranteed by design, not 100% tested in production.

(2) Value guaranteed by characterization, not 100% tested in production.

3.7. Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up (LU) test is based on the two measurement methods.

Table 3-14. ESD and static latch-up characteristics (1) (2) (3)

Symbol	Description	Conditions		Min	Typ	Max	Unit
$V_{ESD(HBM)}$ (4)	Electrostatic discharge voltage (human body model)	T_A = 25 °		-2000	-	2000	V
$V_{ESD(CDM)}$ (5)	Electrostatic discharge voltage (charge device model)	All pins except the corner pins	T_A = 25 °C	-500	-	500	V
		Corner pins only		-750	-	750	V
LU (6)	I-test	T_A = 125 °C		-100	-	100	mA
	V_{supply} over voltage			-	-	8.25	V

(1) All ESD testing are in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

(2) Device failure is defined as: "If after exposure to ESD pulses, the device does not meet the device specification requirements, which include the complete DC parametric and functional testing at room temperature and hot temperature".

(3) This parameter is tested in conformity with AEC-Q100-002E.

(4) This parameter is tested in conformity with AEC-Q100-011D.

(5) This parameter is tested in conformity with AEC-Q100-004D.

3.8. External clock

Table 3-15. High speed external clock (HXTAL) (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{HXTAL}	Crystal or ceramic frequency	-	4	-	40	MHz
R_F	Feedback resistor	-	-	400	-	kΩ
C_{HXTAL}	Recommended matching capacitance on OSCIN and OSCOUT	-	-	20	30	pF
$Ducy_{(HXTAL)}$	Crystal or ceramic duty cycle	-	30	50	70	%
g_m	Oscillator transconductance	Startup, RCU_CTL_HXTALSCAL=00	3.8	4.7	5.4	mA/V
		Startup, RCU_CTL_HXTALSCAL=01	7.7	9.5	11.4	
		Startup, RCU_CTL_HXTALSCAL=10	15.2	19.3	24.0	
		Startup, RCU_CTL_HXTALSCAL=11	22.4	29.7	37.4	
$I_{DDHXTAL}$	Crystal or ceramic operating current	V_{DDA} = 5 V, 40MHz	-	2	-	mA
$t_{SUHXTAL}$	Crystal or ceramic startup time	V_{DDA} = 5 V, 40MHz	-	0.4	-	ms

(1) Value guaranteed by design, not 100% tested in production.

(2) $C_{HXTAL1} = C_{HXTAL2} = 2*(C_{LOAD} - C_S)$, for C_{HXTAL1} and C_{HXTAL2}, it is recommended matching capacitance on OSCIN and OSCOUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

Table 3-16. High speed external clock (HXTAL) in bypass mode (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{HXTAL_ext}	External clock source or oscillator frequency	-	1	-	50	MHz
V_{HXTALH}	OSCIN input pin high level voltage	-	$0.7V_{DDA}$	-	V_{DDA}	V
V_{HXTALL}	OSCIN input pin low level voltage		V_{SS}	-	$0.3V_{DDA}$	V
$t_{H/L(HXTAL)}$	OSCIN high or low time	-	5	-	-	ns
$t_{R/F(HXTAL)}$	OSCIN rise or fall time	-	-	-	10	ns
C_{IN}	OSCIN input capacitance	-	-	5	-	pF
$Ducy_{(HXTAL)}$	Duty cycle	-	30	-	70	%

(1) Value guaranteed by design, not 100% tested in production.

Table 3-17. Low speed external clock (LXTAL) (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{LXTAL}	Crystal or ceramic frequency	-	-	32.768	-	kHz
C_{LXTAL}	Recommended matching capacitance on OSC32IN and OSC32OUT	-	-	10	-	pF
$Duty_{LXTAL}$	Crystal or ceramic duty cycle	-	30	-	70	%
g_m	Oscillator transconductance	LXTALDRI [1:0] = 00	-	3.4	-	μA/V
		LXTALDRI [1:0] = 01	-	6.8	-	
		LXTALDRI [1:0] = 10	-	16.7	-	
		LXTALDRI [1:0] = 11	-	26.7	-	
$I_{DD(LXTAL)}$	Crystal or ceramic operating current	LXTALDRI [1:0] = 00	-	1.1	-	uA
		LXTALDRI [1:0] = 01	-	1.3	-	
		LXTALDRI [1:0] = 10	-	2.1	-	
		LXTALDRI [1:0] = 11	-	3	-	
$t_{START(LXTAL)}$	Crystal or ceramic startup time	LXTALDRI [1:0] = 00	-	3	-	s
		LXTALDRI [1:0] = 01	-	0.85	-	
		LXTALDRI [1:0] = 10	-	0.34	-	
		LXTALDRI [1:0] = 11	-	0.26	-	

(1) Value guaranteed by design, not 100% tested in production.

Table 3-18. Low speed external clock (LXTAL) in bypass mode (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
F_{LXTAL_ext}	External clock source or oscillator frequency	-	-	-	1000	kHz
V_{LXTALH}	OSC32IN input pin high level voltage	-	0.7 V_{DDA}	-	V_{DDA}	V
V_{LXTALL}	OSC32IN input pin low level voltage		V_{SS}	-	0.3 V_{DDA}	V
$t_{H/L(LXTAL)}$	OSC32IN high or low time	-	250	-	-	ns
$t_{R/F(LXTAL)}$	OSC32IN rise or fall time	-	-	-	50	ns
C_{IN}	OSC32IN input capacitance	-	-	5	-	pF
$Ducy_{(LXTAL)}$	Duty cycle	-	30	-	70	%

(1) Value guaranteed by design, not 100% tested in production.

3.9. Internal clock

Table 3-19. High speed internal clock (IRC48M) characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{IRC48M} (1)	High Speed Internal Oscillator (IRC48M) frequency	V_{DDA} = 5 V	-	48	-	MHz
ACC_{IRC48M}	IRC48M oscillator Frequency accuracy, Factory-trimmed	V_{DDA} = 2.97~5.5 V, T_A = -40 °C ~ +125 °C	-2.5	-	2.5	%
		V_{DDA} = 2.97~5.5 V, T_A = 25 °C	-1	-	1	%
	IRC48M oscillator Frequency accuracy, User trimming step (1)	-	-	0.3	-	%
$Ducy_{IRC48M}$ (1)	IRC48M oscillator duty cycle	-	45	-	55	%
$I_{DDAIRC48M}$ (1)	IRC48M oscillator operating current	-	-	1.1	-	mA
$t_{SUIRC48M}$ (1)	IRC48M oscillator startup time	-	-	4.8	-	us

(1) Value guaranteed by design, not 100% tested in production.

Table 3-20. Low speed internal clock (IRC40K) characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{IRC40K} (1)	Low Speed Internal oscillator (IRC40K) frequency	V_{DDA} = 5 V	-	40	-	kHz
ACC_{IRC40K}	IRC40K oscillator Frequency accuracy, Factory-trimmed	V_{DDA} = 2.97~5.5 V, T_A = -40 °C ~ +125 °C	-10	-	10	%
		V_{DDA} = 2.97~5.5 V, T_A = 25 °C	-7	-	7	%
$I_{DDAIRC40K}$ (1)	IRC40K oscillator operating current	-	-	0.75	-	μA
$t_{SUIRC40K}$ (1)	IRC40K oscillator startup time	-	-	30	-	μs

(1) Value guaranteed by design, not 100% tested in production.

3.10. PLL

Table 3-21. PLL characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{PLLIN}	PLL input clock frequency	After pre div	8	-	40	MHz
f_{PLLOUT}	PLL output clock frequency	For GD32A711B/A712B	-	-	120	MHz
		For GD32A711A/ A712AxxxxB	-	-	160	MHz
f_{VCO}	PLL VCO output clock frequency	-	640	-	1280	MHz
t_{LOCK}	PLL lock time	-	-	-	500	us
PLL_DS	Modulation Depth	Down spread	-0.5	-	-3	%
		Center spread	-1.5	-	1.5	%
PLL_FM	Modulation frequency	-	-	-	32	kHz

Symbol	Description	Conditions	Min	Typ	Max	Unit
I_{PLL_V25}	Current consumption on V25	VCO freq = 640 MHz	-	0.55	-	mA
		VCO freq = 1280 MHz	-	1.2	-	
$Jitter_{PLL}$	Period Jitter(rms)	PLL_OUT= 40 MHz	-	40	-	ps
	Cycle to cycle Jitter (rms)		-	66	-	

(1) Value guaranteed by design, not 100% tested in production.

3.11. Memory

Table 3-22. Flash memory characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
PE_{CYC} (2)	Number of guaranteed program /erase cycles before failure (Endurance)	T_A = -40°C ~ +125 °C	100	-	-	kcycles
t_{RET} (2)	Data retention time	T_A = -40°C ~ +125 °C(4)	20	-	-	years
t_{dwROG} (2)	Double-Word programming time	T_A = -40°C ~ +125 °C	-	52	-	µs
t_{PROG} (2)	64 double-word Page programming time	T_A = -40°C ~ +125 °C	-	800	-	
t_{ERASE} (2)	Sector erase time	T_A = -40°C ~ +125 °C	3	6	22	ms
t_{MERASE} (128K dflash0)	Mass erase time	T_A = -40°C ~ +125 °C	-	20	-	ms
t_{MERASE} (96K dflash1)			144	-	1056	ms
$t_{MERASE(1024K)}$ (3)			1536	-	11264	ms
$t_{MERASE(2048K)}$ (3)			3072	-	22528	ms

(1) Value guaranteed by design, not 100% tested in production.
(2) Applicable to data flash and code flash.
(3) Applicable to code flash.
(4) Block program/erase cycle data is not characterized on this device.

3.12. NRST pin

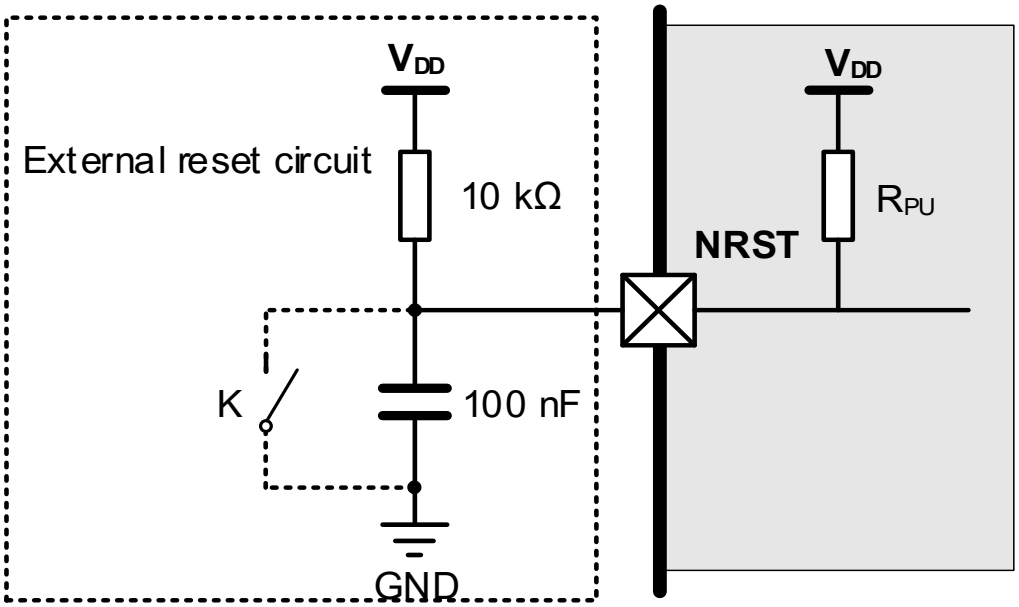
Table 3-23. NRST pin characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST Input low level voltage	V_{DDA} = 2. 97 V	V_{SS}-0.3	-	0.3V_{DDA}	V
$V_{IH(NRST)}$	NRST Input high level voltage		0.7V_{DDA}	-	V_{DDA} +0.3	
V_{hyst}	Schmidt trigger Voltage hysteresis		320	410	-	mV
$V_{IL(NRST)}$	NRST Input low level voltage	V_{DDA} = 3.3 V	V_{SS}-0.3	-	0.3V_{DDA}	
$V_{IH(NRST)}$	NRST Input high level voltage		0.7V_{DDA}	-	V_{DDA} +0.3	
V_{hyst}	Schmidt trigger Voltage hysteresis		380	460	-	
$V_{IL(NRST)}$	NRST Input low level voltage	V_{DDA} = 5.0 V	V_{SS}-0.3	-	0.3V_{DDA}	V

Symbol	Description	Conditions	Min	Typ	Max	Unit
$V_{IH(NRST)}$	NRST Input high level voltage		$0.7V_{DDA}$	-	V_{DDA} +0.3	
V_{hyst}	Schmidt trigger Voltage hysteresis		530	600	-	mV
$V_{IL(NRST)}$	NRST Input low level voltage	V_{DDA} = 5.5 V	V_{SS}-0.3	-	$0.3V_{DDA}$	V
$V_{IH(NRST)}$	NRST Input high level voltage		$0.7V_{DDA}$	-	V_{DDA} +0.3	
V_{hyst}	Schmidt trigger Voltage hysteresis		570	640	-	mV
R_{pu}	Pull-up equivalent resistor	-	-	40	-	kΩ

(1) Value guaranteed by design, not 100% tested in production.

Figure 3-2. Recommended external NRST pin circuit (1)



(1) Unless the voltage on NRST pin go below $V_{IL(NRST)}$ level, the device would not generate a reliable reset.

3.13. GPIO

Table 3-24. I/O DC characteristics, 3.3V Range (2.97V-3.63V) (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	High level input voltage	V_{DDA}=3.3V	$0.7V_{DDA}$	-	V_{DDA}+0.3	V
V_{IL}	Low level input voltage	V_{DDA}=3.3V	V_{SS}-0.3	-	$0.3V_{DDA}$	V
VHYS_33	Input hysteresis	-	$0.06V_{DDA}$	0.119 V_{DDA}	-	V
ILKG_33_S (2)	3.3V input leakage current for Standard GPIO	-	-600 (3)	-	700 (3)	nA
ILKG_33_SP (2)	3.3V input leakage current for Standard Plus GPIO	-	-600	-	700	nA
ILKG_33_M (2)	3.3V input leakage	-	-600	-	700	nA

Symbol	Description	Conditions	Min	Typ	Max	Unit
	current for Medium GPIO					
ILKG_33_F (2)	3.3V input leakage current for Fast GPIO	-	-700	-	850	nA
CIN	GPIO Input capacitance	add 2pF for package/parasitic	2	4.5	7	pF
IPU_33	3.3V GPIO pull up/down resistance	pull up@0.3V_{DDA} pull down@0.7V_{DDA}	30	-	50	kΩ
IOH_33_S (2)	3.3V output high current for Standard GPIO	VOH>=V_{DDA}-0.7V	1.0	-	-	mA
IOH_33_SP (2)	3.3V output high current for Standard Plus GPIO	OSPD=0, VOH>=V_{DDA} -0.7V	1.5	-	-	mA
IOH_33_M (2)	3.3V output high current for Medium GPIO	OSPD=0, VOH>=V_{DDA} -0.7V	3	-	-	mA
IOH_33_F (2)	3.3V output high current for Fast GPIO	OSPD=0, VOH>=V_{DDA} -0.7V	4.5	-	-	mA
IOH_33_SP (2)	3.3V output high current for Standard Plus GPIO	OSPD=1, VOH>=V_{DDA} -0.7V	3	-	-	mA
IOH_33_M (2)	3.3V output high current for Medium GPIO	OSPD=1, VOH>=V_{DDA} -0.7V	6	-	-	mA
IOH_33_F (2)	3.3V output high current for Fast GPIO	OSPD=1, VOH>=V_{DDA} -0.7V	9	-	-	mA
IOL_33_S (2)	3.3V output low current for Standard GPIO	VOL<= 0.7V	1	-	-	mA
IOL_33_SP (2)	3.3V output low current for Standard Plus GPIO	OSPD=0, VOL<= 0.7V	1.5	-	-	mA
IOL_33_M (2)	3.3V output low current for Medium GPIO	OSPD=0, VOL<= 0.7V	3	-	-	mA
IOL_33_F (2)	3.3V output low current for Fast GPIO	OSPD=0, VOL<= 0.7V	4.5	-	-	mA
IOL_33_SP (2)	3.3V output low current for Standard Plus GPIO	OSPD=1, VOL<= 0.7V	3	-	-	mA
IOL_33_M (2)	3.3V output low current for Medium GPIO	OSPD=1, VOL<= 0.7V	6	-	-	mA
IOL_33_F (2)	3.3V output low current for Fast GPIO	OSPD=1, VOL<= 0.7V	9	-	-	mA
FMAX_33_S	3.3V maximum frequency for Standard GPIO	2.9V-3.6V, total 25pF load includes internal 5pF, PCB trace ~10pF and external 10pF	-	-	10	MHz
FMAX_33_SP	3.3V maximum frequency for Standard Plus GPIO	2.9V-3.6V, total 25pF load includes	-	-	25	MHz

Symbol	Description	Conditions	Min	Typ	Max	Unit
		internal 5pF, PCB trace ~10pF and external 10pF				
FMAX_33_M	3.3V maximum frequency for Medium GPIO	2.9V-3.6V, total 25pF load includes internal 5pF, PCB trace ~10pF and external 10pF	-	-	50	MHz
FMAX_33_F	3.3V maximum frequency for Fast GPIO	2.9V-3.6V, total 25pF load includes internal 5pF, PCB trace ~10pF and external 10pF	-	-	120	MHz

(1) Value guaranteed by design, not 100% tested in production.
(2) Value guaranteed by characterization, not 100% tested in production.
(3) The leakage current of PI9 and PI10 are min: -1000, max: 1800nA.

Table 3-25. I/O DC characteristics, 5.0V Range (4.5V-5.5V) (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	High level input voltage	V_{DDA}=5.0V	0.7V_{DDA}	-	V_{DDA}+0.3	V
V_{IL}	Low level input voltage	V_{DDA}=5.0V	V_{SS}-0.3	-	0.3V_{DDA}	V
VHYS_50	Input hysteresis	-	0.06V_{DDA}	0.098 V_{DDA}	-	V
ILKG_50_S (2)	5.0V input leakage current for Standard GPIO	-	-600 (3)	-	700 (3)	nA
ILKG_50_SP (2)	5.0V input leakage current for Standard Plus GPIO	-	-600	-	700	nA
ILKG_50_M (2)	5.0V input leakage current for Medium GPIO	-	-600	-	700	nA
ILKG_50_F (2)	5.0V input leakage current for Fast GPIO	-	-700	-	850	nA
CIN	GPIO Input capacitance	add 2pF for package/parasitic	2	4.5	7	pF
IPU_50	5.0V GPIO pull up/down resistance	pull up@0.3V_{DDA} pull down@0.7V_{DDA}	30	-	50	kΩ
IOH_50_S (2)	5.0V output high current for Standard GPIO	VOH>=V_{DDA} -0.7V	1.6	-	-	mA
IOH_50_SP (2)	5.0V output high current for Standard Plus GPIO	OSPD=0, VOH>=V_{DDA} -0.7V	2.5	-	-	mA
IOH_50_M(2)	5.0V output high current for Medium GPIO	OSPD=0, VOH>=V_{DDA} -0.7V	4	-	-	mA
IOH_50_F (2)	5.0V output high current	OSPD=0, VOH>=V_{DDA}	6	-	-	mA

Symbol	Description	Conditions	Min	Typ	Max	Unit
	for Fast GPIO	-0.7V				
IOH_50_SP (2)	5.0V output high current for Standard Plus GPIO	OSPD=1, VOH>=V_{DDA} -0.7V	5	-	-	mA
IOH_50_M (2)	5.0V output high current for Medium GPIO	OSPD=1, VOH>=V_{DDA} -0.7V	8	-	-	mA
IOH_50_F (2)	5.0V output high current for Fast GPIO	OSPD=1, VOH>=V_{DDA} -0.7V	12	-	-	mA
IOL_50_S (2)	5.0V output low current for Standard GPIO	VOL<= 0.7V	1.6	-	-	mA
IOL_50_SP (2)	5.0V output low current for Standard Plus GPIO	OSPD=0, VOL<= 0.7V	2.5	-	-	mA
IOL_50_M (2)	5.0V output low current for Medium GPIO	OSPD=0, VOL<= 0.7V	4	-	-	mA
IOL_50_F (2)	5.0V output low current for Fast GPIO	OSPD=0, VOL<= 0.7V	6	-	-	mA
IOL_50_SP (2)	5.0V output low current for Standard Plus GPIO	OSPD=1, VOL<= 0.7V	5	-	-	mA
IOL_50_M (2)	5.0V output low current for Medium GPIO	OSPD=1, VOL<= 0.7V	8	-	-	mA
IOL_50_F (2)	5.0V output low current for Fast GPIO	OSPD=1, VOL<= 0.7V	12	-	-	mA
FMAX_50_S	5.0V maximum frequency for Standard GPIO	3.6V - 5.5V, total 25pF load includes internal 5pF, PCB trace ~10pF and external 10pF	-	-	10	MHz
FMAX_50_SP	5.0V maximum frequency for Standard Plus GPIO	3.6V - 5.5V, total 25pF load includes internal 5pF, PCB trace ~10pF and external 10pF	-	-	25	MHz
FMAX_50_M	5.0V maximum frequency for Medium GPIO	3.6V - 5.5V, total 25pF load includes internal 5pF, PCB trace ~10pF and external 10pF	-	-	50	MHz
FMAX_50_F	5.0V maximum frequency for Fast GPIO	3.6V - 5.5V, total 25pF load includes internal 5pF, PCB trace ~10pF and external 10pF	-	-	120	MHz

(1) Value guaranteed by design, not 100% tested in production.
(2) Value guaranteed by characterization, not 100% tested in production.
(3) The leakage current of PI9 and PI10 are min: -1000, max: 1800nA.

Table 3-26. 3.3V (2.97V-3.63V) I/O AC characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
TR_TF_33_S	3.3V Standard GPIO	Capacitance=25pF	5.09	-	16.6	ns

Symbol	Description	Conditions	Min	Typ	Max	Unit
	rise/fall time					
TR_TF_33_S	3.3V Standard GPIO rise/fall time	Capacitance=50pF	9.55	-	31	ns
TR_TF_33_SP	3.3V Standard Plus GPIO rise/fall time	OSPD=0, Capacitance=25pF	3.84	-	11.6	ns
TR_TF_33_SP	3.3V Standard Plus GPIO rise/fall time	OSPD=1, Capacitance=25pF	1.91	-	8.22	ns
TR_TF_33_SP	3.3V Standard Plus GPIO rise/fall time	OSPD=0, Capacitance=50pF	7.17	-	21.5	ns
TR_TF_33_SP	3.3V Standard Plus GPIO rise/fall time	OSPD=1, Capacitance=50pF	3.56	-	10.8	ns
TR_TF_33_M	3.3V Medium GPIO rise/fall time	OSPD=0, SREN=0, Capacitance=25pF	2.23	-	6.87	ns
TR_TF_33_M	3.3V Medium GPIO rise/fall time	OSPD=0, SREN=1, Capacitance=25pF	3.64	-	12.5	ns
TR_TF_33_M	3.3V Medium GPIO rise/fall time	OSPD=1, SREN=0, Capacitance=25pF	1.1	-	3.51	ns
TR_TF_33_M	3.3V Medium GPIO rise/fall time	OSPD=1, SREN=1, Capacitance=25pF	2.49	-	8.76	ns
TR_TF_33_M	3.3V Medium GPIO rise/fall time	OSPD=0, SREN=0, Capacitance=50pF	4.15	-	12.6	ns
TR_TF_33_M	3.3V Medium GPIO rise/fall time	OSPD=0, SREN=1, Capacitance=50pF	5.4	-	18.1	ns
TR_TF_33_M	3.3V Medium GPIO rise/fall time	OSPD=1, SREN=0, Capacitance=50pF	2.07	-	6.36	ns
TR_TF_33_M	3.3V Medium GPIO rise/fall time	OSPD=1, SREN=1, Capacitance=50pF	3.47	-	11.9	ns
TR_TF_33_F	3.3V Fast GPIO rise/fall time	OSPD=0, SREN=0, Capacitance=25pF	1.06	-	3.4	ns
TR_TF_33_F	3.3V Fast GPIO rise/fall time	OSPD=0, SREN=1, Capacitance=25pF	2.03	-	6.57	ns
TR_TF_33_F	3.3V Fast GPIO rise/fall time	OSPD=1, SREN=0, Capacitance=25pF	0.56	-	2.11	ns
TR_TF_33_F	3.3V Fast GPIO rise/fall time	OSPD=1, SREN=1, Capacitance=25pF	1.46	-	4.75	ns
TR_TF_33_F	3.3V Fast GPIO rise/fall time	OSPD=0, SREN=0, Capacitance=50pF	2.01	-	6.05	ns
TR_TF_33_F	3.3V Fast GPIO rise/fall time	OSPD=0, SREN=1, Capacitance=50pF	2.86	-	9.18	ns
TR_TF_33_F	3.3V Fast GPIO rise/fall time	OSPD=1, SREN=0, Capacitance=50pF	1.03	-	3.13	ns
TR_TF_33_F	3.3V Fast GPIO rise/fall	OSPD=1, SREN=1,	1.95	-	6.25	ns

Symbol	Description	Conditions	Min	Typ	Max	Unit
	time	Capacitance=50pF				

(1) Value guaranteed by design, not 100% tested in production.

Table 3-27. 5.0V (4.5V-5.5V) I/O AC characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
TR_TF_50_S	5.0V Standard GPIO rise/fall time	Capacitance=25pF	4.22	-	10.5	ns
TR_TF_50_S	5.0V Standard GPIO rise/fall time	Capacitance=50pF	8.0	-	19.8	ns
TR_TF_50_SP	5.0V Standard Plus GPIO rise/fall time	OSPD=0, Capacitance=25pF	2.92	-	7.31	ns
TR_TF_50_SP	5.0V Standard Plus GPIO rise/fall time	OSPD=1, Capacitance=25pF	1.46	-	3.66	ns
TR_TF_50_SP	5.0V Standard Plus GPIO rise/fall time	OSPD=0, Capacitance=50pF	5.53	-	13.6	ns
TR_TF_50_SP	5.0V Standard Plus GPIO rise/fall time	OSPD=1, Capacitance=50pF	2.75	-	6.82	ns
TR_TF_50_M	5.0V Medium GPIO rise/fall time	OSPD=0, SREN=0, Capacitance=25pF	1.76	-	4.35	ns
TR_TF_50_M	5.0V Medium GPIO rise/fall time	OSPD=0, SREN=1, Capacitance=25pF	2.9	-	7.65	ns
TR_TF_50_M	5.0V Medium GPIO rise/fall time	OSPD=1, SREN=0, Capacitance=25pF	0.91	-	2.24	ns
TR_TF_50_M	5.0V Medium GPIO rise/fall time	OSPD=1, SREN=1, Capacitance=25pF	1.95	-	5.31	ns
TR_TF_50_M	5.0V Medium GPIO rise/fall time	OSPD=0, SREN=0, Capacitance=50pF	3.27	-	8.02	ns
TR_TF_50_M	5.0V Medium GPIO rise/fall time	OSPD=0, SREN=1, Capacitance=50pF	4.36	-	11.2	ns
TR_TF_50_M	5.0V Medium GPIO rise/fall time	OSPD=1, SREN=0, Capacitance=50pF	1.67	-	4.04	ns
TR_TF_50_M	5.0V Medium GPIO rise/fall time	OSPD=1, SREN=1, Capacitance=50pF	2.77	-	7.33	ns
TR_TF_50_F	5.0V Fast GPIO rise/fall time	OSPD=0, SREN=0, Capacitance=25pF	0.84	-	2.16	ns
TR_TF_50_F	5.0V Fast GPIO rise/fall time	OSPD=0, SREN=1, Capacitance=25pF	1.58	-	4.12	ns
TR_TF_50_F	5.0V Fast GPIO rise/fall time	OSPD=1, SREN=0, Capacitance=25pF	0.43	-	1.18	ns
TR_TF_50_F	5.0V Fast GPIO rise/fall time	OSPD=1, SREN=1, Capacitance=25pF	1.08	-	2.94	ns
TR_TF_50_F	5.0V Fast GPIO rise/fall time	OSPD=0, SREN=0, Capacitance=50pF	1.57	-	3.8	ns

Symbol	Description	Conditions	Min	Typ	Max	Unit
TR_TF_50_F	5.0V Fast GPIO rise/fall time	OSPD=0, SREN=1, Capacitance=50pF	2.28	-	5.79	ns
TR_TF_50_F	5.0V Fast GPIO rise/fall time	OSPD=1, SREN=0, Capacitance=50pF	0.77	-	1.96	ns
TR_TF_50_F	5.0V Fast GPIO rise/fall time	OSPD=1, SREN=1, Capacitance=50pF	1.5	-	3.91	ns

(1) Value guaranteed by design, not 100% tested in production.

3.14. Glitch Filter

Table 3-28. Glitch Filter (1)

Symbol	Description	Min	Typ	Max	Unit
TFILT	Glitch filter max filtered pulse width	-	-	20	ns
TUNFILT	Glitch filter min unfiltered pulse width	400	-	-	ns

(1) Value guaranteed by design, not 100% tested in production.

3.15. ADC

Table 3-29. ADC characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage	-	2.97	5.0	5.5	V
V_{REFP}	Positive Reference Voltage	-	2.97	5.0	5.5	V
V_{REFN}	Negative Reference Voltage	-	-	V_{SS}	-	V
V_{IN}	ADC input voltage range	-	0	-	V_{REFP}	V
f_{ADC}	ADC clock	-	1.875	-	16	MHz
f_S	Sampling rate	12-bit	0.125	-	1.067	MSPs
		10-bit	0.144	-	1.23	
		8-bit	0.17	-	1.45	
		6-bit	0.208	-	1.78	
R_{AIN}	External input impedance	See ***Equation 1***	-	-	355	kΩ
R_{ADC}	Input sampling switch resistance	-	-	-	800	Ω
C_{ADC}	Input sampling capacitance	No pin/pad capacitance included	-	3.7	5.4	pF
TUE	Total Unadjusted Error	CALNUM [2:0] = 000	-	±3	±6	LSB
t_s	Sampling time	f_{ADC} = 16 MHz	0.156	-	40.03	μs
			2.5	-	640.5	$1/f_{ADC}$
t_{CONV}	Total conversion time (including sampling time)	12-bit	-	15	-	$1/ f_{ADC}$
		10-bit	-	13	-	
		8-bit	-	11	-	
		6-bit	-	9	-	
t_{SU}	Startup time	-	-	-	1	μs
I_{VDDA}	ADC consumption from the V_{DDA} supply	f_{ADC} = 16 MHz, V_{DDA} = V_{REFP} = 5 V	-	1.2	-	mA
I_{VREFP}	ADC consumption from the V_{REFP} supply(When capacitor selftest off)	f_{ADC} = 16 MHz, V_{DDA} = V_{REFP} = 5 V	-	0.025	-	mA

(1) Value guaranteed by design, not 100% tested in production.

Equation 1: R_{AIN} max formula $R_{AIN} < \frac{T_s}{f_{ADC} * C'_{ADC} * \ln(2^{N+2})} - R_{ADC}$

The formula above (Equation 1) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution). C'_{ADC} includes C_{ADC} and Parasitic Capacitance.

Table 3-30. Internal reference voltage value

Symbol	Description	Conditions	Min	Typ	Max	Unit
$V_{REFINT0/1}$	Internal Reference Voltage	-	1.16	1.2	1.24	V

Table 3-31. Internal reference voltage calibration values

Symbol	Test conditions	Memory address
$V_{REFINT0}$	V_{DDA} = V_{REFP} = 5V, T_A = 25 ± 5 °C	0x1FFFF7FC-0x1FFFF7FD
$V_{REFINT1}$		0x1FFFF7DC-0x1FFFF7DD

Table 3-32. ADC dynamic accuracy at f_{ADC} = 16 MHz, V_{DDA} = V_{REFP} = 5.0 V(1)

Symbol	Description	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 16 MHz	10.8	11.2	-	bits
SNDR	Signal-to-noise and distortion ratio	Input Frequency = 20 kHz	66.8	69.2	-	dB
SNR	Signal-to-noise ratio	Temperature = - 40~125 °C	67	70	-	
THD	Total harmonic distortion	CALNUM [2:0] =000		-77	-71	

(1) Value guaranteed by characterization, not 100% tested in production.

Table 3-33. ADC dynamic accuracy at f_{ADC} = 16 MHz, V_{DDA} = V_{REFP} = 2.97 V(1)

Symbol	Description	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 16 MHz	10.5	10.9	-	bits
SNDR	Signal-to-noise and distortion ratio	Input Frequency = 20 kHz	65	67.4	-	dB
SNR	Signal-to-noise ratio	Temperature = - 40~125 °C	65	68.3	-	
THD	Total harmonic distortion	CALNUM [2:0] = 000		-77.1	-70	

(1) Value guaranteed by characterization, not 100% tested in production.

Table 3-34. ADC static accuracy at f_{ADC} = 16 MHz ,, V_{DDA} = V_{REFP} = 5.0 V(1)

Symbol	Description	Test conditions	Min	Typ	Max	Unit
Offset	Offset error	f_{ADC} = 16 MHz	-5	-	5	LSB
DNL	Differential linearity error	Temperature = - 40~125 °C	-1	-	2	
INL	Integral linearity error	CALNUM [2:0] = 000	-2.5	-	2.5	

(1) Value guaranteed by characterization, not 100% tested in production.

Table 3-35. ADC static accuracy at f_{ADC} = 16 MHz , V_{DDA} = V_{REFP} = 2.97 V(1)

Symbol	Description	Test conditions	Min	Typ	Max	Unit
Offset	Offset error	f_{ADC} = 16 MHz	-5	-	5	LSB
DNL	Differential linearity error	Temperature = - 40~125 °C	-1	-	3.5	
INL	Integral linearity error	CALNUM [2:0] = 000	-3	-	3	

(1) Value guaranteed by characterization, not 100% tested in production.

3.16. DAC

Table 3-36. DAC characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage	-	2.97	5.0	5.5	V
V_{REFP}	Positive Reference Voltage	-	2.97	-	V_{DDA}	V
V_{REFN}	Negative Reference Voltage	-	-	V_{SS}	-	V
R_{LOAD}	Resistive load	Resistive load with buffer ON	1	-	-	kΩ
Ro	Impedance output	Impedance output with buffer OFF	-	-	15	kΩ
C_{LOAD}	Capacitive load	Capacitive load with buffer ON	-	-	100	pF
DAC_OUT min	Lower DAC_OUT voltage	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V
		Lower DAC_OUT voltage with buffer OFF	0.5	-	-	mV
DAC_OUT max	Higher DAC_OUT voltage	Higher DAC_OUT voltage with buffer ON	-	-	V_{DDA}-0.2	V
		Higher DAC_OUT voltage with buffer OFF	-	-	V_{REFP}-1LSB	V
I_{DDA}	DAC current consumption in quiescent mode	With no load, middle code(0x800) on the input, V_{REFP} = 5.5 V	-	775	-	μA
		With no load, worst code(0xF1C) on the input, V_{REFP} = 5.5 V	-	900	-	
$I_{DDVREFP}$	DAC current consumption in quiescent mode	With no load, middle code(0x800) on the input, V_{REFP} = 5.5 V	-	180	-	μA
		With no load, worst code(0xF1C) on the input, V_{REFP} = 5.5 V	-	240	-	
DNL (2)	Differential non linearity	10-bit configuration, buffer ON	-	-	±1	LSB
		12-bit configuration, buffer ON	-	-	±4	
INL (2)	Integral non linearity	10-bit configuration, buffer ON	-	-	±1.5	LSB
		12-bit configuration, buffer ON	-	-	±6	
Offset (2)	Offset error	DAC in 12-bit mode	-	-	±20	LSB
GE (2)	Gain error	DAC in 12-bit mode, buffer ON	-	-	±1	%
$T_{setting}$	Settling time	$C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq$ 5 kΩ	-	1	2	μs
T_{wakeup}	Wakeup from off state	-	-	5	10	μs
Update rate	Max frequency for a correct DAC_OUT change from code i to i±1LSB	$C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq$ 5 kΩ	-	-	2	MS/s

Symbol	Description	Conditions	Min	Typ	Max	Unit
PSRR	Power supply rejection ratio (to V_{DDA})	No R_{Load}, C_{LOAD} = 50 pF	55	80	-	dB

(1) Value guaranteed by design, not 100% tested in production.

(2) Value guaranteed by characterization, not 100% tested in production.

3.17. I2C

Table 3-37. I2C characteristics (1)(2)

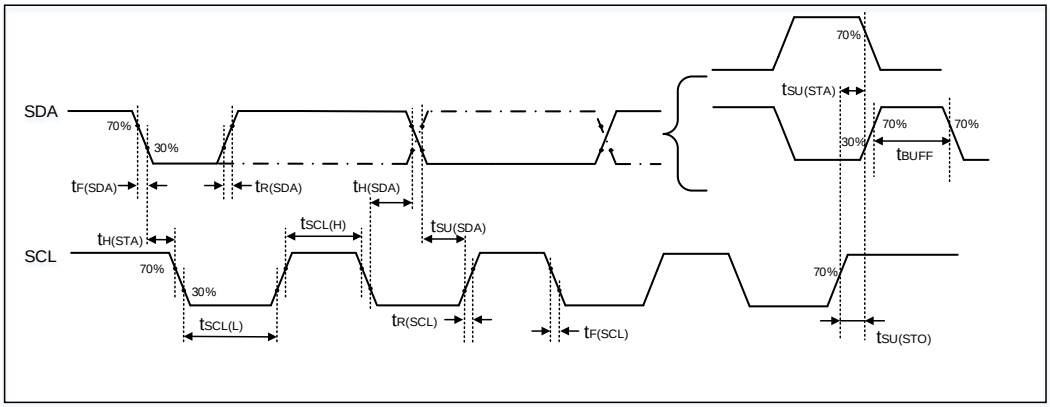
Symbol	Description	Conditions	Standard mode		Fast mode		Fast mode plus		Unit
			Min	Max	Min	Max	Min	Max	
$t_{SCL(H)}$	SCL clock high time	-	4.0	-	0.6	-	0.2	-	μs
$t_{SCL(L)}$	SCL clock low time	-	4.7	-	1.3	-	0.5	-	μs
$t_{SU(SDA)}$	SDA setup time	-	250	-	100	-	50	-	ns
$t_{H(SDA)}$	SDA data hold time	-	0(3)	3450	0	900	0	450	ns
$t_{R(SDA/SCL)}$	SDA and SCL rise time	-	-	1000	-	300	-	120	ns
$t_{F(SDA/SCL)}$	SDA and SCL fall time	-	-	300	-	300	-	120	ns
$t_{H(STA)}$	Start condition hold time	-	4.0	-	0.6	-	0.26	-	μs
$t_{SU(STA)}$	Repeated Start condition setup time	-	4.7	-	0.6	-	0.26	-	μs
$t_{SU(STO)}$	Stop condition setup time	-	4.0	-	0.6	-	0.26	-	μs
t_{BUFF}	Stop to Start condition time (bus free)	-	4.7	-	1.3	-	0.5	-	μs

(1) Value guaranteed by design, not 100% tested in production.

(2) To ensure the standard mode I2C frequency, f_{PCLK1} must be at least 2 MHz. To ensure the fast mode I2C frequency, f_{PCLK1} must be at least 4 MHz. To ensure the fast mode plus I2C frequency, f_{PCLK1} must be at least a multiple of 10 MHz.

(3) The external device should provide a data hold time of 300 ns at least in order to bridge the undefined region of the falling edge of SCL.

Figure 3-3. I2C bus timing diagram



3.18. SPI

Table 3-38. Standard SPI characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/T_{SCK}$	SCK clock frequency	V_{DDA} = 5 V	-	-	20	MHz
$t_{sck(H)}$	SCK clock high time		-	$T_{SCK}/2$	-	ns
$t_{sck\ (L)}$	SCK clock low time		-	$T_{SCK}/2$	-	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time	V_{DDA} = 5 V	-	-	10	ns
$t_{H(MO)}$	Data output hold time		-	-	-	ns
$t_{SU(MI)}$	Data input setup time		5	-	-	ns
$t_{H(MI)}$	Data input hold time		5	-	-	ns
SPI slave mode						
$t_{SU(NSS)}$	NSS enable setup time	V_{DDA} = 5 V	50	-	-	ns
$t_{H(NSS)}$	NSS enable hold time		50	-	-	ns
$t_{A(SO)}$	Data output access time		-	25	-	ns
$t_{DIS(SO)}$	Data output disable time		-	9	-	ns
$t_{V(SO)}$	Data output valid time		-	10	-	ns
$t_{H(SO)}$	Data output hold time		-	-	-	ns
$t_{SU(SI)}$	Data input setup time		5	-	-	ns
$t_{H(SI)}$	Data input hold time		20	-	-	ns

(1) Value guaranteed by design, not 100% tested in production.

Figure 3-4. SPI timing diagram - master mode

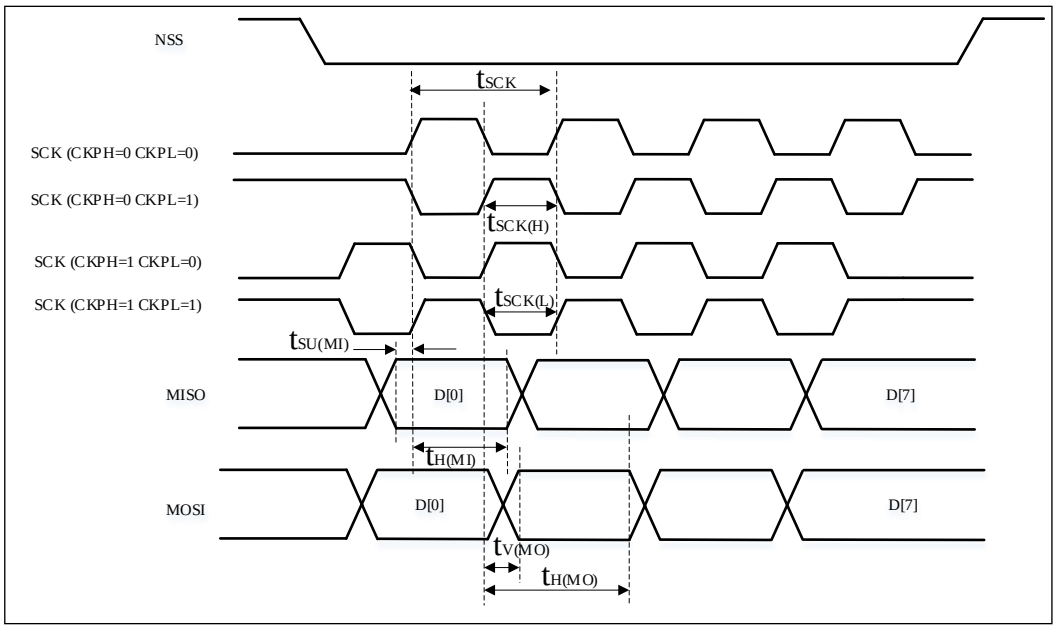
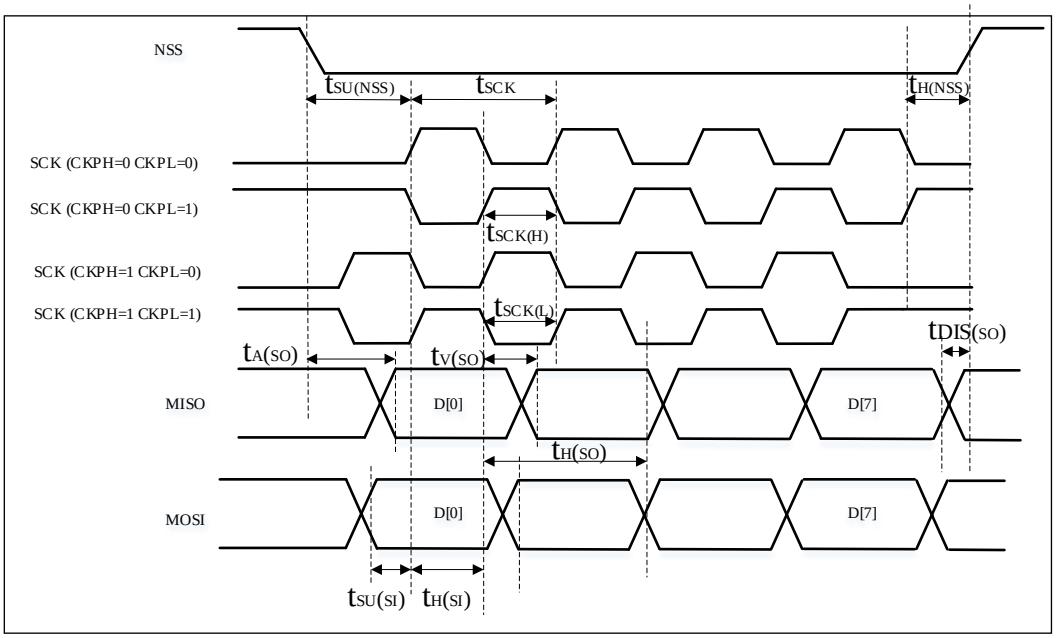


Figure 3-5. SPI timing diagram - slave mode



3.19. I2S

Table 3-39. I2S characteristics (1) (2)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{CK}	Clock frequency	Master mode (data: 32 bits, Audio frequency = 96 kHz)	-	6.25	-	MHz
		Slave mode	-	-	12.5	
t_H	Clock high time	f_{CK}= 6.25 MHz	-	80	-	ns
t_L	Clock low time		-	80	-	ns
$t_{V(WS)}$	WS valid time	Master mode	-	3	-	ns
$t_{H(WS)}$	WS hold time	Master mode	-	3	-	ns
$t_{SU(WS)}$	WS setup time	Slave mode	0	-	-	ns
$t_{H(WS)}$	WS hold time	Slave mode	3	-	-	ns
$Ducy_{(SCK)}$	I2S slave input clock duty cycle	Slave mode	-	50	-	%
$t_{SU(SD_MR)}$	Data input setup time	Master mode	1	-	-	ns
$t_{SU(SD_SR)}$	Data input setup time	Slave mode	0	-	-	ns
$t_{H(SD_MR)}$	Data input hold time	Master receiver	0	-	-	ns
$t_{H(SD_SR)}$		Slave receiver	1	-	-	ns
$t_{v(SD_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	-	10	ns
$t_{h(SD_ST)}$	Data output hold time	Slave transmitter (after enable edge)	3	-	-	ns
$t_{v(SD_MT)}$	Data output valid time	Master transmitter (after enable edge)	-	-	10	ns
$t_{h(SD_MT)}$	Data output hold time	Master transmitter (after enable edge)	0	-	-	ns

(1) Value guaranteed by design, not 100% tested in production.

(2) Value guaranteed by characterization, not 100% tested in production.

Figure 3-6. I2S timing diagram - master mode

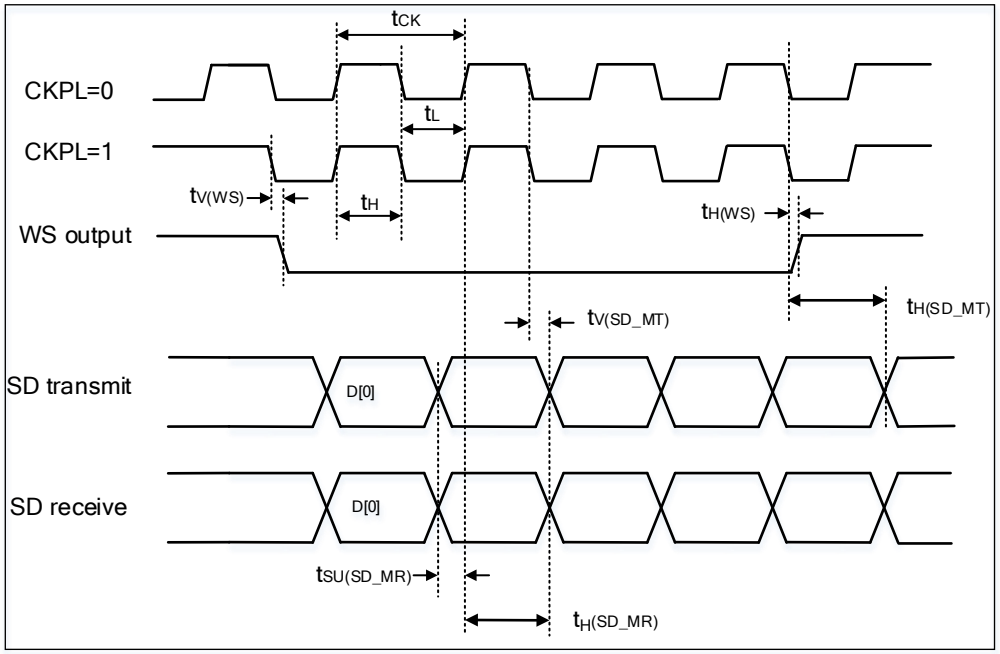
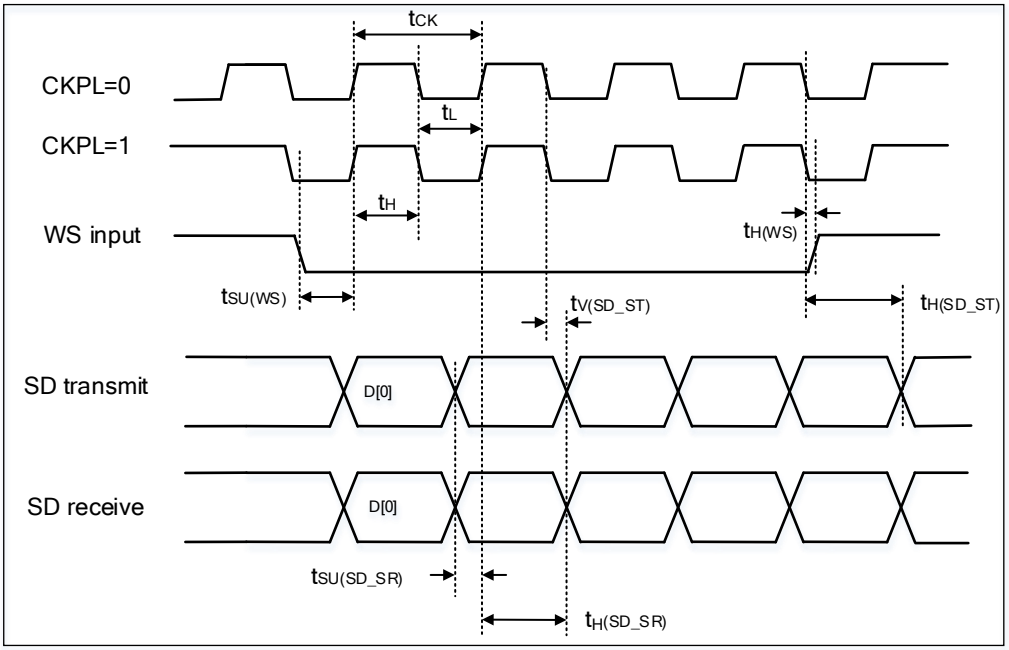


Figure 3-7. I2S timing diagram - slave mode



3.20. Temperature monitoring

Table 3-40. Temperature monitoring characteristics (1)

Symbol	Description	Min	Typ	Max	Unit
$TEMP_{high}$	PMU_CFG_TEMP1SEL=0	-	145	-	°C
	PMU_CFG_TEMP1SEL=1	-	155	-	

(1) Value guaranteed by design, not 100% tested in production.

3.21. CAN

Refer to
GPIO
Table 3-24. I/O DC characteristics, 3.3V Range *(2.97V-3.63V) (1), Table 3-25. I/O DC characteristics, 5.0V Range (4.5V-5.5V) (1)* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

3.22. QSPI

Table 3-41. Standard QSPI characteristics for GD32A711B/A712B (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SDR mode						
f_{SCK} $1/t_{CK}$	SCK clock frequency	-	-	-	60	MHz
$t_{w(CKH)}$	SCK clock high time, even division	-	t_{CK} /2	-	t_{CK} /2+1	ns
	SCK clock high time, odd division	-	(n/2)* t_{CK} / (n+1)	-	(n/2)* t_{CK} / (n+1)+1	ns
$t_{w(CKL)}$	SCK clock low time, even division	-	t_{CK} /2-1	-	t_{CK} /2	ns
	SCK clock low time, odd division	-	(n/2+1)* t_{CK} / (n+1)-1	-	(n/2+1)* t_{CK} /(n+1)	ns
$t_{V(OUT)}$	Data output valid time	-	-	0	1	ns
$t_{H(OUT)}$	Data output hold time	-	-	0	1	ns
$t_{SU(IN)}$	Data input setup time	-	1.5	-	-	ns
$t_{H(IN)}$	Data input hold time	-	4	-	-	ns
DDR mode						
f_{SCK} $1/t_{CK}$	SCK clock frequency	-	-	-	60	MHz
$t_{w(CKH)}$	SCK clock high time, even division	-	t_{CK}/2	-	t_{CK} /2+1	ns
	SCK clock high time, odd division	-	(n/2)* t_{CK} / (n+1)	-	(n/2)* t_{CK} / (n+1)+1	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(CKL)}$	SCK clock low time, even division	-	t_{CK} /2-1	-	t_{CK} /2	ns
	SCK clock low time, odd division	-	(n/2+1)* t_{CK} / (n+1)-1	-	(n/2+1)* t_{CK} /(n+1)	ns
$t_{V(OUT)}$	Data output valid time	-	-	0	1	ns
$t_{H(OUT)}$	Data output hold time	-	-	0	1	ns
$t_{SU(IN)}$	Data input setup time	-	1	-	-	ns
$t_{H(IN)}$	Data input hold time	-	1	-	-	ns

(1) Value guaranteed by design, not 100% tested in production.

Table 3-42. Standard QSPI characteristics for GD32A711A/A712A (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SDR mode						
f_{SCK} $1/t_{CK}$	SCK clock frequency	-	-	-	80	MHz
$t_{w(CKH)}$	SCK clock high time, even division	-	t_{CK} /2	-	t_{CK} /2+1	ns
	SCK clock high time, odd division	-	(n/2)* t_{CK} / (n+1)	-	(n/2)* t_{CK} / (n+1)+1	ns
$t_{w(CKL)}$	SCK clock low time, even division	-	tCK/2-1	-	tCK/2	ns
	SCK clock low time, odd division	-	(n/2+1)* t_{CK} / (n+1)-1	-	(n/2+1)* t_{CK} /(n+1)	ns
$t_{V(OUT)}$	Data output valid time	-	-	0	1	ns
$t_{H(OUT)}$	Data output hold time	-	-	0	1	ns
$t_{SU(IN)}$	Data input setup time	-	1.5	-	-	ns
$t_{H(IN)}$	Data input hold time	-	4	-	-	ns
DDR mode						
f_{SCK} $1/t_{CK}$	SCK clock frequency	-	-	-	80	MHz
$t_{w(CKH)}$	SCK clock high time, even division	-	t_{CK} /2	-	t_{CK} /2+1	ns
	SCK clock high time, odd division	-	(n/2)* t_{CK} / (n+1)	-	(n/2)* t_{CK} / (n+1)+1	ns
$t_{w(CKL)}$	SCK clock low time, even division	-	t_{CK} /2-1	-	t_{CK} /2	ns
	SCK clock low time, odd division	-	(n/2+1)* t_{CK} / (n+1)-1	-	(n/2+1)* t_{CK} /(n+1)	ns
$t_{V(OUT)}$	Data output valid time	-	-	0	1	ns
$t_{H(OUT)}$	Data output hold time	-	-	0	1	ns
$t_{SU(IN)}$	Data input setup time	-	1	-	-	ns
$t_{H(IN)}$	Data input hold time	-	1	-	-	ns

(1) Value guaranteed by design, not 100% tested in production

Figure 3-8. QSPI timing diagram - SDR mode

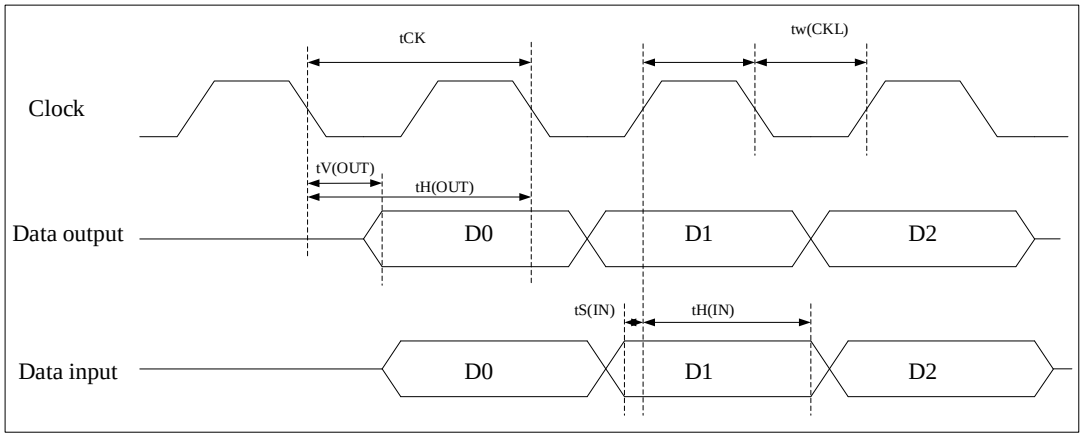
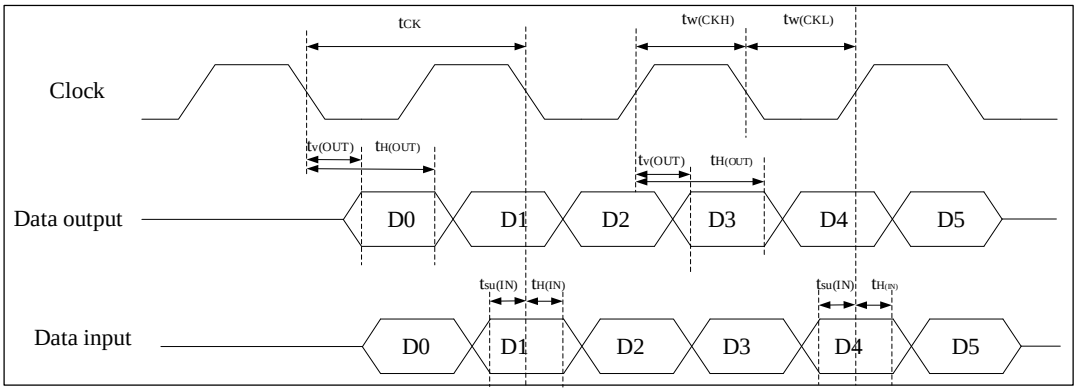


Figure 3-9. QSPI timing diagram - DDR mode



3.23. Comparators

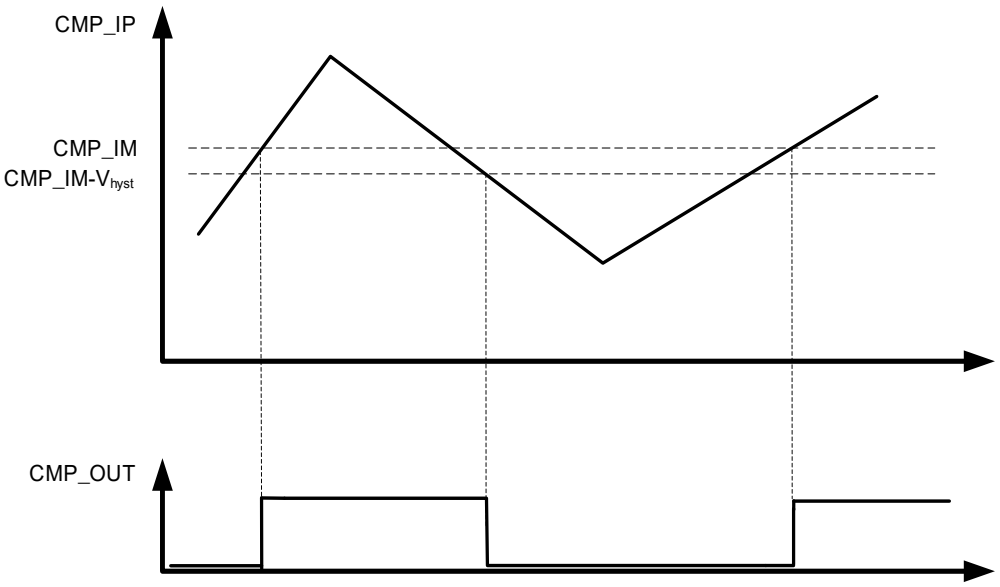
Table 3-43. CMP characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage	-	2.97	5	5.5	V
V_{IN}	Input voltage range	-	0	-	V_{DDA}	V
V_{BG}	Scaler input voltage	-	-	V_{REFINT}	-	V
V_{SC}	Scaler offset voltage	-	-	2	-	mV
I_{DDA}(SCALER)	Scaler static consumption from V_{DDA}	BEN = 0 (bridge disable)	-	400	-	nA
		BEN = 1 (bridge enable)	-	1.6	-	μA
t_{START_SCALER}	Scaler startup time	-	-	-	90	μs
t_D	Propagation delay for 200 mV step with 100 mV overdrive	low power mode	-	391	-	ns
		Medium power mode	-	178	-	ns
		High speed power mode	-	57	-	ns
I_{DD}	Current consumption	low power mode	-	2.5	-	μA
		Medium power mode	-	7	-	

Symbol	Description	Conditions	Min	Typ	Max	Unit
		High speed power mode	-	103	-	
V_{offset}	Offset error	-	-	5	-	mV
V_{hyst}	Hysteresis Voltage	No Hysteresis	-	0	-	mV
		Low Hysteresis	-	15	-	
		Medium Hysteresis	-	31	-	
		High Hysteresis	-	47	-	

(1) Value guaranteed by design, not 100% tested in production.

Figure 3-10. CMP hysteresis



3.24. Temperature sensor

Table 3-44. Temperature sensor characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{25}	Uncalibrated Offset	T_A= 25°C	-	1207	-	mV
E_{OFF}	Uncalibrated Offset Error	T_A = 25°C	-	3.96	-	mV
Avg_Slope	Average slope	-	-	4	-	mV/°C
E_M	Slope Error	-	-	11	-	µV/°C
LIN	Linearity	T_A = -40 °C to 125 °C	-	±2	-	°C
t_{s_temp}	ADC sampling time when reading the temperature	-	10	-	-	µs
t_{ON}	Turn-on Time	f_{ADC} = 16 MHz, t_{s_temp} = 10 µs	-	50	-	µs
ETOT (2)	Temp Sensor Error Using Typical Slope and Factory-Calibrated Offset	T_A = -40 °C to 125 °C	-	±5	-	°C

(1) Value guaranteed by design, not 100% tested in production.

(2) The factory-calibrated offset value (ADC code value) is stored in the read-only area of flash in locations 0x1FFFF7F8.

4. Package information

4.1. LQFP176 package outline dimensions

Figure 4-1. LQFP176 package outline

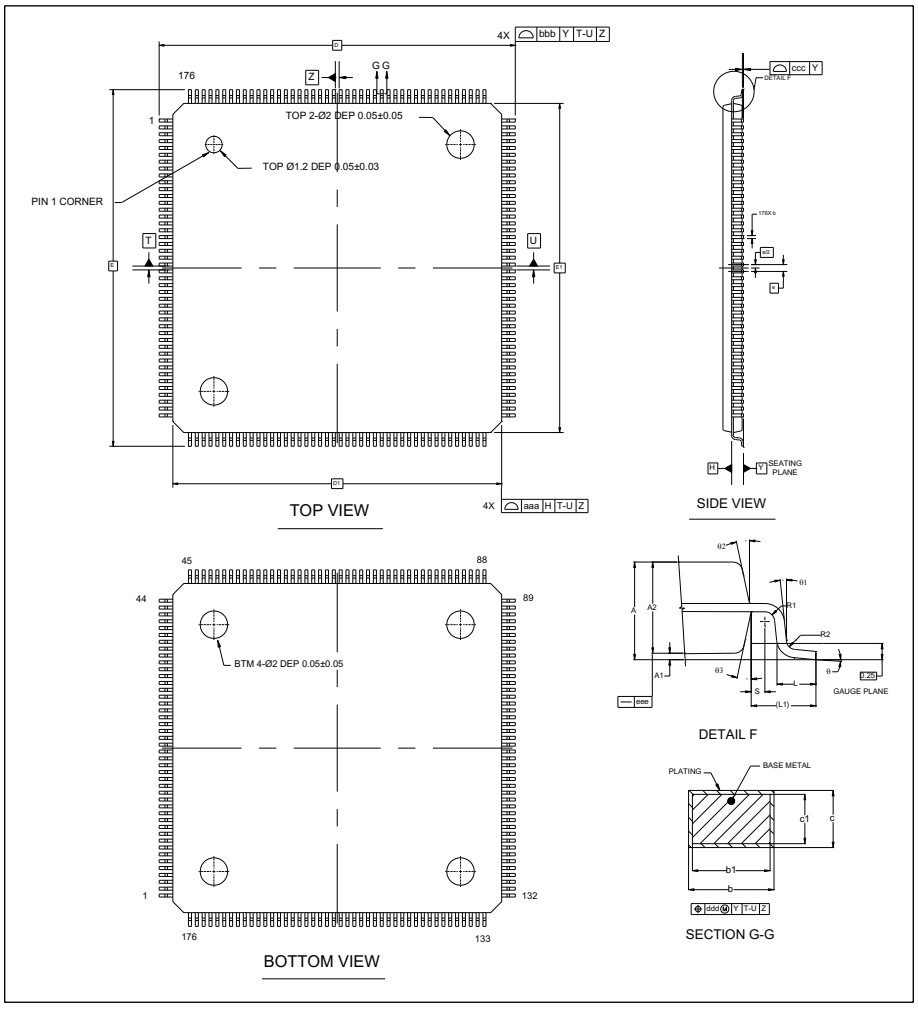


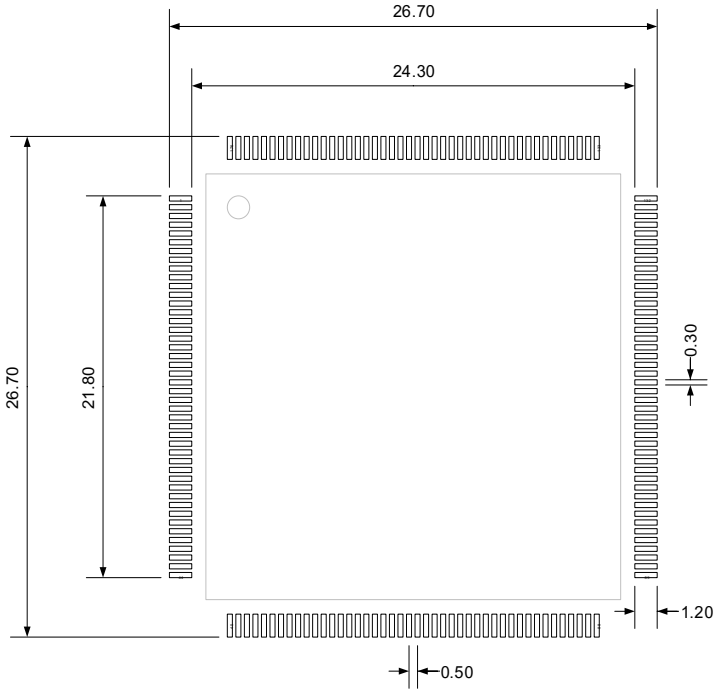
Table 4-1. LQFP176 package dimensions

Symbol	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.18	0.22	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.127	0.134
D	-	26.00	-
D1	-	24.00	-
E	-	26.00	-

Symbol	Min	Typ	Max
E1	-	24.00	-
e	-	0.50	-
L	0.45	0.60	0.75
L1	-	1.00	-
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
θ3	11°	12°	13°
aaa	-	0.20	-
bbb	-	0.20	-
ccc	-	0.08	-
ddd	-	0.08	-
eee	-	0.05	-

(Original dimensions are in millimeters)

Figure 4-2. LQFP176 recommended footprint



(Original dimensions are in millimeters)

4.2. LQFP144 package outline dimensions

Figure 4-3. LQFP144 package outline

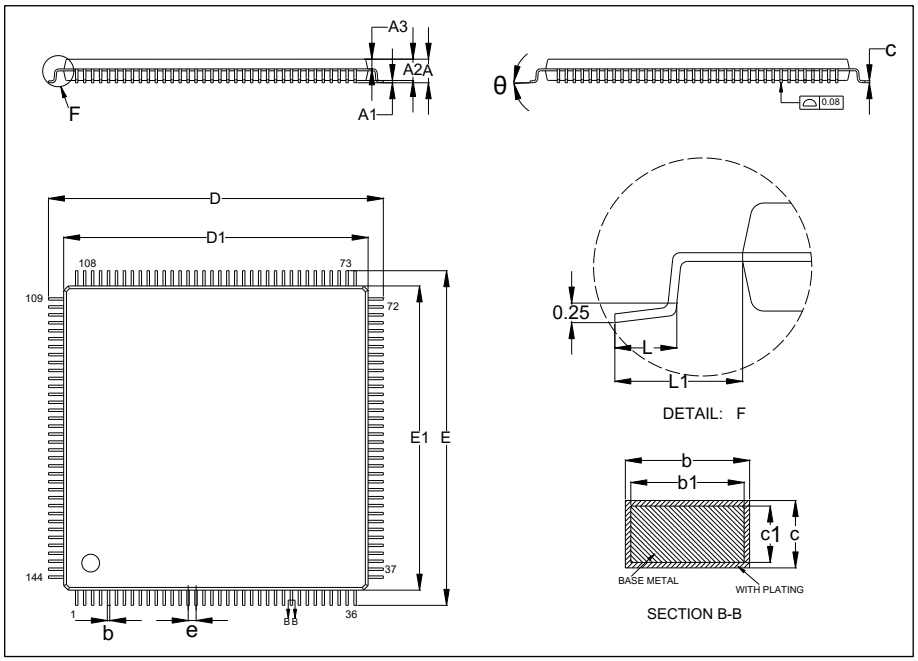
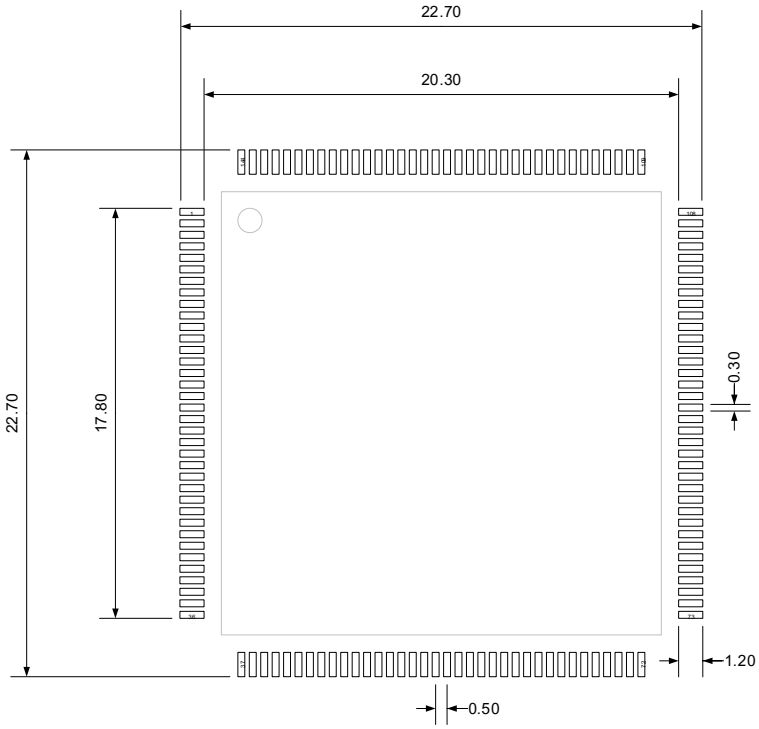


Table 4-2. LQFP144 package dimensions

Symbol	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	21.80	22.00	22.20
D1	19.90	20.00	20.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
e	-	0.50	-
L	0.45	-	0.75
L1	-	1.00	-
θ	0°	-	7°

(Original dimensions are in millimeters)

Figure 4-4. LQFP144 recommended footprint



(Original dimensions are in millimeters)

4.3. LQFP100 package outline dimensions

Figure 4-5. LQFP100 package outline

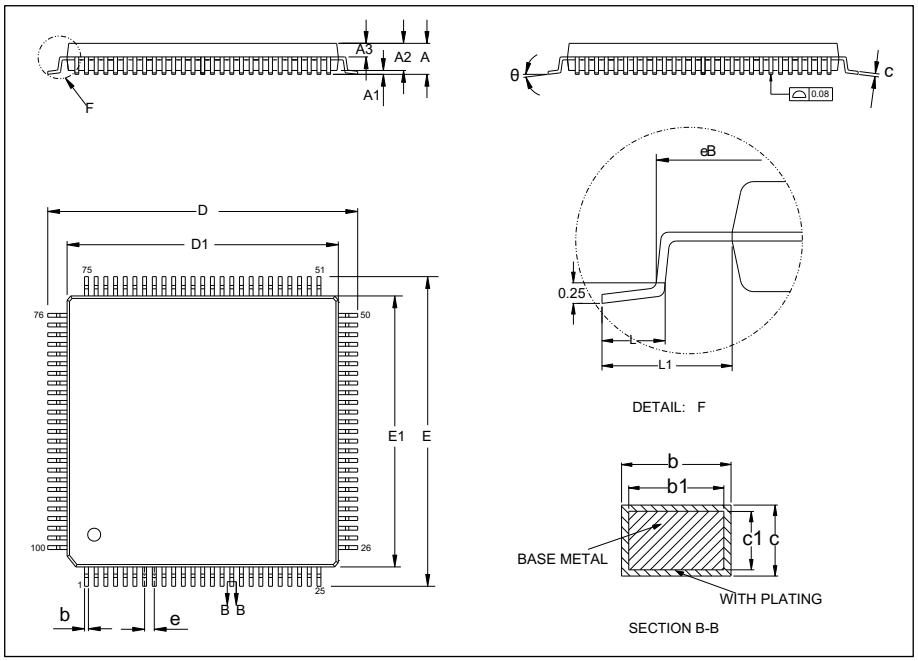
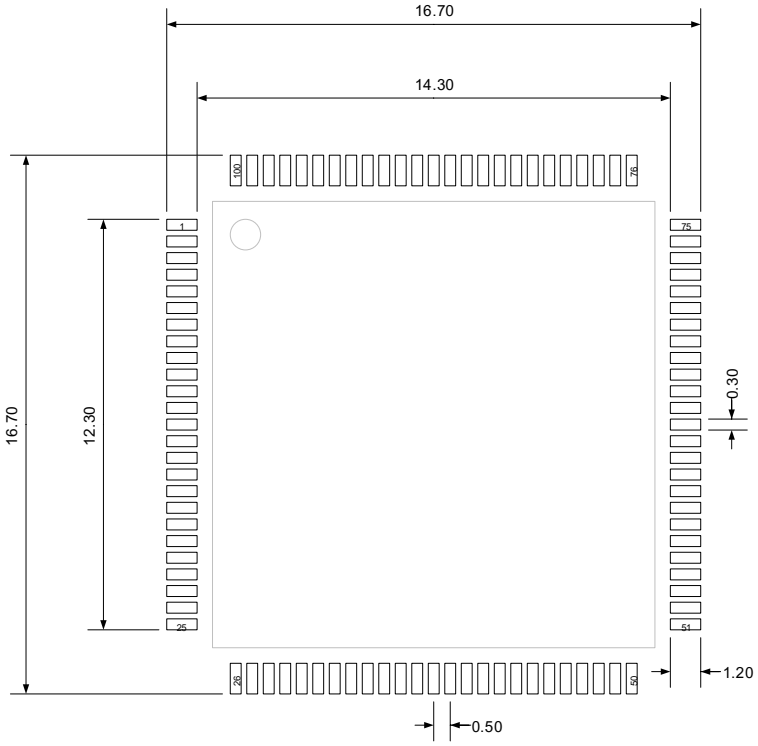


Table 4-3. LQFP100 package dimensions

Symbol	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
e	-	0.50	-
eB	15.05	-	15.35
L	0.45	-	0.75
L1	-	1.00	-
θ	0°	-	7°

(Original dimensions are in millimeters)

Figure 4-6. LQFP100 recommended footprint



(Original dimensions are in millimeters)

4.4. LQFP64 package outline dimensions

Figure 4-7. LQFP64 package outline

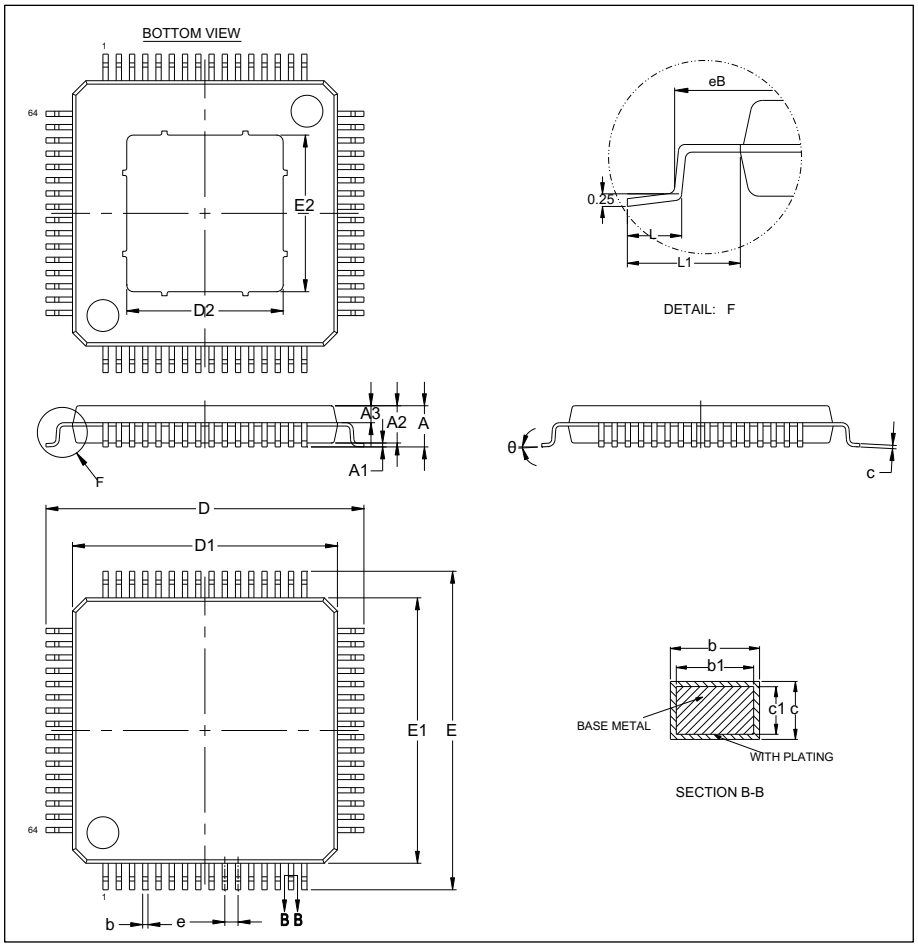


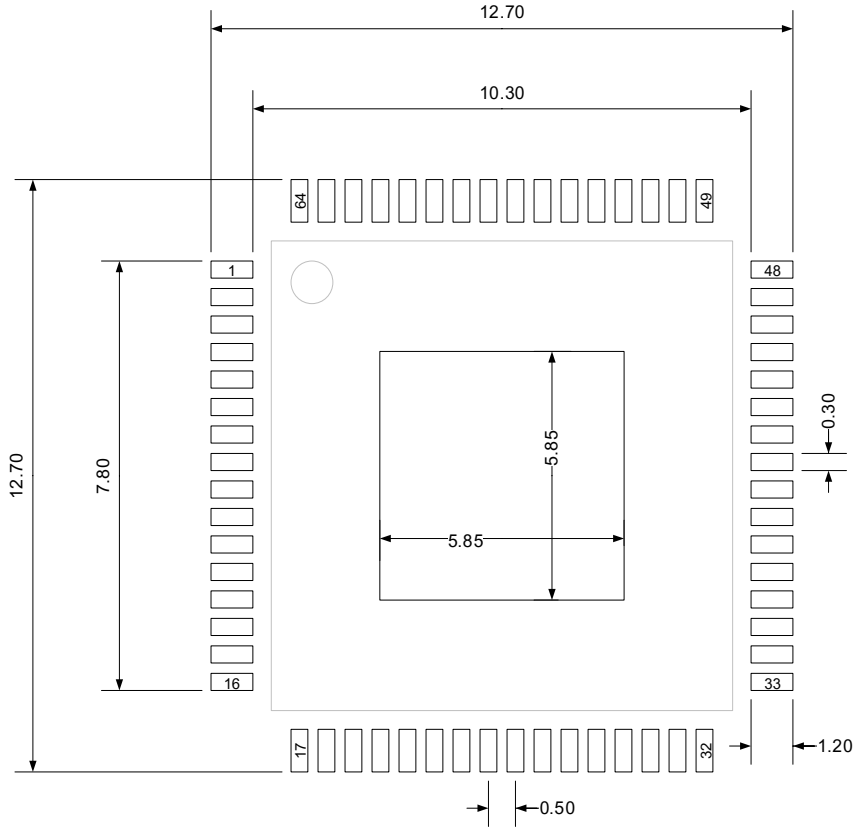
Table 4-4. LQFP64 package dimensions

Symbol	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
D2	-	5.90	-
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
E2	-	5.90	-

Symbol	Min	Typ	Max
e	-	0.50	-
eB	11.05	-	11.25
L	0.45	-	0.75
L1	-	1.00	-
θ	0°	-	7°

(Original dimensions are in millimeters)

Figure 4-8. LQFP64 recommended footprint



(Original dimensions are in millimeters)

4.5. QFN56 package outline dimensions

Figure 4-9. QFN56 package outline

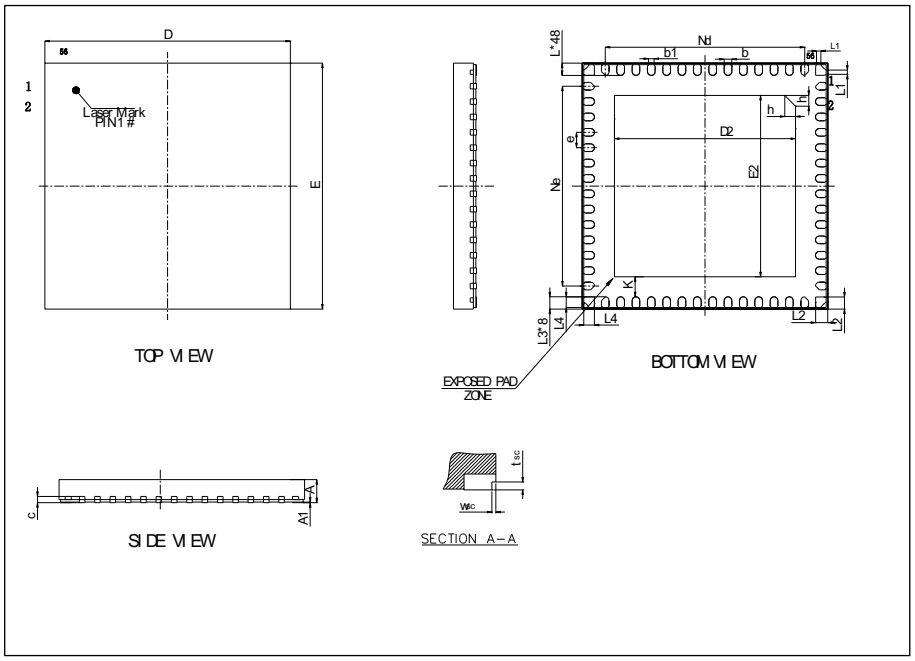
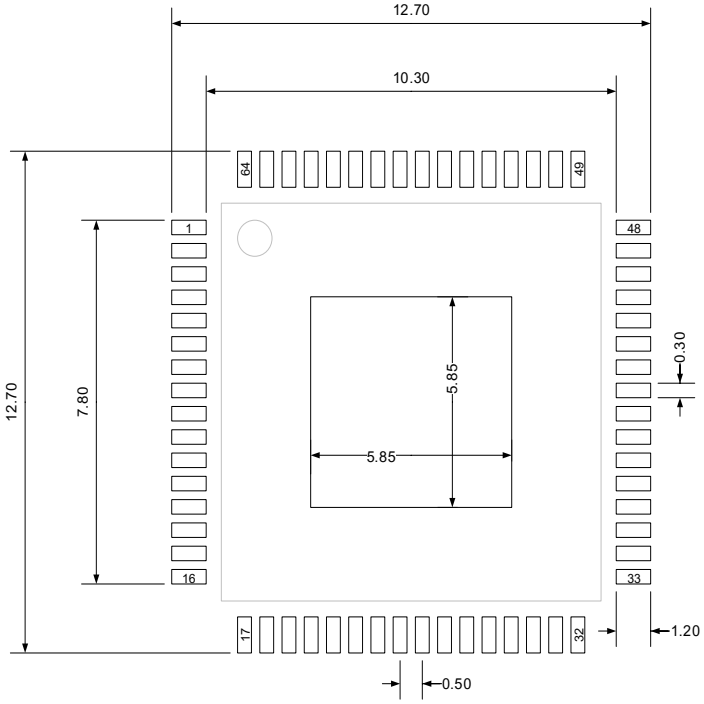


Table 4-5. QFN56 package dimensions

Symbol	Min	Typ	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1		0.18	
c		0.203	
D	7.90	8.00	8.10
D2	5.80	5.90	6.00
E	7.90	8.00	8.10
E2	5.80	5.90	6.00
e		0.50	
Nd		6.50	
Ne		6.50	
L	0.35	0.40	0.45
L1		0.14	
L2		0.395	
L3	0.30	0.40	0.50
L4		0.35	
h	0.30	0.35	0.40
K		0.65	
Wsc	0.025	-	0.105
tsc	0.05	-	0.18

(Original dimensions are in millimeters)

Figure 4-10. QFN56 recommended footprint



(Original dimensions are in millimeters)

4.6. Moisture Sensitivity Level

Table 4-6. Moisture Sensitivity Level (1)

Package	MSL
All Packages	3

(1) Determined in accordance with the 'Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices' in the IPC/JEDEC J-STD-020 standard.

4.7. Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter "θ". For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

θ_{JA}: Thermal resistance, junction-to-ambient.

θ_{JB}: Thermal resistance, junction-to-board.

θ_{JC}: Thermal resistance, junction-to-case.

Ψ_{JB}: Thermal characterization parameter, junction-to-board.

Ψ_{JT}: Thermal characterization parameter, junction-to-top center.

$$\theta_{JA}=(T_J-T_A)/P_D \quad (4\text{-}1)$$

$$\theta_{JB}=(T_J-T_B)/P_D \quad (4\text{-}2)$$

$$\theta_{JC}=(T_J-T_C)/P_D \quad (4\text{-}3)$$

Where, T_J = Junction temperature.

T_A = Ambient temperature

T_B = Board temperature

T_C = Case temperature which is monitoring on package surface

P_D = Total power dissipation

θ_{JA} represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower θ_{JA} can be considerate as better overall thermal performance. θ_{JA} is generally used to estimate junction temperature.

θ_{JB} is used to measure the heat flow resistance between the chip surface and the PCB board.

θ_{JC} represents the thermal resistance between the chip surface and the package top case. θ_{JC} is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

Table 4-7. Package thermal characteristics(1)

Symbol	Condition	Package	Value	Unit
θ_{JA}	Natural convection, 2S2P PCB	LQFP176	32.9	°C/W
		LQFP144	40.53	
		LQFP100	39.74	
		LQFP64	28.88	
		QFN56	20.98	
θ_{JB}	Cold plate, 2S2P PCB	LQFP176	25.6	°C/W
		LQFP144	28.25	
		LQFP100	26.17	
		LQFP64	9.05	
		QFN56	3.9	
θ_{JC}	Cold plate, 2S2P PCB	LQFP176	9.3	°C/W
		LQFP144	10.38	
		LQFP100	10.81	
		LQFP64	10.98	
		QFN56	6.08	
Ψ_{JB}	Natural convection, 2S2P PCB	LQFP176	25	°C/W
		LQFP144	29.23	
		LQFP100	26.54	
		LQFP64	9.09	
		QFN56	4.11	
Ψ_{JT}	Natural convection, 2S2P PCB	LQFP176	0.4	°C/W
		LQFP144	0.38	
		LQFP100	0.41	
		LQFP64	0.43	
		QFN56	0.059	

(1) Thermal characteristics are based on simulation, and meet JEDEC specification.

5. Revision history

Table 5-1. Revision history

Rev.	Description	Date
0.0	1. Initial Release	Jun.06, 2025
0.1	1. Update 2.4 / 2.6 section 2. Update CPN	Jul.17, 2025
0.2	1. Update 2.6 section. 2. Update 4 chapter.	Aug.28, 2025
0.3	1. Update 2.4 section. 2. Update 4 chapter.	Oct.18, 2025
0.4	1. Delete 2.4 Memory map 2. Delete 3. Functional descriptions 3. Delete 2.6.x..pin definitions and add attachment	Dec 19, 2025
1.0	1. Delete 2.4 Memory map 2. Delete 3. Functional descriptions 3. Update 2.1 / 2.2 section,160Mhz/120Mhz information,add CPN figure 4. Update 1. Section 160Mhz/120Mhz information 5. Add the differences in ClockTree for 160/120MHz across different chip versions. 6. Add descriptions in the ClockTree regarding LXTAL accessibility for different package types.(c) Customer requirements 7. Update Memory characteristics in 3.11 Section 8. Add max value in 3.4/3.13 Section, add ADC accuracy in 3.15 section 9. Update IRC40K accuracy in 3.9 Section 10. Remove the Pinouts package diagram in section 2.3 and add a description to refer to the "GD32A711_712_PinMux_Matrix" attachment for viewing.	Jan. 13, 2026
1.1	1. In the attachment GD32A711_712_PinMux_Matrix Release V1.1.xlsx, add the QFN56 package to the PinMux, IO_Signal, and Peripheral_Mux sheets respectively, and add a new sheet named QFN56_Pinouts. 2. Update Table 2.1， add GD32A712BPU7TB/ GD32A712BPU3TB information 3. Add QFN56 package outline dimensions in 4.5 Section	March 25, 2026
1.2	1. Delete the Max parameter in table 3-9 and modify its annotation (5) : The reference for the MAX value is 160MHz, 125°C. 2. Modify the name of the table in Section 3.8 They are respectively; table3-15 High speed external clock (HXTAL); table3-16 High speed external clock (HXTAL) in bypass mode; table3-17 Low speed external clock (LXTAL); table3-18 Low speed external clock (LXTAL) in bypass mode. 3. Delete the "For" in the frequency-related parameter coditions in table 3-3;	Sep 11, 2026

Rev.	Description	Date
	4. Add the description of default mode in pinmux and support for the QFN56 drop-down box option. 5. Remove "characteristics" from the title of the Electrical characteristics sub-chapter. 6. Update the names and formats of the two tables in Device information. 7. Update Part Number information. 8. Change GD32A711_712,GD32A711_712xxxxB,GD32A711_712AxxxxB(GD32A711_712BxxxxB) and GD32A711x&A712x to GD32A711/A712. 9. Change GD32A711B/A712BxxxxB to GD32A711B/A712B; Change GD32A711A/ A712AxxxxB to GD32A711A/A712A. 10. Revision history format adjustment. 11. Add headers and footers. 12. Table 3-29. ADC characteristics deletes V(AIN). 13. Section 3.4. Remove the word “indicative” from the text. 14. Table 3-3. Delete the power dissipation data. 15. Table 2-1. Remove GD32A712BPU7TB. 16. Table 3-2. Add note (2). 17. Table3-22. Add "PE(CYC)" and "t(RET)"data retention time conditions，add comment. 18. Add CMP comments under the table of Device information. 19. Font modification: Change the document font to Arial MT Pro. 20. SPI timing diagram modification. 21. QSPI timing diagram modification. 22. Chapter 3 Timer+WDG Deleted. 23. Add 4.6. Moisture Sensitivity Level. 24. Add a QFN56 package option and correct the default mode description in the PinMux sheet in the attached table. 25. Figure 2-3. Unify the division signs of "/" and "÷". 26. Delete the original "Table 3-30. ADC RAIN max for fADC = 16 MHz (1)"	

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